

L P C 1 7 8 8

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Title LPC1788 XPLORER++			
Size B	Document Number SCHEMATIC		Rev A.
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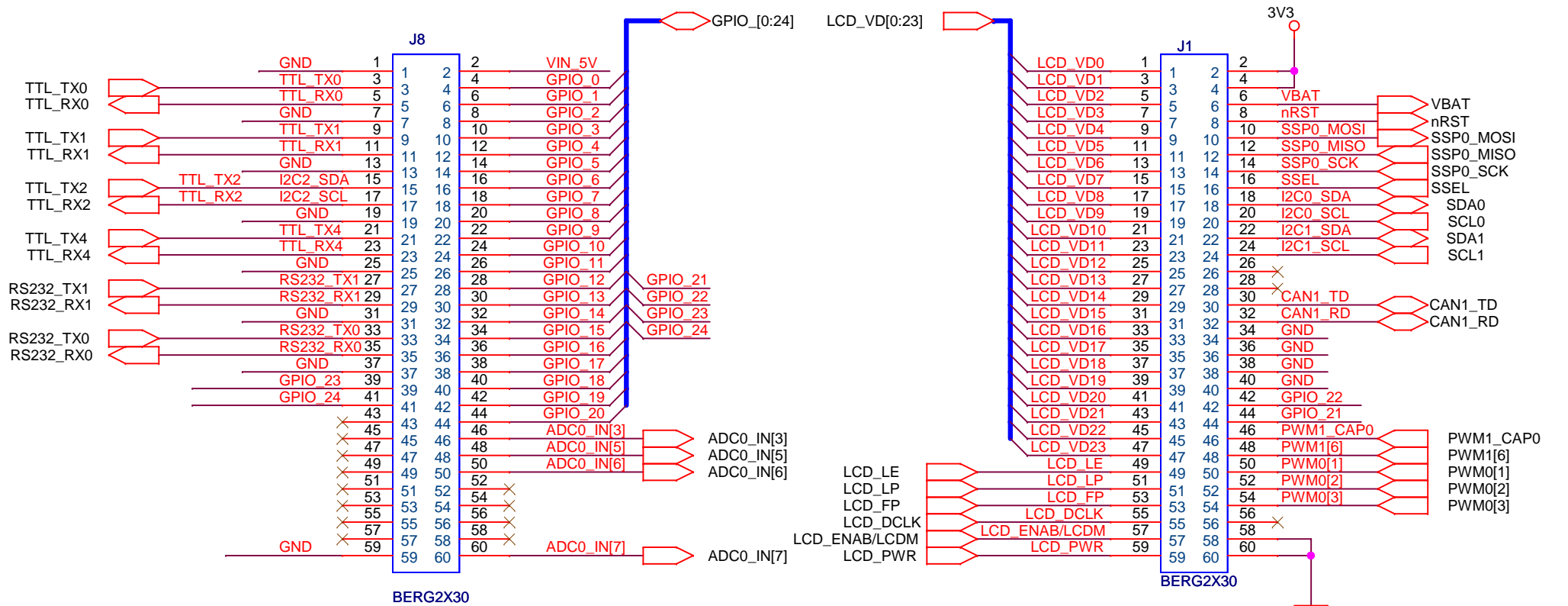
PIN OUT

PORT	HEADER J8	PORT
GND	GND 1 2	VIN_5V
P0[2]	TX0 3 4	GPIO_0
P0[3]	RX0 5 6	GPIO_1
GND	GND 7 8	GPIO_2
P0[15]	TX1 9 10	GPIO_3
P0[16]	RX1 11 12	GPIO_4
GND	GND 13 14	GPIO_5
P0[10]	TX2 15 16	GPIO_6
P0[11]	RX2 17 18	GPIO_7
GND	GND 19 20	GPIO_8
P5[4]	TX4 21 22	GPIO_9
P5[3]	RX4 23 24	GPIO_10
GND	GND 25 26	GPIO_11
RS232_TX1	RS232_TX1 27 28	GPIO_12
RS232_RX1	RS232_RX1 29 30	GPIO_13
GND	GND 31 32	GPIO_14
RS232_TX0	RS232_TX0 33 34	GPIO_15
RS232_RX0	RS232_RX0 35 36	GPIO_16
GND	GND 37 38	GPIO_17
P2[11]	GPIO_23 39 40	GPIO_18
P4[24]	GPIO_24 41 42	GPIO_19
-	NC 43 44	GPIO_20
-	NC 45 46	ADC0_IN[3]
-	NC 47 48	ADC0_IN[5]
-	NC 49 50	ADC0_IN[6]
-	NC 51 52	NC
-	NC 53 54	NC
-	NC 55 56	NC
-	NC 57 58	NC
GND	GND 59 60	ADC0_IN[7]
		P0[13]

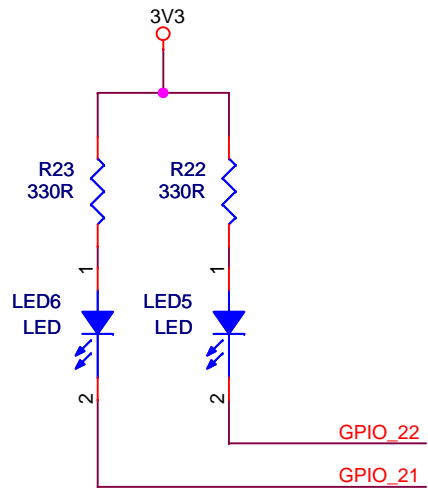
PORT	HEADER J1	PORT
P0[4]	LCD_VD0 1 2	3V3
P0[5]	LCD_VD1 3 4	3V3
P2[8]	LCD_VD2 5 6	VBAT
P4[29]	LCD_VD3 7 8	nRST
P2[6]	LCD_VD4 9 10	SSP0_MOSI
P2[7]	LCD_VD5 11 12	SSP0_MISO
P1[20]	LCD_VD6 13 14	SSP0_SCK
P2[9]	LCD_VD7 15 16	SSEL
P0[6]	LCD_VD8 17 18	I2C0_SDA
P0[7]	LCD_VD9 19 20	I2C0_SCL
P4[28]	LCD_VD10 21 22	I2C1_SDA
P1[21]	LCD_VD11 23 24	I2C1_SCL
P1[22]	LCD_VD12 25 26	NC
P1[23]	LCD_VD13 27 28	NC
P1[24]	LCD_VD14 29 30	CAN1_TD
P1[25]	LCD_VD15 31 32	CAN1_RD
P0[8]	LCD_VD16 33 34	GND
P0[9]	LCD_VD17 35 36	GND
P2[12]	LCD_VD18 37 38	GND
P2[13]	LCD_VD19 39 40	GND
P1[26]	LCD_VD20 41 42	GPIO_22
P1[27]	LCD_VD21 43 44	GPIO_21
P1[28]	LCD_VD22 45 46	PWM1_CAP0
P1[29]	LCD_VD23 47 48	PWM1[6]
P2[1]	LCD_LE 49 50	PWM0[1]
P2[5]	LCD_LP 51 52	PWM0[2]
P2[3]	LCD_FP 53 54	PWM0[3]
P2[2]	LCD_DCLK 55 56	NC
P2[4]	LCD_ENAB/LCDM 57 58	GND
P2[0]	LCD_PWR 59 60	GND
		3V3
		3V3
		VBAT
		RESET
		P0[18]
		P0[17]
		P2[22]
		P1[18]
		P0[27]
		P0[28]
		P2[14]
		P2[15]
		-
		-
		P0[1]
		P0[0]
		GND
		GND
		GND
		GND
		P1[6]
		P1[13]
		P1[28]
		P1[26]
		P1[2]
		P1[3]
		P1[5]
		-
		GND
		GND

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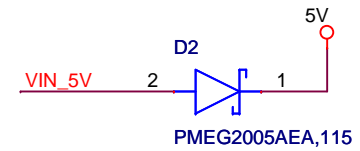
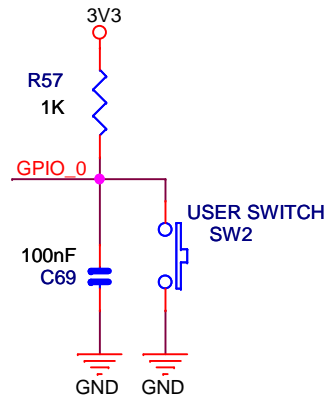
HEADER



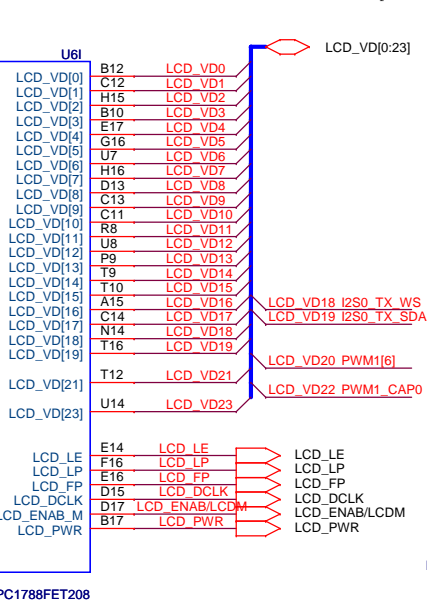
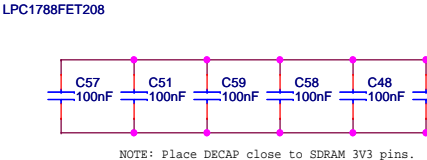
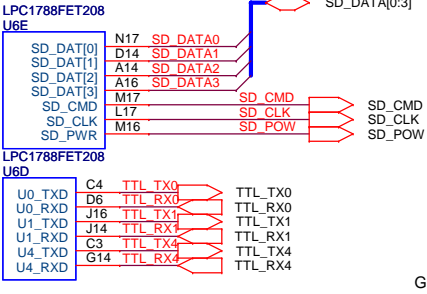
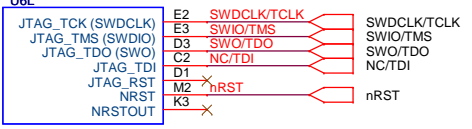
TEST LED



USER SWITCH

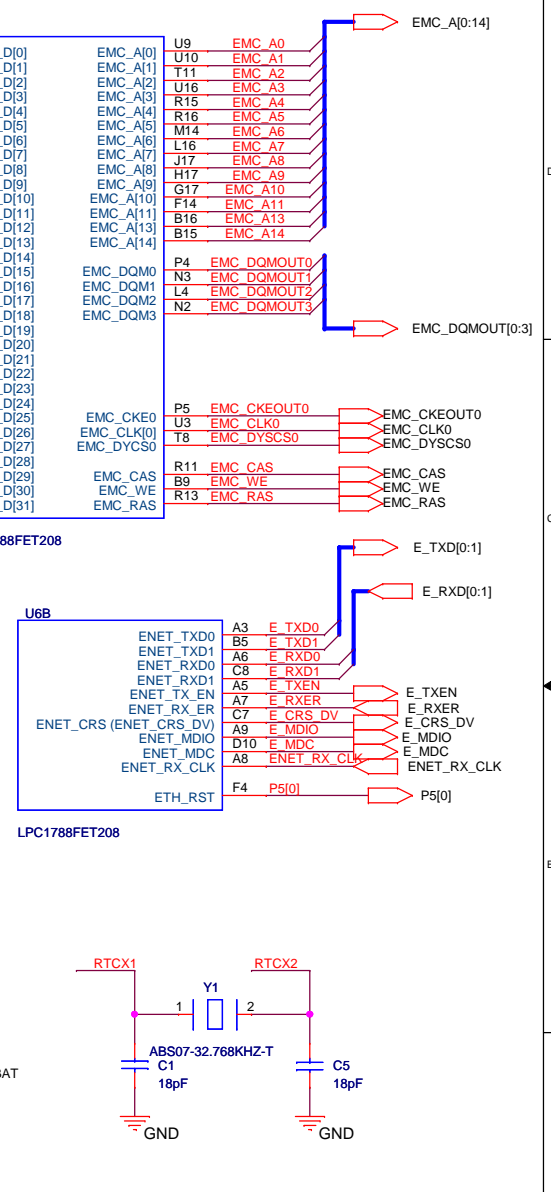
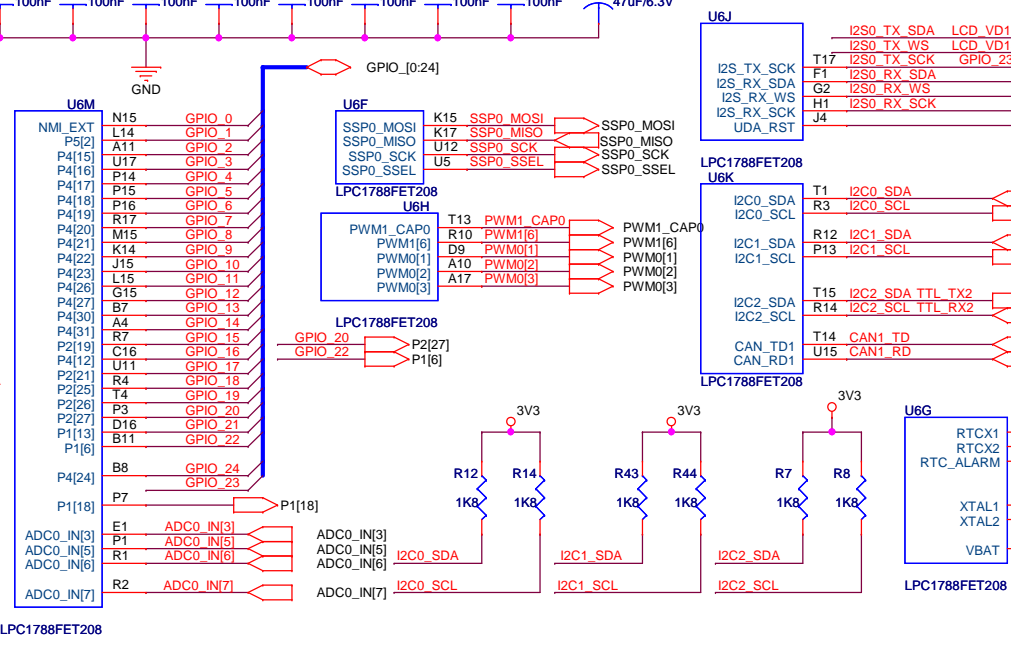
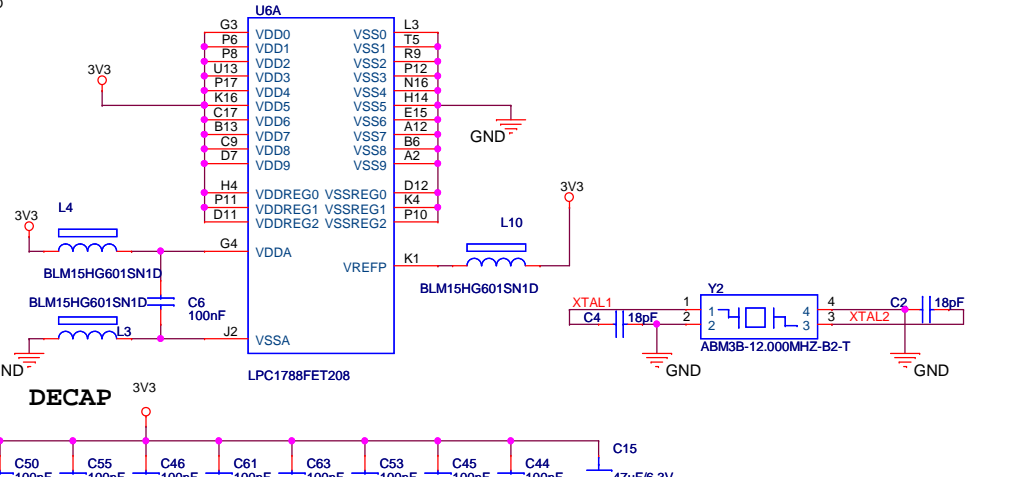


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NOTE:
LCD lines are multiplexed with I2S and PWM pin.
IMPACT: Can not use Audio and PWM when LCD is configured for 24-bit resolution.

LPC1788



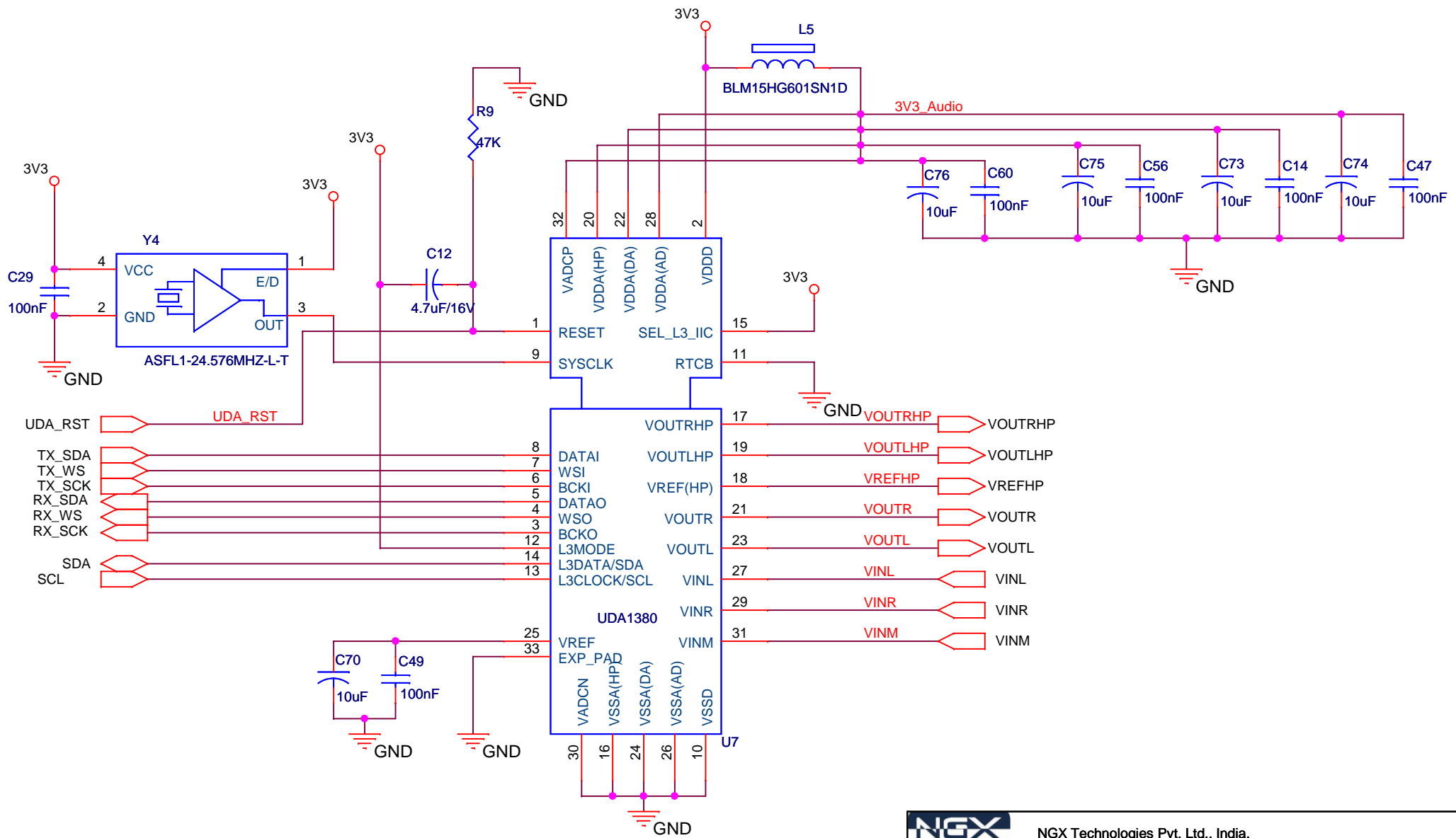
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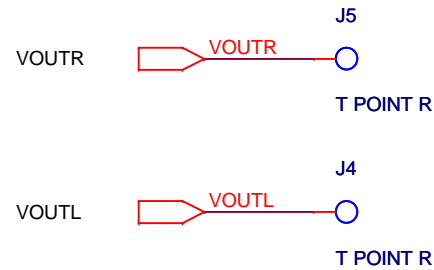
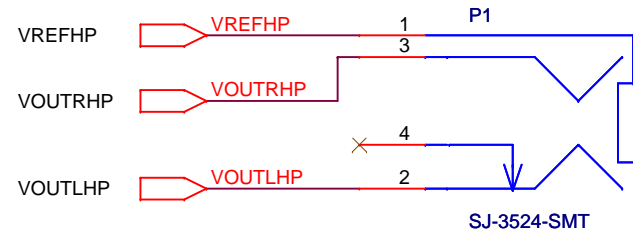
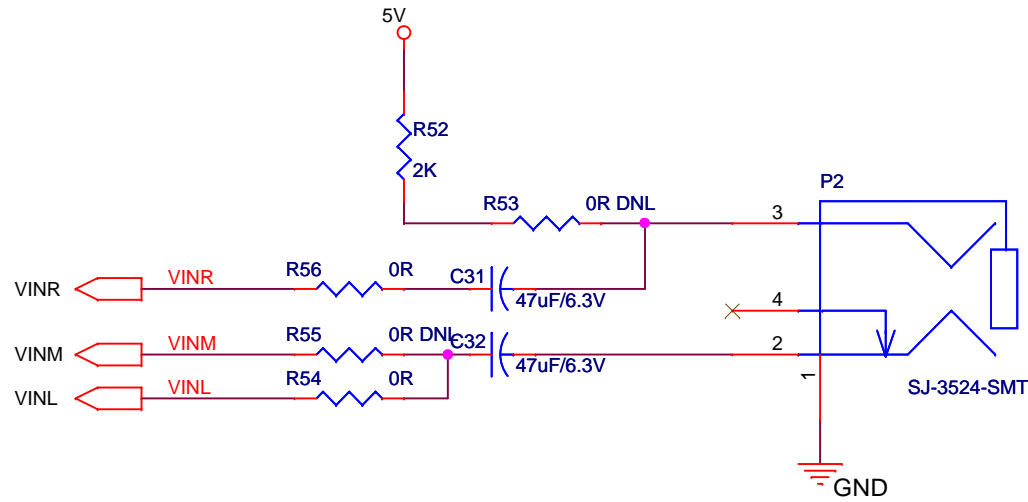
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UDA1380



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AUDIO JACK3.5MM



NOTE :

DNI R53, R55



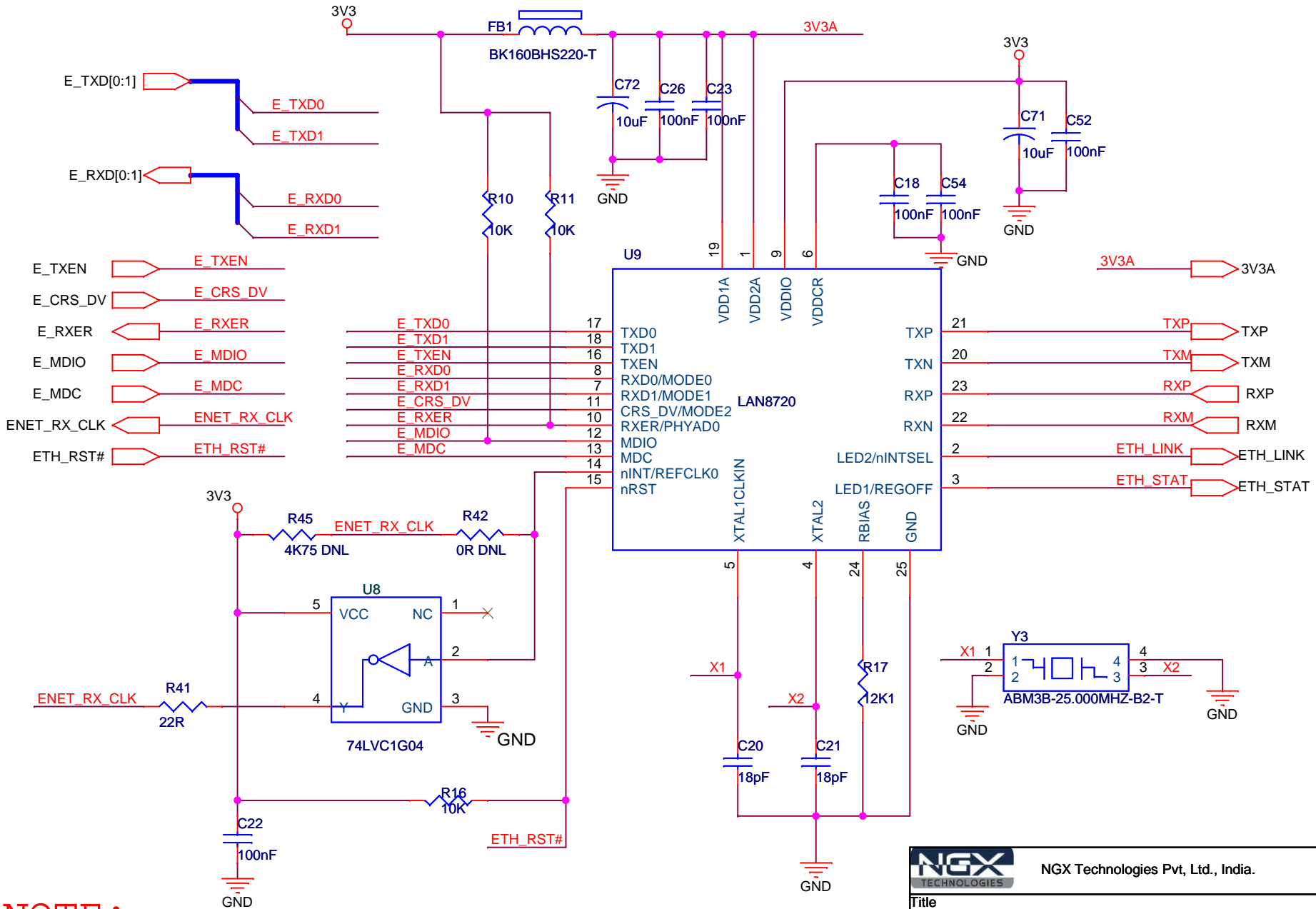
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Title
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ETHERNET LAN8720



NOTE :
DNI R45, R42



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Title

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Size
A

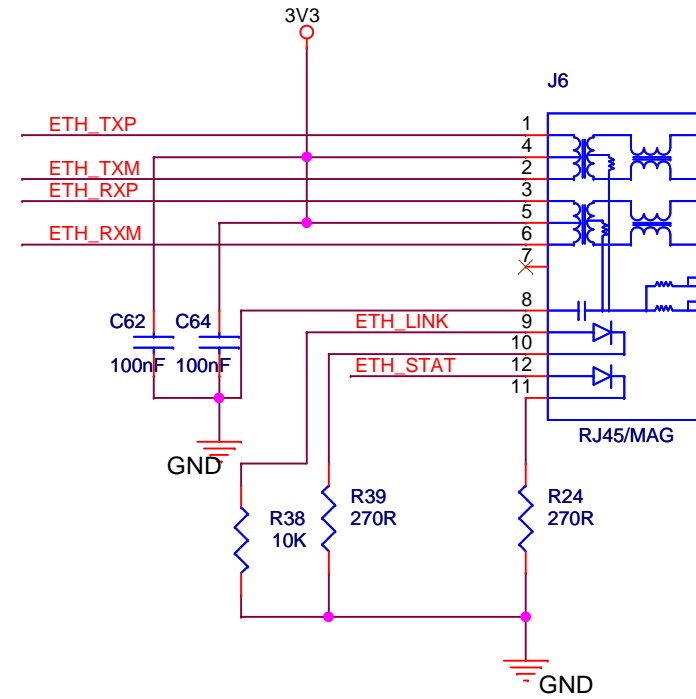
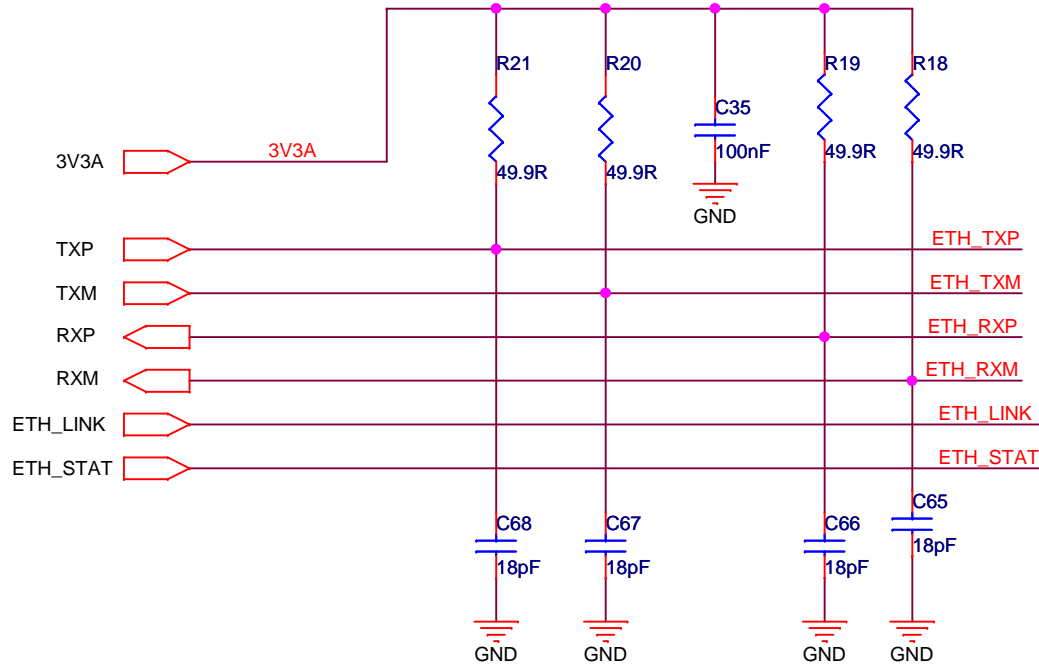
Document Number
ETHERNET_LAN8720

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A.

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RJ45 MAGNETICS



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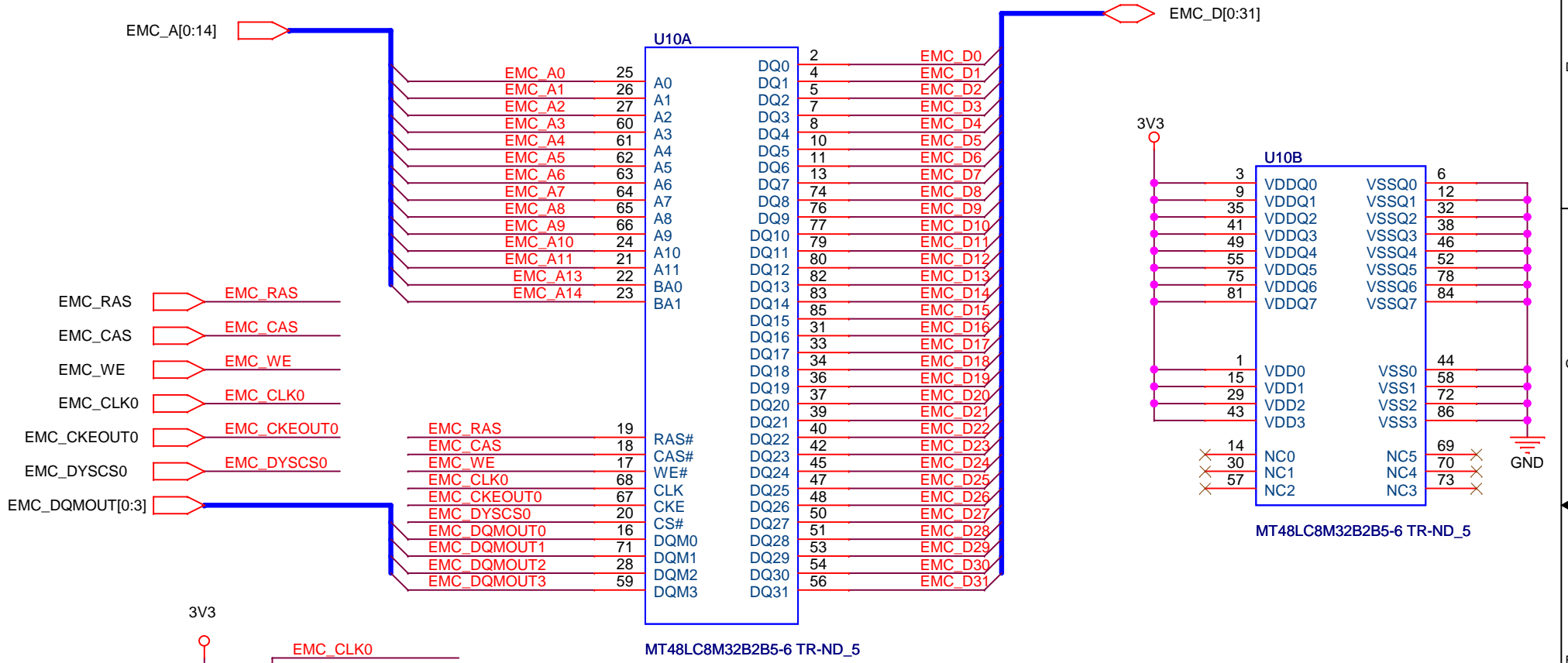
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SDRAM



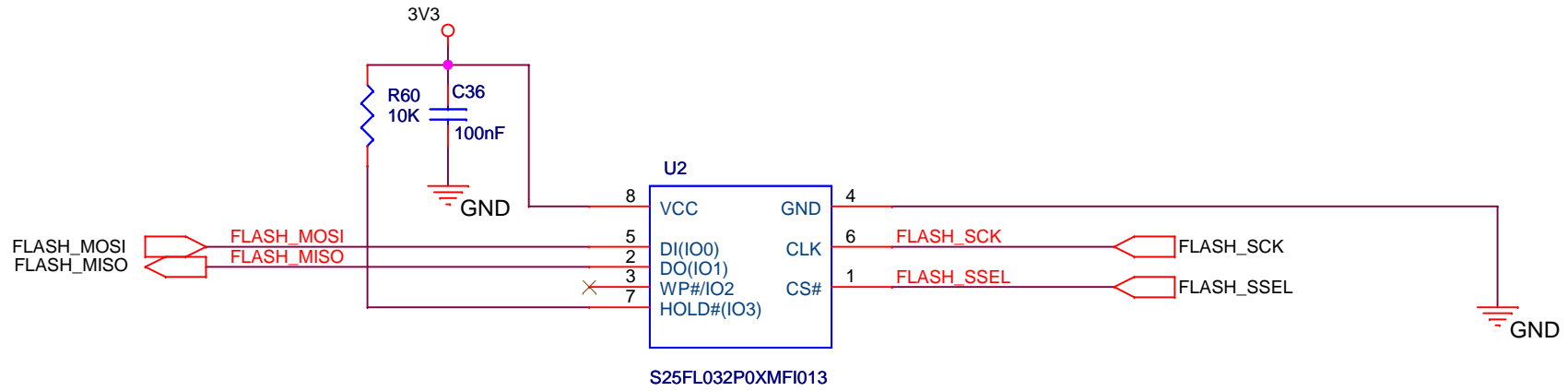
DECAP

NOTE: Place DECAP close to SDRAM 3V3 pins.

NOTE :
DNI R58 ,R59

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FLASH



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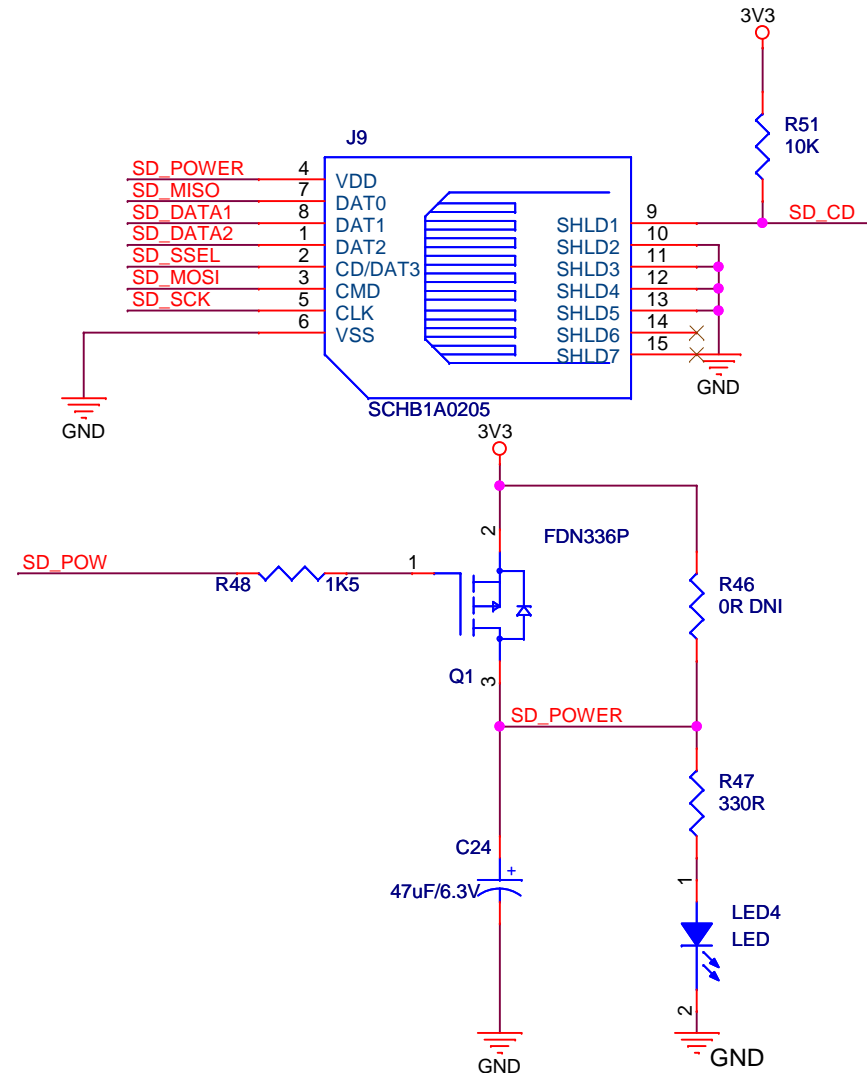
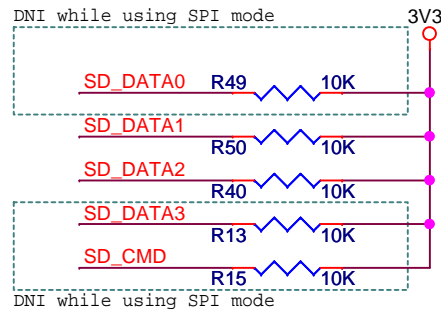
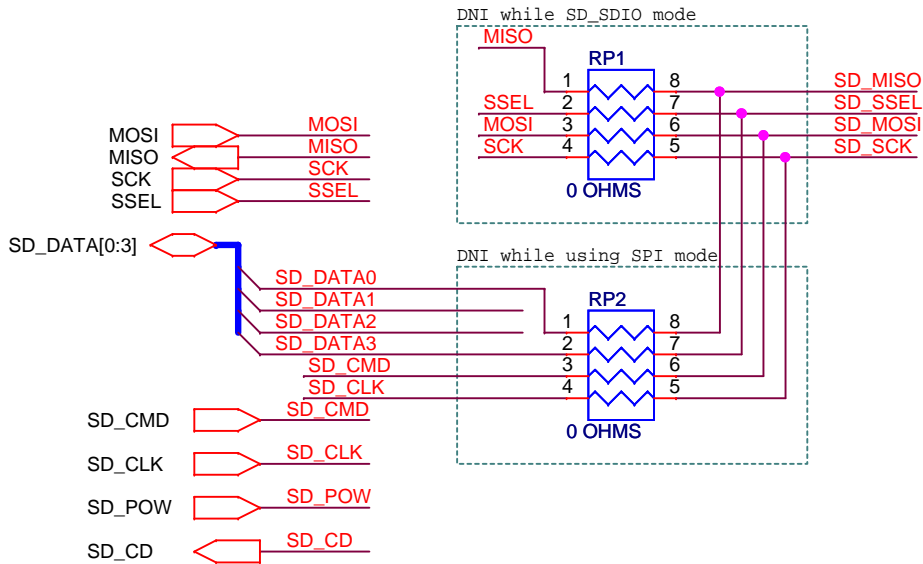
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FLASH

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MICRO SD CARD



NOTE :
DNI R46, RP1



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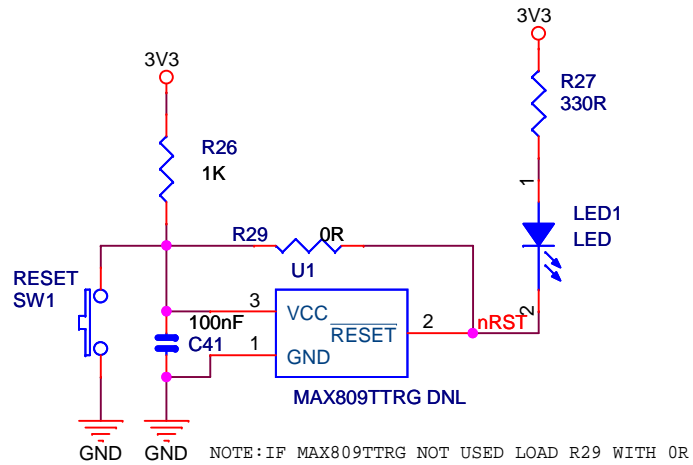
Size A Document Number
SD_MICRO_MMC

Rev A.

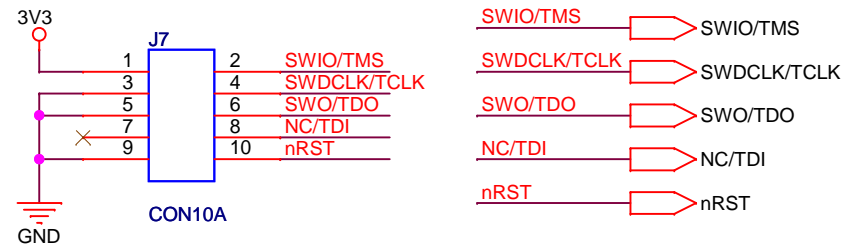
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RESET SWITCH



JTAG/SWD



NOTE :

DNI U1



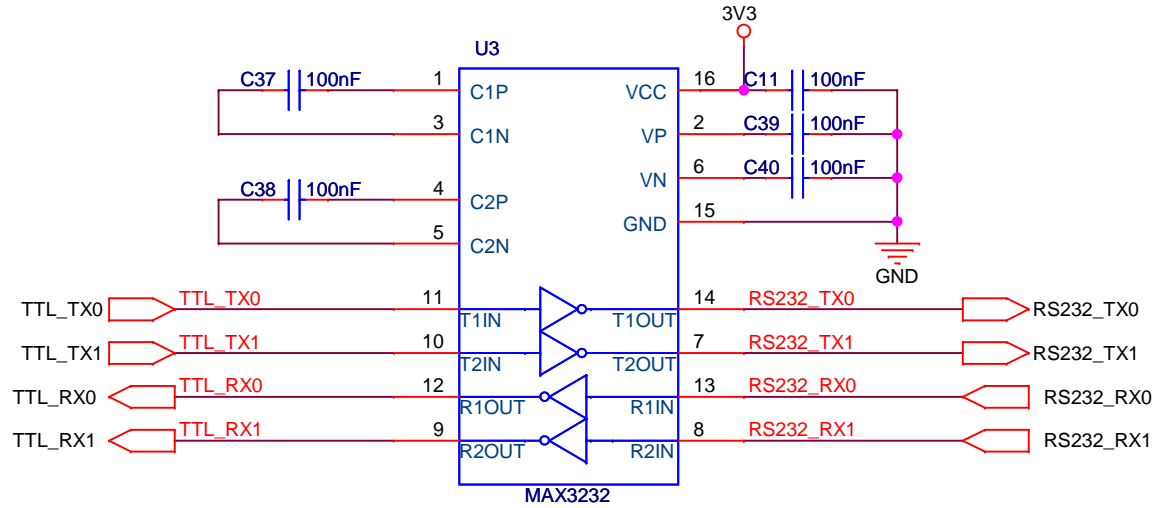
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UART SECTION



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A UART_MAX3232

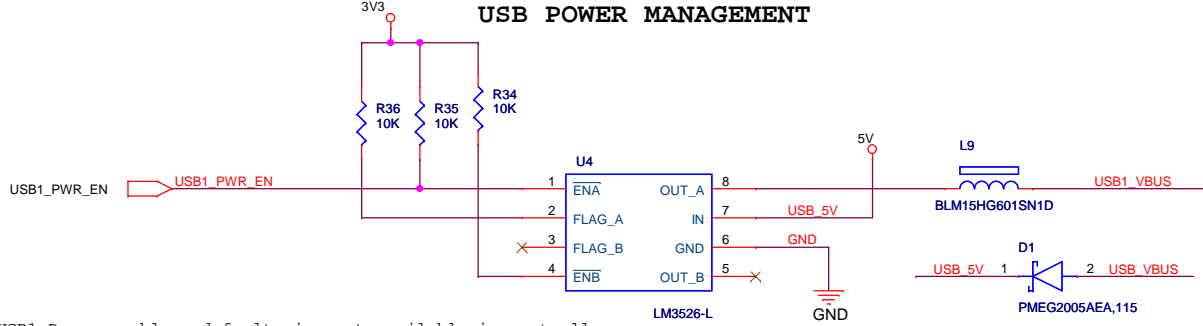
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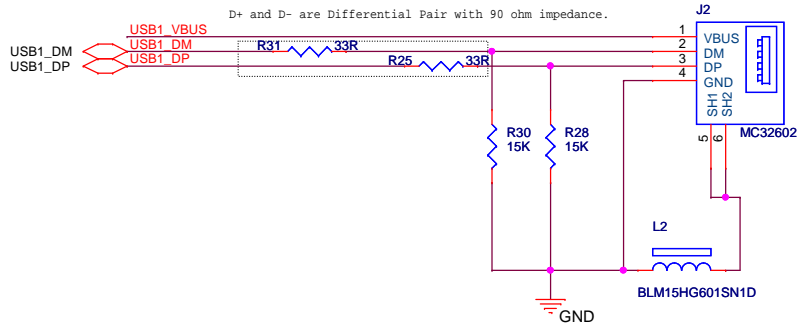
USB 1x HOST 1x DEVICE

USB POWER MANAGEMENT



USB1 Power enable and fault pins not available in controller and are monitored/controlled using GPIO.

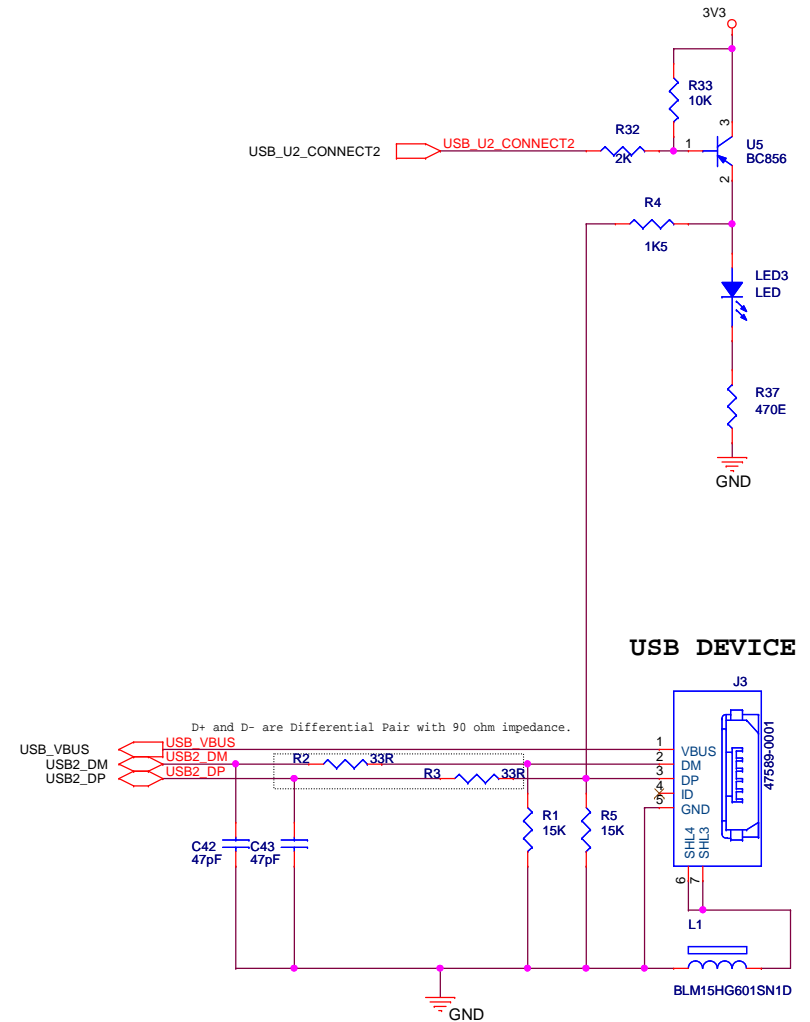
USB HOST



USB ROUTING GUIDELINES

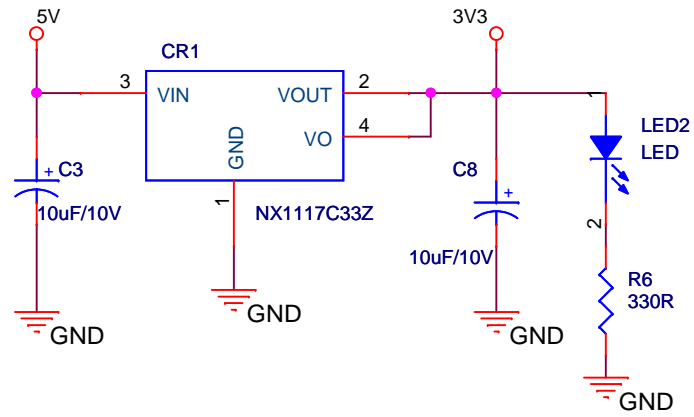
- =>Route USB trace pairs together [DM & DP].
- =>Do not route USB traces under crystals, oscillators, magnetic devices or ICs that use and/or duplicate clocks.
- =>Route high-speed USB signals using a minimum of vias and corners.
- =>Use 20-mil minimum spacing between high-speed USB signal pairs and other signal traces for optimal signal quality.

USB DEVICE



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POWER



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