CMOS 4-Bit Latch/4-to-16 Line Decoders

High-Voltage Types (20-Volt Rating)
CD4514B Output "High" on Select
CD4515B Output "Low" on Select

The RCA-CD4514B and -CD4515B consist of a 4-bit strobed latch and a 4-to-16-line decoder. The latches hold the last input data presented prior to the strobe transition from 1 to 0. Inhibit control allows all outputs to be placed at 0(CD4514B) or 1(CD4515B) regardless of the state of the data or strobe inputs.

The decode truth table indicates all combinations of data inputs and appropriate selected outputs.

These devices are similar to industry types MC14514 and MC14515.

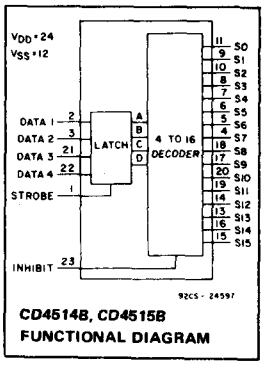
The CD4514B and CD4515B types are supplied in 24-lead hermetic dual-in-line ceramic packages (D and F suffixes), 24-lead dual-in-line plastic packages (E suffix), 24-lead ceramic flat packages (K suffix), and in chip form (H suffix).

Features:

- Strobed input latch
- Inhibit control
- 100% tested for quiescent current at 20 V
- Maximum input current of 1 μA at 18 V over full package-temperature range; 100 nA at 18 V and 25°C
- Noise margin (over full package temperature range):
  1 V at V_{DD} = 5 V
  2 V at V_{DD} = 10 V
  2.5 V at V_{DD} = 15 V
- 5-V, 10-V, and 15-V parametric ratings
- Standardized, symmetrical output characteristics.
- Meets all requirements of JEDEC Tentative Standard No. 13A, "Standard Specifications for Description of 'B' Series CMOS Devices"

Applications:

- Digital multiplexing
- Address decoding
- Hexadecimal/BCD decoding
- Program-counter decoding
- Control decoder



CD4514B, CD4515B FUNCTIONAL DIAGRAM

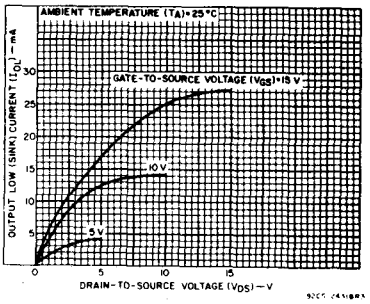


Fig. 1 — Typical output low (sink) current characteristics.

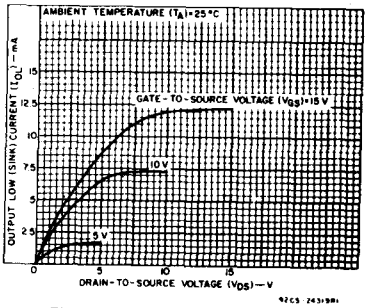


Fig. 2 — Minimum output low (sink) current characteristics.

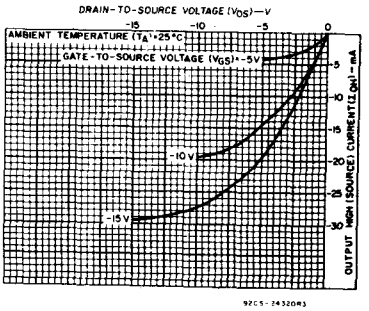


Fig. 3 — Typical output high (source) current characteristics.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD}) (Voltages referenced to V_{SS} Terminal)	−0.5 to +20 V
INPUT VOLTAGE RANGE, ALL INPUTS	−0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT	±10 mA
POWER DISSIPATION PER PACKAGE (P_D):	
For T_A = −40 to +60°C (PACKAGE TYPE E)	500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E)	Derate Linearly at 12 mW/°C to 200 mW
For T_A = −55 to +100°C (PACKAGE TYPES D, F, K)	500 mW
For T_A = +100 to +125°C (PACKAGE TYPES D, F, K)	Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types)	100 mW
OPERATING-TEMPERATURE RANGE (T_A):	
PACKAGE TYPES D, F, K, H	−55 to +125°C
PACKAGE TYPE E	−40 to +85°C
STORAGE TEMPERATURE RANGE (T_{stg})	−65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):	
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max.	+265°C

RECOMMENDED OPERATING CONDITIONS at T_A = 25°C, Except as Noted.
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	V_{DD} (V)	LIMITS Min.	LIMITS Max.	UNITS
Supply-Voltage Range (For T_A = Full Package-Temperature Range)		3	18	V
Data Setup Time, t_S	5	150	–	ns
	10	70	–	
	15	40	–	
Strobe Pulse Width, t_W	5	250	–	ns
	10	100	–	
	15	75	–	

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C) Values at -55, +25, +125 Apply to D, F, K, H Packages Values at -40, +25, +85 Apply to E Package							UNITS
								+25			
	V_O (V)	V_{IN} (V)	V_{DD} (V)	-55	-40	+85	+125	Min.	Typ.	Max.	
Quiescent Device Current, I_{DD} Max.	-	0,5	5	5	5	150	150	-	0.04	5	μA
	-	0,10	10	10	10	300	300	-	0.04	10	
	-	0,15	15	20	20	600	600	-	0.04	20	
	-	0,20	20	100	100	3000	3000	-	0.08	100	
Output Low (Sink) Current I_{OL} Min.	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1	-	mA
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	-	
	1.5	0,15	15	4.2	4	2.8	2.4	3.4	6.8	-	
Output High (Source) Current, I_{OH} Min.	4.6	0,5	5	-0.64	-0.61	-0.42	-0.36	-0.51	-1	-	
	2.5	0,5	5	-2	-1.8	-1.3	-1.15	-1.6	-3.2	-	
	9.5	0,10	10	-1.6	-1.5	-1.1	-0.9	-1.3	-2.6	-	
	13.5	0,15	15	-4.2	-4	-2.8	-2.4	-3.4	-6.8	-	
Output Voltage: Low-Level, V_{OL} Max.	-	0,5	5	0.05				-	0	0.05	V
	-	0,10	10	0.05				-	0	0.05	
	-	0,15	15	0.05				-	0	0.05	
Output Voltage: High-Level, V_{OH} Min.	-	0,5	5	4.95				4.95	5	-	
	-	0,10	10	9.95				9.95	10	-	
	-	0,15	15	14.95				14.95	15	-	
Input Low Voltage, V_{IL} Max.	0.5, 4.5	-	5	1.5				-	-	1.5	V
	1, 9	-	10	3				-	-	3	
	1.5,13.5	-	15	4				-	-	4	
Input High Voltage, V_{IH} Min.	0.5, 4.5	-	5	3.5				3.5	-	-	
	1, 9	-	10	7				7	-	-	
	1.5,13.5	-	15	11				11	-	-	
Input Current I_{IN} Max.	-	0,18	18	±0.1	±0.1	±1	±1	-	$\pm 10^{-5}$	±0.1	μA

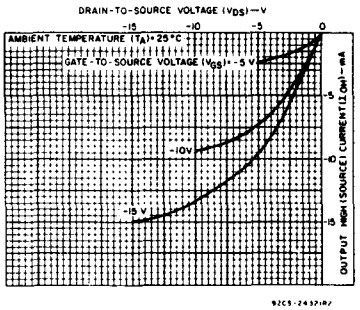


Fig. 4 — Minimum output high (source) current characteristics.

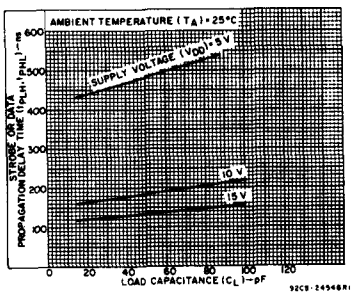


Fig. 5 — Typical strobe or data propagation delay time vs. load capacitance.

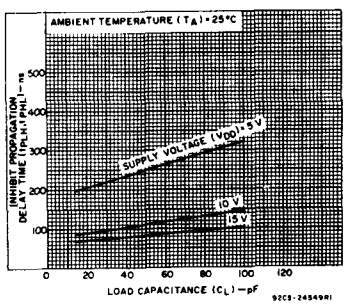


Fig. 6 — Typical inhibit propagation delay time vs. load capacitance.

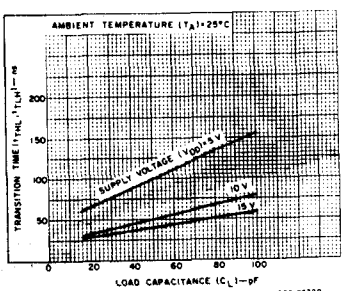


Fig. 7 — Typical low-to-high transition time vs. load capacitance.

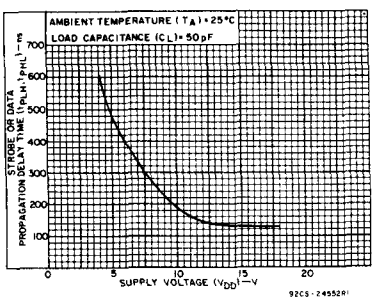


Fig. 8 — Typical strobe or data propagation delay time vs. supply voltage.

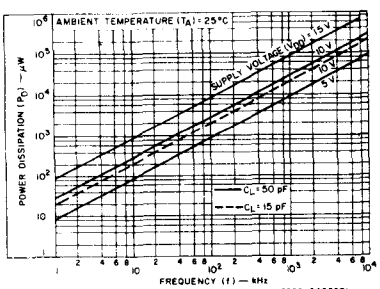


Fig. 9 — Typical power dissipation vs. frequency.

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C; Input t_r, t_f = 20 ns, C_L = 50 pF, R_L = 200 KΩ

CHARACTERISTIC	TEST CONDITIONS	LIMITS		UNITS
		V_{DD} V	Typ.	Max.	
Propagation Delay Time: t_{PHL}, t_{PLH} Strobe or Data		5	485	970	ns
		10	185	370	
		15	135	270	
Inhibit		5	250	500	
		10	110	220	
		15	85	170	
Transition Time, t_{TLH}, t_{THL}		5	100	200	
		10	50	100	
		15	40	80	
Minimum Strobe Pulse Width, t_W		5	125	250	ns
		10	50	100	
		15	40	75	
Minimum Data Setup Time, t_S		5	75	150	ns
		10	35	70	
		15	20	40	
Input Capacitance, C_{IN}	Any Input	–	5	7.5	pF

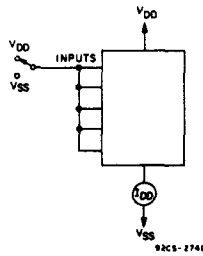


Fig. 10 – Quiescent device current test circuit.

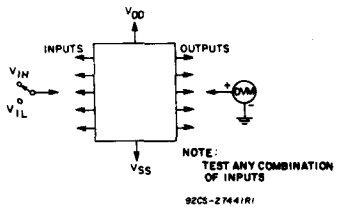


Fig. 11 – Input voltage test circuit.

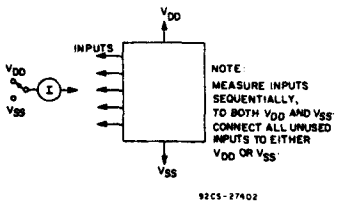


Fig. 12 – Input current test circuit.

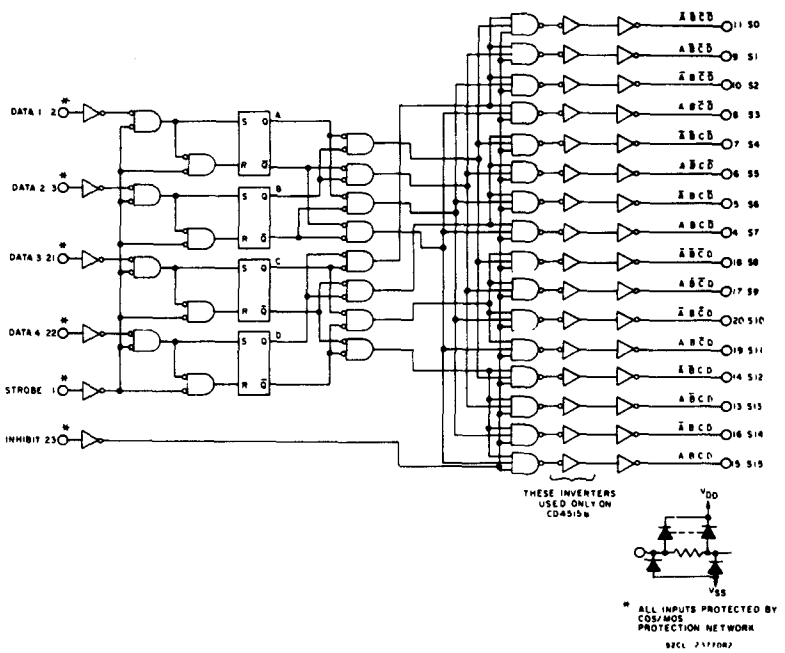


Fig. 13 – Logic diagram for CD4514B and CD4515B.

DECODE TRUTH TABLE (Strobe = 1)

INHIBIT	DECODER INPUTS				SELECTED OUTPUT CD4514B = Logic 1 (High) CD4515B = Logic 0 (Low)
	D	C	B	A	
0	0	0	0	0	S0
0	0	0	0	1	S1
0	0	0	1	0	S2
0	0	0	1	1	S3
0	0	1	0	0	S4
0	0	1	0	1	S5
0	0	1	1	0	S6
0	0	1	1	1	S7
0	1	0	0	0	S8
0	1	0	0	1	S9
0	1	0	1	0	S10
0	1	0	1	1	S11
0	1	1	0	0	S12
0	1	1	0	1	S13
0	1	1	1	0	S14
0	1	1	1	1	S15
1	X	X	X	X	All Outputs = 0, CD4514B All Outputs = 1, CD4515B

X = Don't Care Logic 1 = high Logic 0 = low

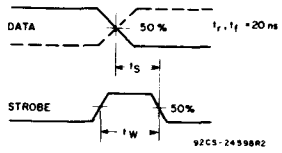
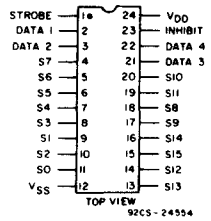
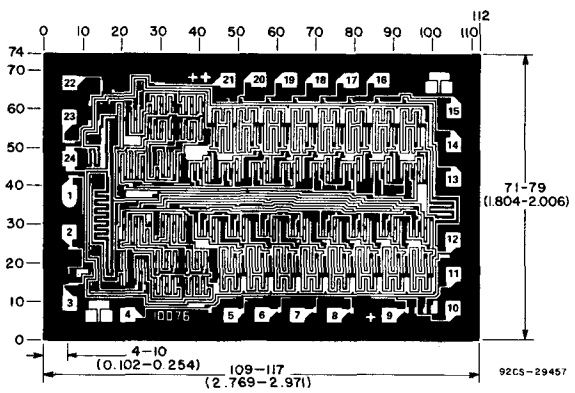


Fig. 14 — Waveforms for setup time and strobe pulse width.



CD4514B
CD4515B

TERMINAL ASSIGNMENT



Dimensions and Pad Layout for CD4515B Chip
(Dimensions and pad layout for the CD4514B are identical)

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

The photographs and dimensions of each CMOS chip represent a chip when it is part of the wafer. When the wafer is separated into individual chips, the angle of cleavage may vary with respect to the chip face for different chips. The actual dimensions of the isolated chip, therefore, may differ slightly from the nominal dimensions shown. The user should consider a tolerance of −3 mils to +16 mils applicable to the nominal dimensions shown.