FWS-2365

Desktop Network Appliance

User Manual 3rd Ed

Last Updated: April 7, 2022

Copyright Notice

Acknowledgement

Packing List

Before setting up your product, please make sure the following items have been shipped:

Item	Quantity
● FWS-2365	1
● Dual 2.5" HDD Bay	1
● SATA Cable	2
● SATA Power Cable	2
● Power Adapter	1
● System Rubber Foot	4

If any of these items are missing or damaged, please contact your distributor or sales representative immediately.

About this Document

This User's Manual contains all the essential information, such as detailed descriptions and explanations on the product's hardware and software features (if any), its specifications, dimensions, jumper/connector settings/definitions, and driver installation instructions (if any), to facilitate users in setting up their product.

Users may refer to the product page at AAEON.com for the latest version of this document.

Safety Precautions

Please read the following safety instructions carefully. It is advised that you keep this manual for future references

1. All cautions and warnings on the device should be noted.
2. All cables and adapters supplied by AAEON are certified and in accordance with the material safety laws and regulations of the country of sale. Do not use any cables or adapters not supplied by AAEON to prevent system malfunction or fires.
3. Make sure the power source matches the power rating of the device.
4. Position the power cord so that people cannot step on it. Do not place anything over the power cord.
5. Always completely disconnect the power before working on the system's hardware.
6. No connections should be made when the system is powered as a sudden rush of power may damage sensitive electronic components.
7. If the device is not to be used for a long time, disconnect it from the power supply to avoid damage by transient over-voltage.
8. Always disconnect this device from any AC supply before cleaning.
9. While cleaning, use a damp cloth instead of liquid or spray detergents.
10. Make sure the device is installed near a power outlet and is easily accessible.
11. Keep this device away from humidity.
12. Place the device on a solid surface during installation to prevent falls
13. Do not cover the openings on the device to ensure optimal heat dissipation.
14. Watch out for high temperatures when the system is running.
15. Do not touch the heat sink or heat spreader when the system is running
16. Never pour any liquid into the openings. This could cause fire or electric shock.

17. As most electronic components are sensitive to static electrical charge, be sure to ground yourself to prevent static charge when installing the internal components. Use a grounding wrist strap and contain all electronic components in any static-shielded containers.

18. If any of the following situations arises, please the contact our service personnel:

    i. Damaged power cord or plug

    ii. Liquid intrusion to the device

    iii. Exposure to moisture

    iv. Device is not working as expected or in a manner as described in this manual

    v. The device is dropped or damaged

    vi. Any obvious signs of damage displayed on the device

19. DO NOT LEAVE THIS DEVICE IN AN UNCONTROLLED ENVIRONMENT WITH TEMPERATURES BEYOND THE DEVICE'S PERMITTED STORAGE TEMPERATURES (SEE CHAPTER 1) TO PREVENT DAMAGE.

FCC Statement

This device complies with Part 15 FCC Rules. Operation is subject to the following two conditions: (1) this device may not cause harmful interference, and (2) this device must accept any interference received including interference that may cause undesired operation.

Caution:

There is a danger of explosion if the battery is incorrectly replaced. Replace only with the same or equivalent type recommended by the manufacturer. Dispose of used batteries according to the manufacturer's instructions and your local government's recycling or disposal directives.

Attention:

Il y a un risque d'explosion si la batterie est remplacée de façon incorrecte.
Ne la remplacer qu'avec le même modèle ou équivalent recommandé par le constructeur. Recycler les batteries usées en accord avec les instructions du fabricant et les directives gouvernementales de recyclage.

China RoHS Requirements (CN)

产品中有毒有害物质或元素名称及含量

AAEON System QO4-381 Rev.A0

部件名称	有毒有害物质或元素					
	铅 (Pb)	汞 (Hg)	镉 (Cd)	六价铬 (Cr(VI))	多溴联苯 (PBB)	多溴二苯醚(PBDE)
印刷电路板及其电子组件	×	○	○	○	○	○
外部信号连接器及线材	×	○	○	○	○	○
外壳	○	○	○	○	○	○
中央处理器与内存	×	○	○	○	○	○
硬盘	×	○	○	○	○	○
液晶模块	×	×	○	○	○	○
光驱	×	○	○	○	○	○
触控模块	×	○	○	○	○	○
电源	×	○	○	○	○	○
电池	×	○	○	○	○	○

本表格依据 SJ/T 11364 的规定编制。

○：表示该有毒有害物质在该部件所有均质材料中的含量均在GB/T 26572标准规定的限量要求以下。

×：表示该有害物质的某一均质材料超出了GB/T 26572的限量要求，然而该部件仍符合欧盟指令2011/65/EU 的规范。

备注:

一、此产品所标示之环保使用期限，系指在一般正常使用状况下。

二、上述部件物质中央处理器、内存、硬盘、光驱、电源为选购品。

三、上述部件物质液晶模块、触控模块仅一体机产品适用。

China RoHS Requirement (EN)

Hazardous and Toxic Materials List

AAEON System QO4-381 Rev.A0

Component Name	Hazardous or Toxic Materials or Elements					
	Lead (Pb)	Mercury (Hg)	Cadmium (Cd)	Hexavalent Chromium (Cr(VI))	Polybrominated biphenyls (PBBs)	Polybrominated diphenyl ethers (PBDEs)
PCB and Components	X	O	O	O	O	O
Wires & Connectors for Ext.Connections	X	O	O	O	O	O
Chassis	O	O	O	O	O	O
CPU & RAM	X	O	O	O	O	O
HDD Drive	X	O	O	O	O	O
LCD Module	X	X	O	O	O	O
Optical Drive	X	O	O	O	O	O
Touch Control Module	X	O	O	O	O	O
PSU	X	O	O	O	O	O
Battery	X	O	O	O	O	O

This form is prepared in compliance with the provisions of SJ/T 11364.

O: The level of toxic or hazardous materials present in this component and its parts is below the limit specified by GB/T 26572.

X: The level of toxic of hazardous materials present in the component exceed the limits specified by GB/T 26572, but is still in compliance with EU Directive 2011/65/EU (RoHS 2).

Notes:

1. The Environment Friendly Use Period indicated by labelling on this product is applicable only to use under normal conditions.
2. Individual components including the CPU, RAM/memory, HDD, optical drive, and PSU are optional.
3. LCD Module and Touch Control Module only applies to certain products which feature these components.

Table of Contents

Chapter 1

Product Specifications

1.1 Specifications

System	
Form Factor	Desktop
Processor	Intel® Atom™ Processor C3000 series (4~16 cores)
Chipset	SoC
System Memory	DDR4 SODIMM ECC x 2, up to 64GB

Network	
Ethernet	1GbE RJ-45 x 6 (2 ports co-lay SFP) 10G SFP+ x 4 (4 core processors only support 2 SFP ports)
Bypass	Supports 1 pair on LAN Ports 3-4

Display	
Graphics Controller	—
Connector	—

Storage	
HDD	SATA III port x 2, 2.5" HDD/SSD up to 2
CF/CFAST/mSATA	On board 16GB eMMC, up to 128GB Optional mSATA slot x 1 (co-lay with M.2 slot)

Internal/Expansion Interface

PCIe Slot	—
Expansion slot	Half-sized Mini-card slot x 1 (PCIe)
	Full-sized Mini-card slot x 1 (PCIe + USB2.0) with SIM slot
	M.2 B key 3052 x 1 (USB3.0) with SIM slot
KB/Mouse	Reserved pin header
USB	USB 3.0 x 2 (1 Port only supports USB2.0 signal)

Miscellaneous

RTC	Internal RTC
Watchdog Timer	1~255 steps by software programmable
Software Button	GPIO programmable push button x 1
TPM	TPM v2.0 9665
GPIO	4 bits input/ 4 bits output
Fan	System Fan x 1
MTBF (HOURS)	TBD
Color	Black

Physical & Environmental

Power Requirement	12V DC Power in connector
	4 Core Processors: 40W Power Adapter
	8 Cores and above: 60W Power Adapter
Operating Temperature	32°F ~ 104°F (0°C ~ 40°C)
Storage Temperature	-4°F ~ 140°F (-20°C ~ 60°C)
Operating Humidity	10%~80% relative humidity, non-condensing
Storage Humidity	10%~80% @40°C; non-condensing

Physical & Environmental

Vibration	0.5 g rms/ 5 ~ 500Hz / operation (2.5" HDD)
	1.5 g rms/ 5 ~ 500Hz / non-operation
Shock	10 G peak acceleration (11 m sec. duration), operation
	20 G peak acceleration (11 m sec. duration), non-operation
Dimension (W x D x H)	260mm x 178mm x 44mm

I/O

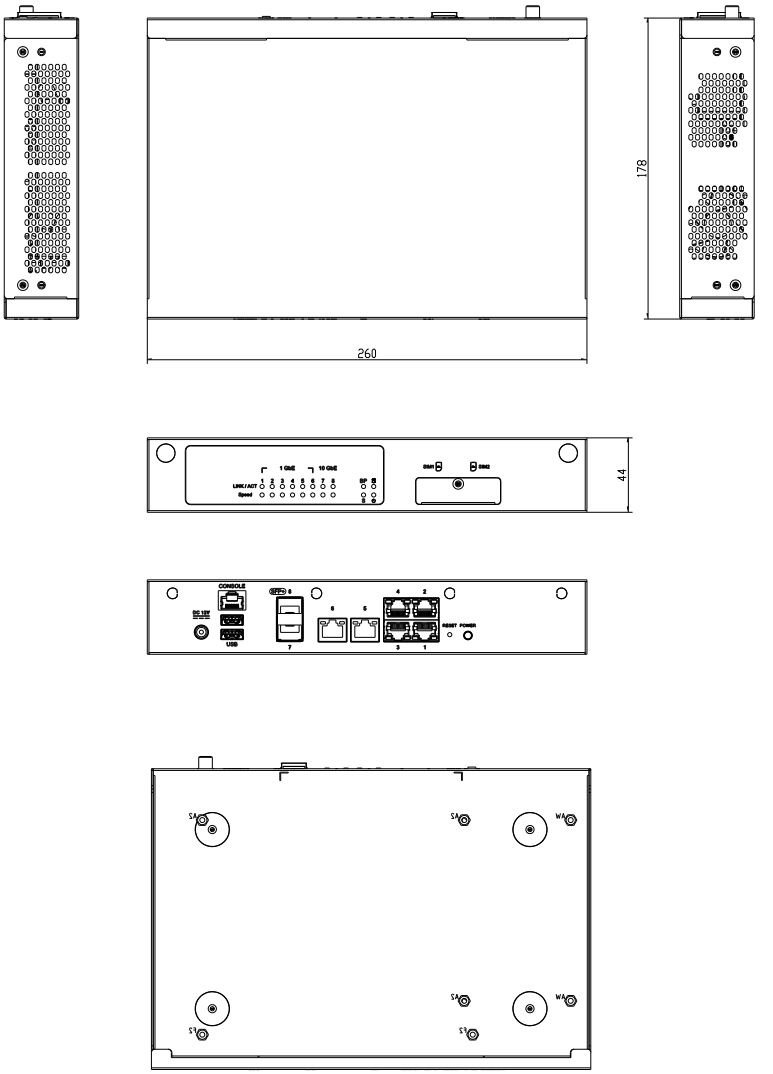
Front Panel	Power LED x 1
	Status LED x 1
	Storage Active LED x 1
	Bypass LED x 1
	Ethernet LED x 20
	Antenna Hole x 2
	Accessible SIM slot x 2
Rear Panel	USB 3.0 Port x 2
	RJ-45 Port x 6
	SFP+ Port x 2
	RJ-45 Console x 1
	12V DC Power Input x 1
	Software Reset Button x 1
	Power Button x 1
	Antenna Hole x 4

Chapter 2

Hardware Information

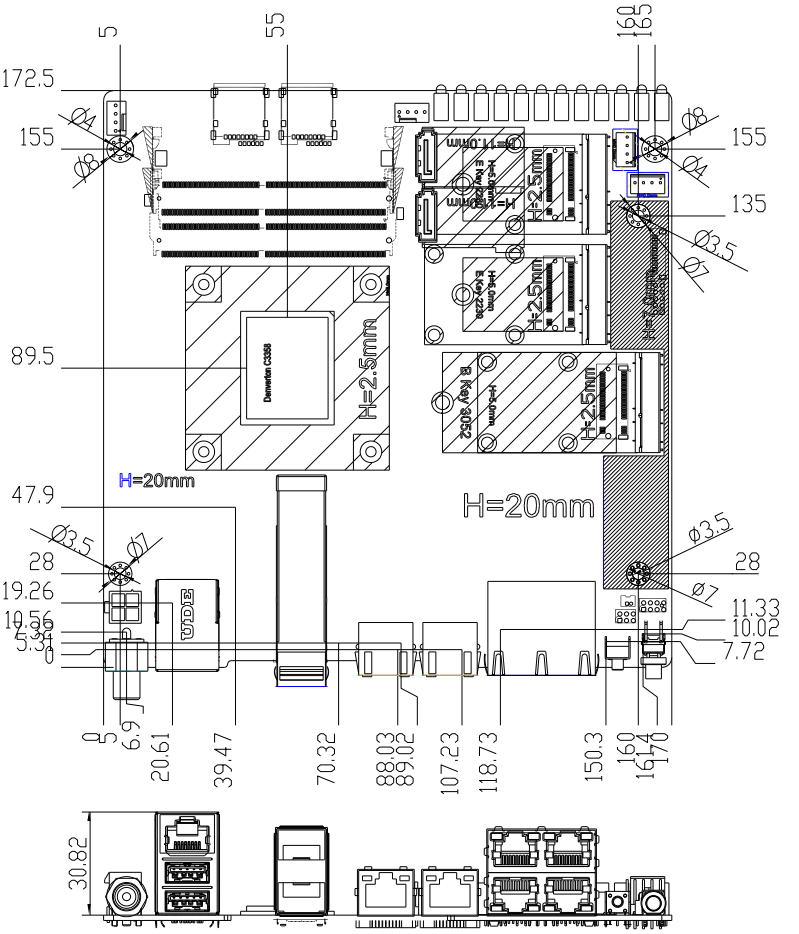
2.1 Dimensions

System

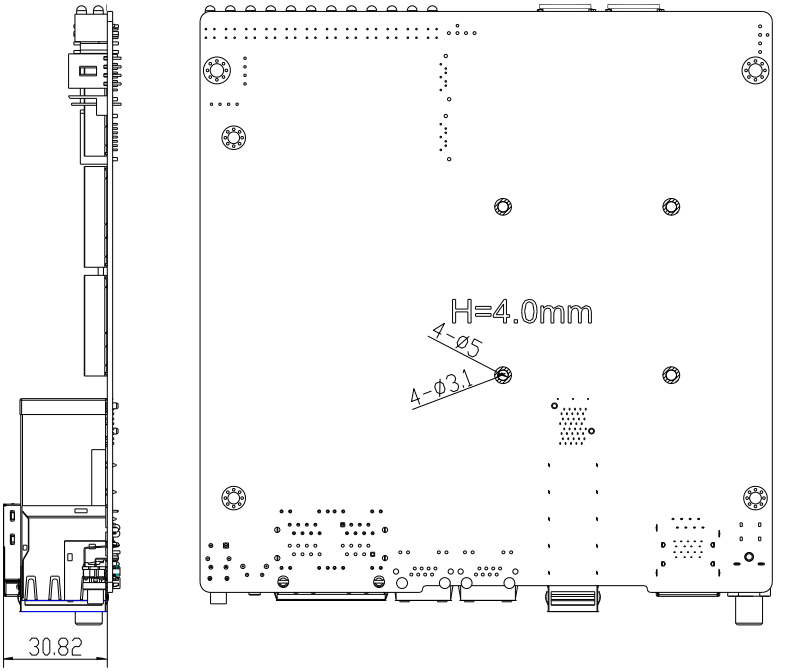


Board

Top and I/O View

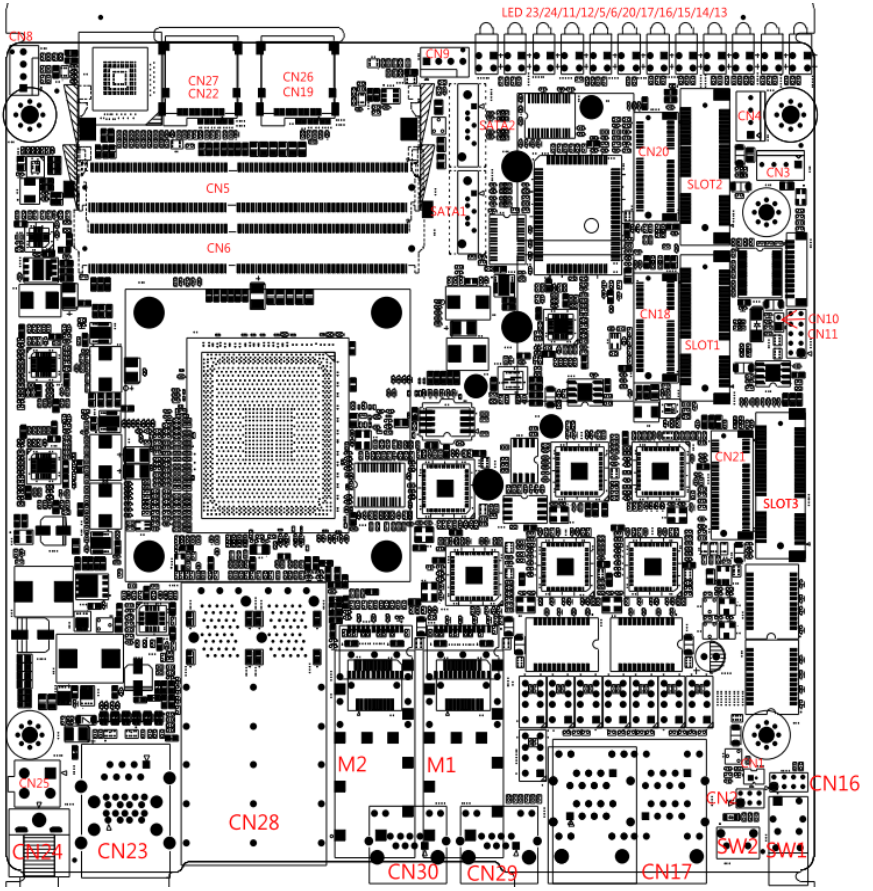


Bottom and Side View



2.2 Jumpers and Connectors

Top and I/O View



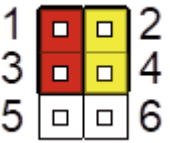
Note: Components and their locations may vary depending upon which configuration was purchased. If you have questions about your FWS-2365, visit our website to contact an AAEON support representative.

2.3 List of Jumpers

Please refer to the table below for all of the board's jumpers that you can configure for your application

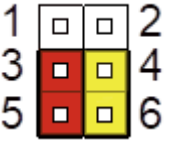
Label	Function
CN2	Clear CMOS

2.3.1 Clear CMOS (CN2)



Pins 1-3 and 2-4 Selected

Normal, Default



Pins 3-5 and 4-6 Selected

Clear CMOS

Note: To prevent damage to the system or unwanted operation, do not connect jumpers in any other configuration than the ones shown in the diagram.

2.4 List of Connectors

Please refer to the table below for all of the board's connectors that you can configure for your application. (Optional) denotes a component that is not included on the standard configuration. Some optional components may replace standard components. Contact AAEON support if you have any questions about the configuration of your FWS-2365 system.

Label	Function
CN1	Battery Header
CN3	SATA Power Connector
CN4	SATA Power Connector
CN5	DDR4 SODIMM Slot
CN6	DDR4 SODIMM Slot
CN8	FAN1 Connector
CN9	FAN2 Connector
CN10	Case Open Header
CN11	Digital IO Header
CN16	Front Panel Header
CN17	LAN1~4 RJ45 Connector
CN18	M.2 E-Key (USB2.0+PCIE) (Optional)
CN19	Micro-SIM Card Slot
CN20	M.2 E-Key (PCIe only) (Optional)
CN21	M.2 B-Key 3052 (USB3.0/2.0 + SATA)
CN22	Micro-SIM Card Slot
CN23	Dual USB3.2 Gen 1 + Console Port
CN24	DC Power In
CN25	DC Power In
CN26	Micro-SIM Card Slot (Optional)
CN27	Micro-SIM Card Slot (Optional)

Label	Function
CN28	10 Gbps SPF+ Connector LAN 2 Port Connector (4 Port Optional)
CN29	LAN5 RJ45 Connector
CN30	LAN6 RJ45 Connector
LED5	LAN8 LED Indicator
LED6	LAN7 LED Indicator
LED11	LAN10 LED Indicator
LED12	LAN9 LED Indicator
LED13	LAN1 LED Indicator
LED14	LAN2 LED Indicator
LED15	LAN3 LED Indicator
LED16	LAN4 LED Indicator
LED17	LAN5 LED Indicator
LED20	LAN6 LED Indicator
LED23	Power + HDD LED Indicator
LED24	Status + Bypass LED Indicator
M1	LAN5 SFP Connector (optional)
M2	LAN6 SFP Connector (optional)
SATA1	SATA Connector
SATA2	SATA Connector
SLOT1	mPCIe Full-Sized Mini-Card (PCIE+USB2.0)
SLOT2	mPCIe Half-Sized Mini-Card (PCIe only)
SLOT3	mPCIe Full-Sized Mini-Card (USB2.0 + SATA) (Optional)
SW1	Power Button
SW2	Software Reset

2.4.1 System Configuration Notes

Expansion Card Slots

Standard expansion slot configuration is CN21, SLOT1 and SLOT2.

Optional expansion slots replace standard configuration per diagram in Chapter 2.2.

M1, M2 SFP Connectors (Optional)

Optional M1 and M2 SFP LAN Ports replace CN29, CN30 RJ45 LAN Ports in system configuration.

CN26, CN27 Micro-SIM Card Slots (Optional)

CN26 connects to CN18/SLOT1; CN27 connects to CN21/SLOT3; depending on your system's configuration.

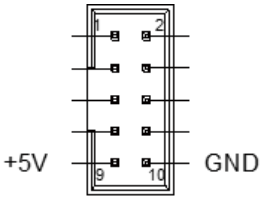
2.4.2 Battery Header (CN1)

Pin	Signal	Pin	Signal
1	+3.3V	2	GND

2.4.3 Case Open Pin Header (CN10)

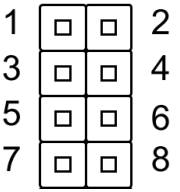
Pin	Signal	Pin	Signal
1	Case Open	2	GND

2.4.4 Digital IO Header (CN11)



Pin	Signal	Pin	Signal
1	Digital I/O bit1	2	Digital I/O bit2
3	Digital I/O bit3	4	Digital I/O bit4
5	Digital I/O bit5	6	Digital I/O bit6
7	Digital I/O bit7	8	Digital I/O bit8
9	+5V	10	GND

2.4.5 Front Panel Header (CN16)



Pin	Signal	Pin	Signal
1	Power Button SW+	2	Ground
3	Hardware Reset SW+	4	Ground
5	Power LED+	6	Power LED-
7	HDD LED+	8	HDD LED-

2.4.6 DC Power In (CN25)

Pin	Signal	Pin	Signal
1	GND	2	GND
3	+12V	4	+12V

2.5 Hardware Assembly

2.5.1 Opening the System

Before performing any hardware installation, make sure the system is powered down and not in sleep or suspended mode. Disconnect the power cable or connector and ensure there is no power to the system.

Step 1: Remove the four screws (two on each side) securing the top panel. Please note the placement of the screws for later reassembly.

Step 2: Remove the top panel by first sliding it slightly, then lifting.

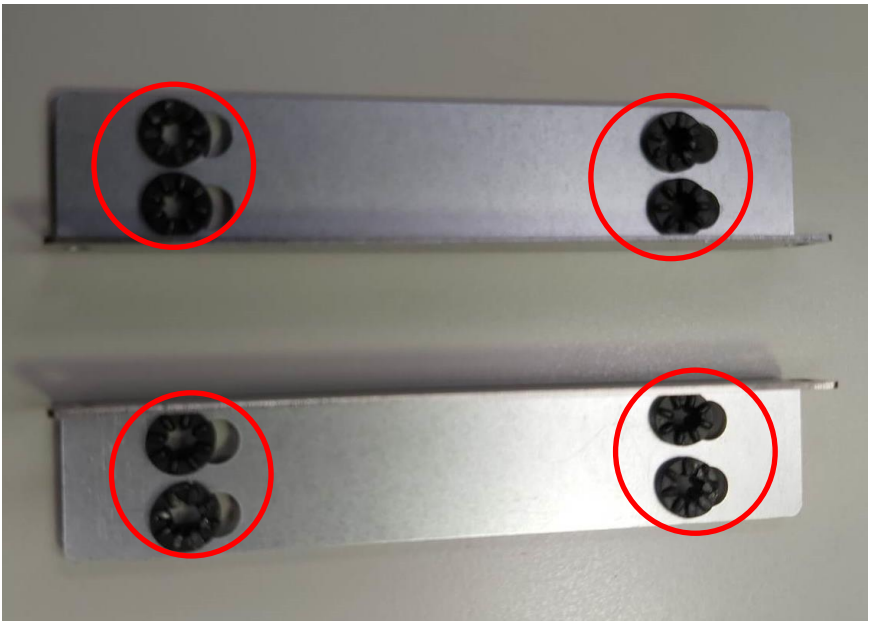
Follow these steps in reverse to secure the top panel when finished with hardware installation. Ensure the top panel is secure and the screws are fastened snugly.

2.5.2 Installing the Dual 2.5″ Drive Assembly

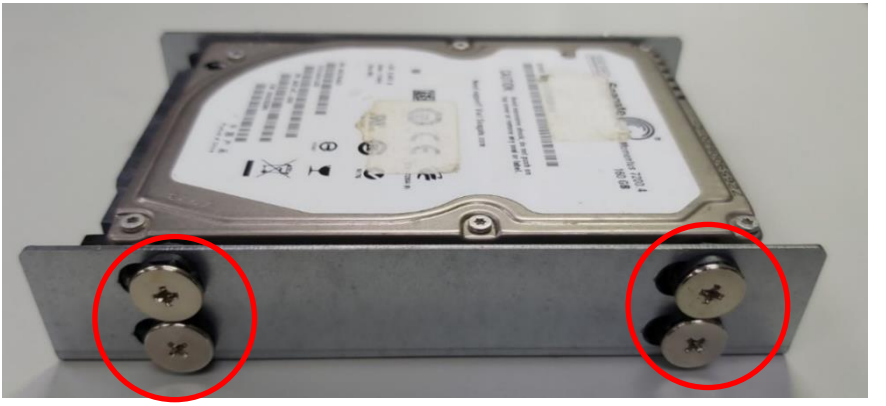
Before beginning, ensure you have the following ready: two (2) dual 2.5″ drive mounting brackets (L-bracket), eight (8) mounting cushions, eight (8) mounting screws, two (2) 2.5″ SATA drives (HDD or SSD).

Step 1: Follow the directions in the previous section for accessing the system.

Step 2: Install the mounting cushions into the mounting holes as shown:

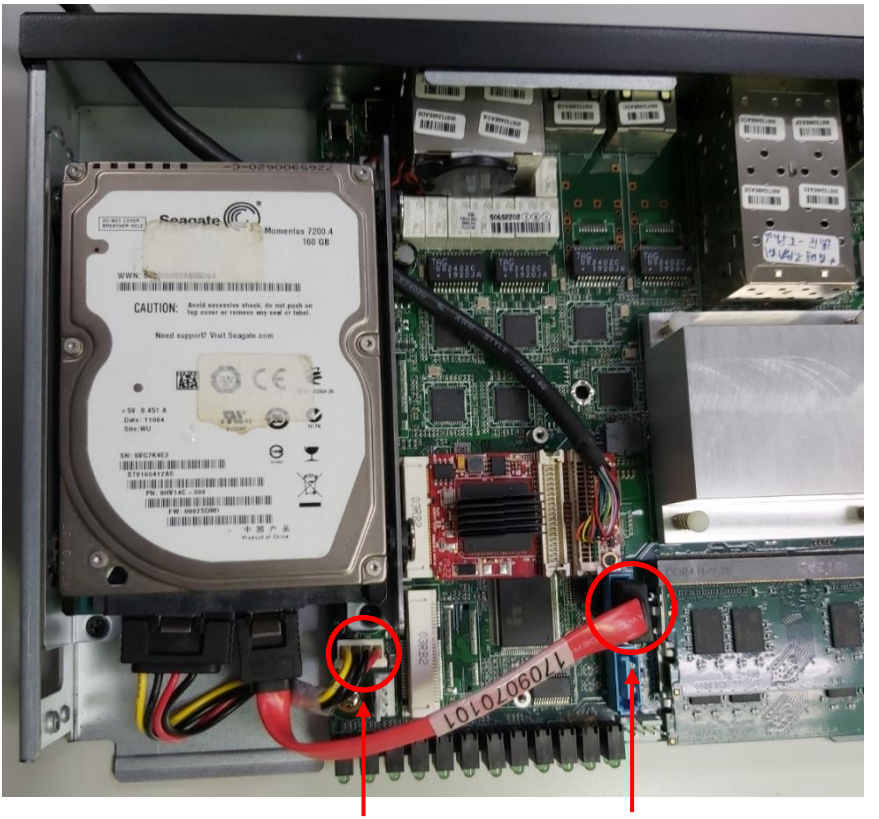


Step 3: Mount the two 2.5" drives to the mounting bracket. Not the direction, the flange on the mounting brackets will go under the drive assembly, and the drives should be mounted label side up.

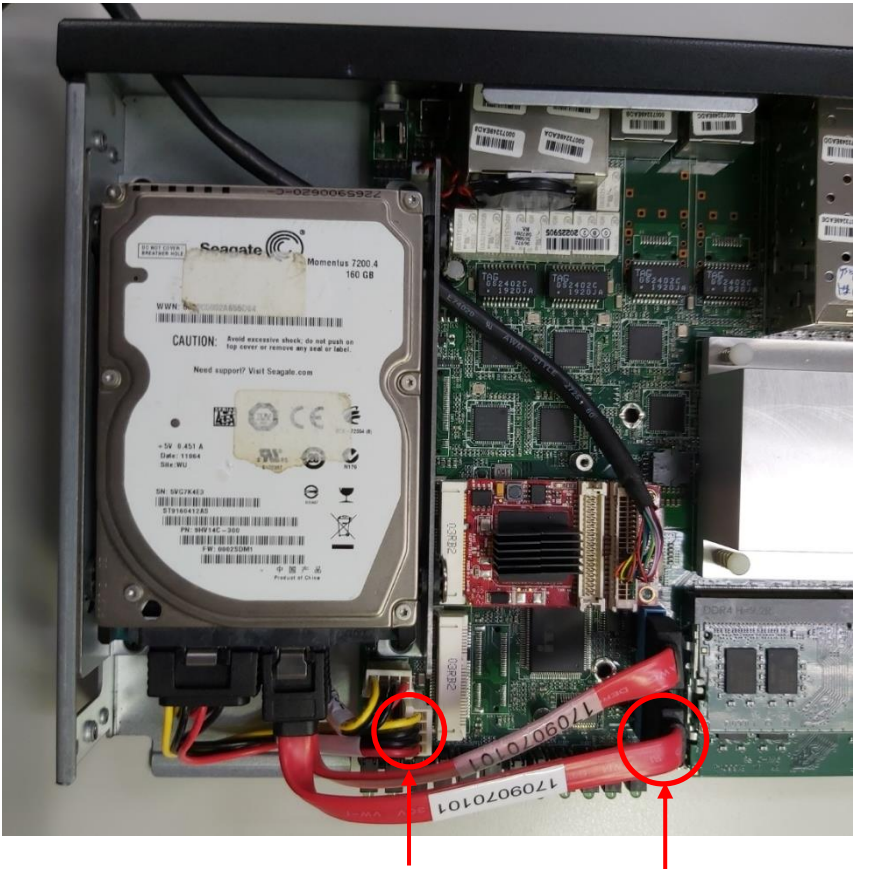


Step 4: Mount the drive assembly into the system. Secure with four screws mounted through the flange as shown. Please not the direction of the drives to ensure access to the SATA connectors.

Step 5: Connect the bottom drive to the SATA1 connector and CN3 SATA Power Connector on the board (See Chapter 2.2 for reference).



Step 6: Repeat for the top drive, connecting to CN4 SATA Power connector and SATA2 Connector on the board.



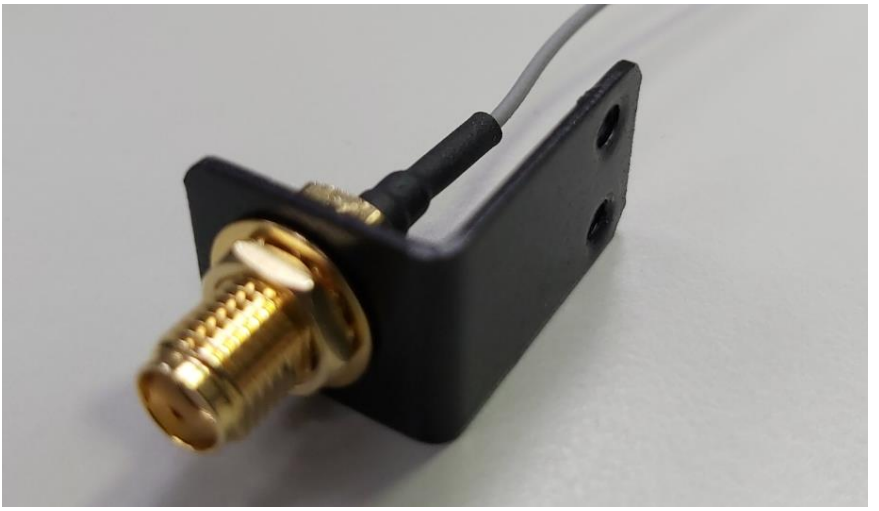
Drive installation is complete. Reassemble the system following instructions in Chapter 2.5.1 or continue to the next section for Antenna Mount Assembly.

2.5.3 Antenna Mount Assembly

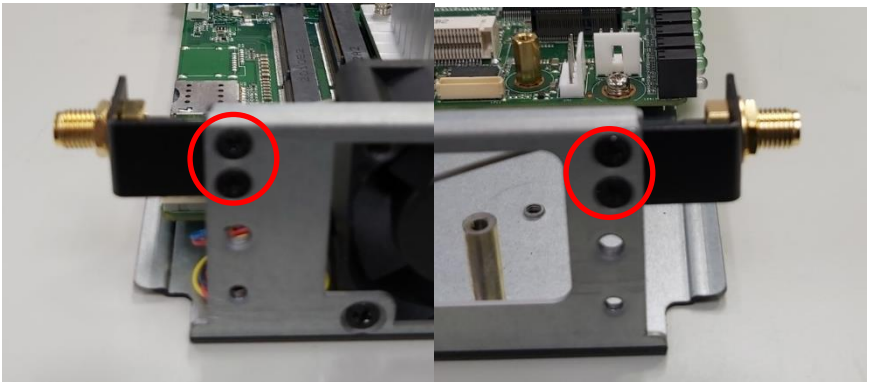
Before beginning, ensure you have the following ready: two (2) antenna screw mounts with securing washer and nut, two (2) antenna mounting brackets, four (4) mounting screws.

Step 1: Follow the directions in Chapter 2.5.1 for accessing the system.

Step 2: Assemble the antenna mounts by placing the screw mounts into the mounting brackets and securing with washer and nut.



Step 3: Mount the antennas to either side of the system chassis and secure with two screws each.



Chapter 3

AMI BIOS Setup

3.1 System Test and Initialization

The system uses certain routines to perform testing and initialization during the boot up sequence. If an error, fatal or non-fatal, is encountered, the system will output a few short beeps or display an error message. The system can usually continue the boot up sequence with non-fatal errors.

The system configuration verification routines check the current system configuration against the values stored in the CMOS memory and BIOS NVRAM. If a system configuration is not found or an error is detected, the system will load the default configuration and reboot automatically.

There are four situations in which you will need to setup system configuration:

1. You are starting your system for the first time
2. You have changed the hardware attached to your system
3. The system configuration was reset by the Clear-CMOS jumper
4. The CMOS memory has lost power and the configuration information has been erased.

The system CMOS memory has an integral lithium battery backup for data retention. However, you will need to replace the battery unit when it runs down.

3.2 AMI BIOS Setup

The AMI BIOS ROM has a pre-installed Setup program that allows users to modify basic system configurations, which is stored in the battery-backed CMOS RAM and BIOS NVRAM so that the information is retained when the power is turned off.

To enter BIOS Setup, press <Del> or <Esc> immediately while your computer is powering up.

The function for each interface can be found below.

Main – Date and time can be set here. Press <Tab> to switch between date elements

Advanced – Access hardware monitor and advanced board features and options

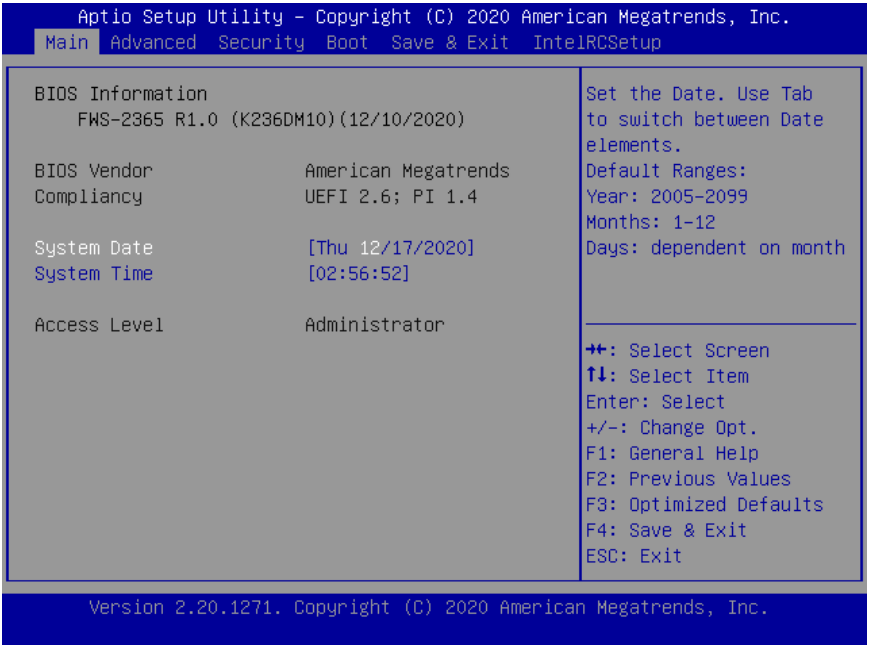
Security – The setup administrator password can be set here

Boot – Set boot drive priority and quiet boot options

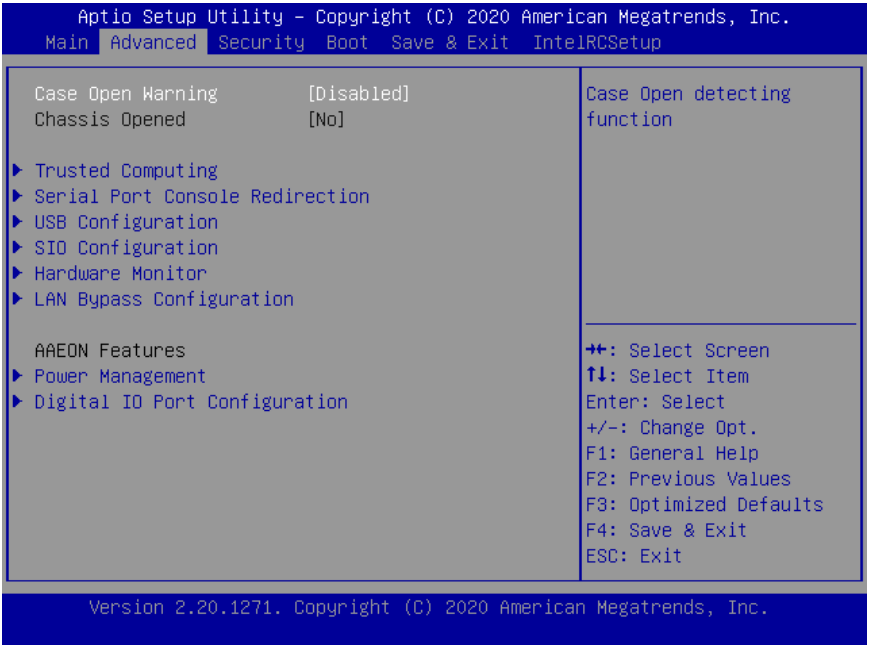
Save & Exit – Save changes and exit the program

IntelRCSetup – Access Intel RC Setup options

3.3 Setup Submenu: Main

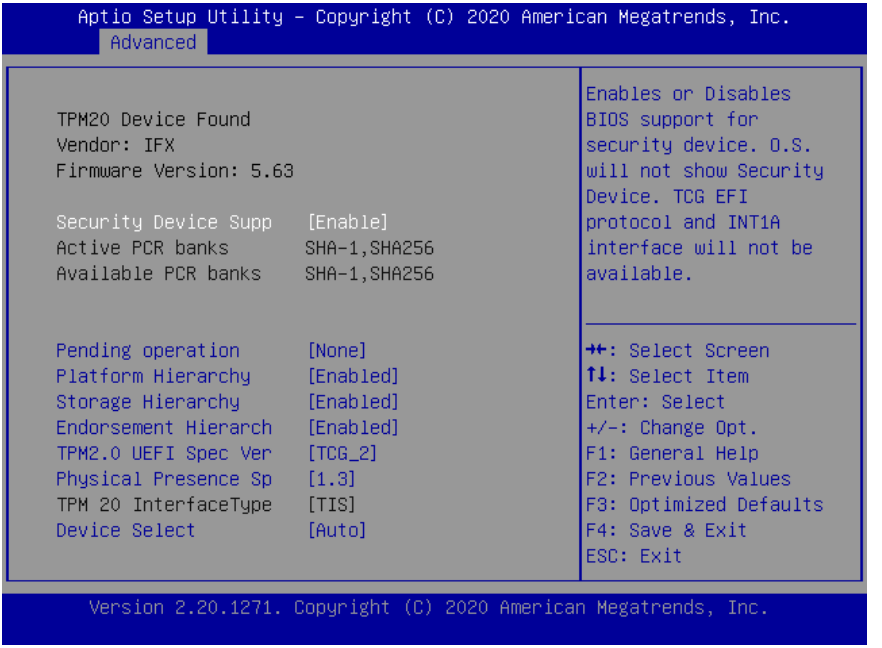


3.4 Setup Submenu: Advanced



Options Summary		
Case Open Warning	Disabled	Optimal Default, Failsafe Default
	Enabled	
	Clear	
Case Open detecting function		

3.4.1 Trusted Computing

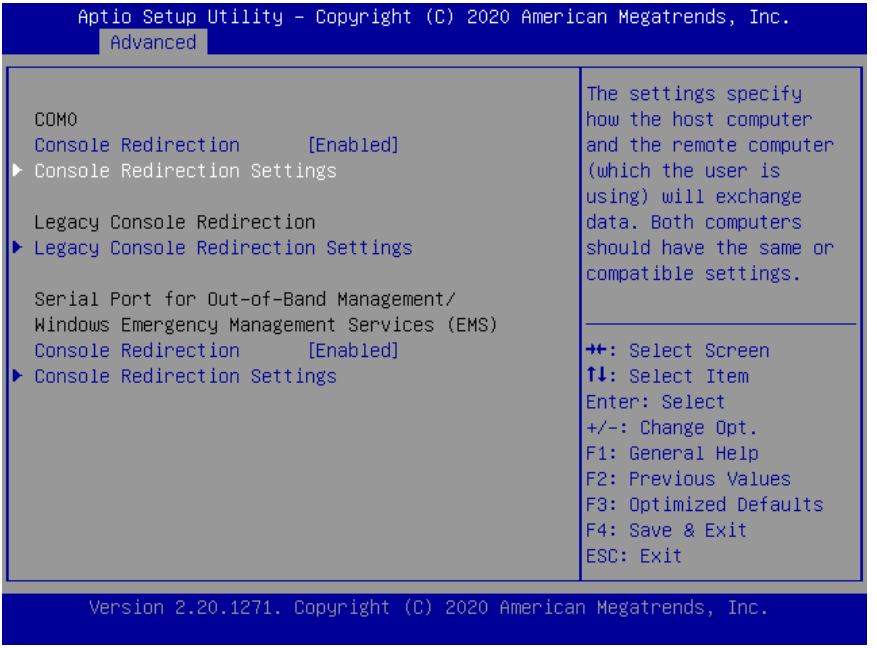


Options Summary		
Security Device Supp	Disable	
	Enable	Optimal Default, Failsafe Default
Enables or Disables BIOS support for security device. O.S. will not show Security Device. TCG EFI protocol and INT1A interface will not be available.		
Pending operation	None	Optimal Default, Failsafe Default
	TPM Clear	
Schedule an Operation for the Security Device. NOTE: Your Computer will reboot during restart in order to change state of Security Device.		
Platform Hierarchy	Disable	
	Enable	Optimal Default, Failsafe Default
Enable or Disable Platform Hierarchy		
Storage Hierarchy	Disable	
	Enable	Optimal Default, Failsafe Default
Enable or Disable Storage Hierarchy		

Table Continues on Next Page...

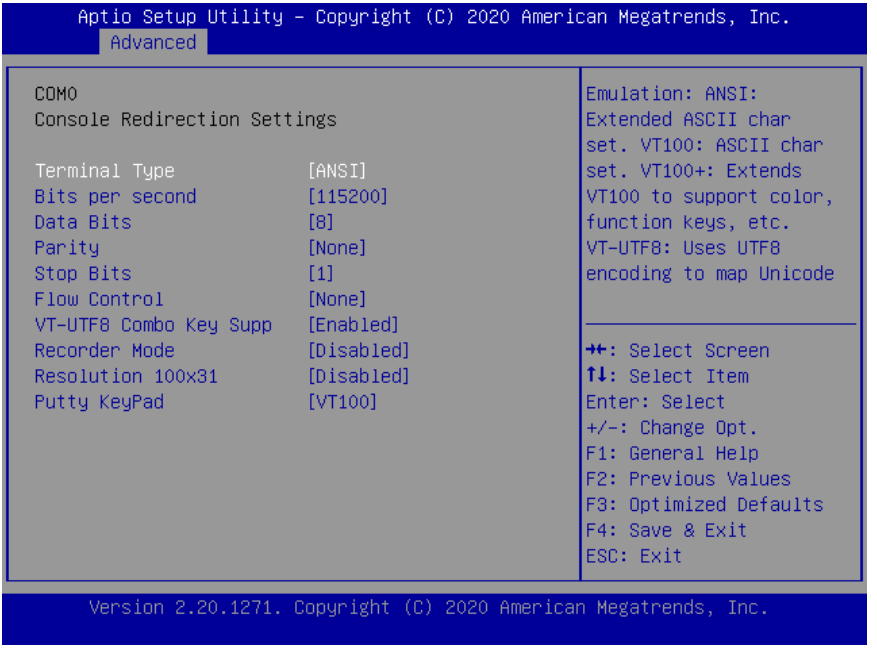
Options Summary		
Endorsement Hierarchy	Disable	
	Enable	Optimal Default, Failsafe Default
Enable or Disable Endorsement Hierarchy		
TPM2.0 UEFI Spec Version	TCG_1_2	
	TCG_2	Optimal Default, Failsafe Default
Select the TCG2 Spec Version Support, TCG_1_2: The Compatible mode for Win8/Win10 TCG_2: Support new TCG2 protocol and event		
Physical Presence Spec Version	1.2	
	1.3	Optimal Default, Failsafe Default
Select to Tell O.S. to support PPI Spec Version 1.2 or 1.3. Note some HCK tests might not support 1.3.		
Device Select	TPM 1.2	
	TPM 2.0	
	Auto	Optimal Default, Failsafe Default
TPM 1.2 will restrict support to TPM 1.2 device, TPM 2.0 will restrict support to TPM 2.0 devices, Auto will support both with the default set to TPM 2.0 devices if not found, TPM 1.2 device will be enumerated.		

3.4.2 Serial Port Console Redirection



Options Summary		
COM0 Console Redirection	Disabled	
	Enabled	Optimal Default, Failsafe Default
Console Redirection Enable or Disable		
EMS Console Redirection	Disabled	
	Enabled	Optimal Default, Failsafe Default
Console Redirection Enable or Disable		

3.4.2.1 COM0 Console Redirection

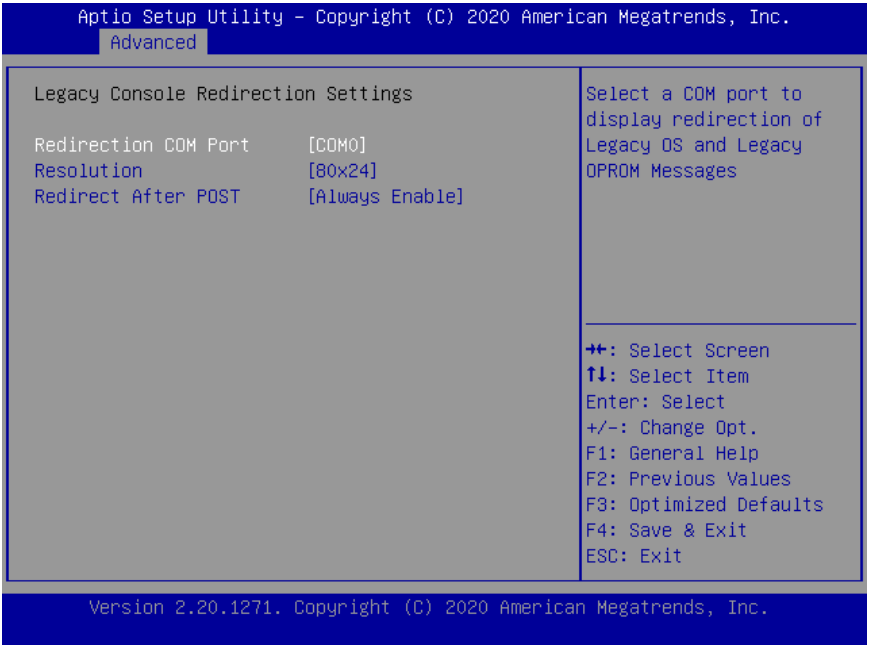


Options Summary		
Terminal Type	VT100	
	VY100+	
	VT-UTF8	
	ANSI	Optimal Default, Failsafe Default
Emulation: ANSI: Extended ASCII char set. VT100: ASCII char set. VT100+: Extends VT100 to support color, function keys, etc. VT-UTF8: Uses UTF8 encoding to map Unicode.		
Bits per second	9600	
	19200	
	38400	
	57600	
	115200	Optimal Default, Failsafe Default
Selects serial port transmission speed. The speed must be matched on the other side. Long or noisy lines may require lower speeds.		

Table Continues on Next Page...

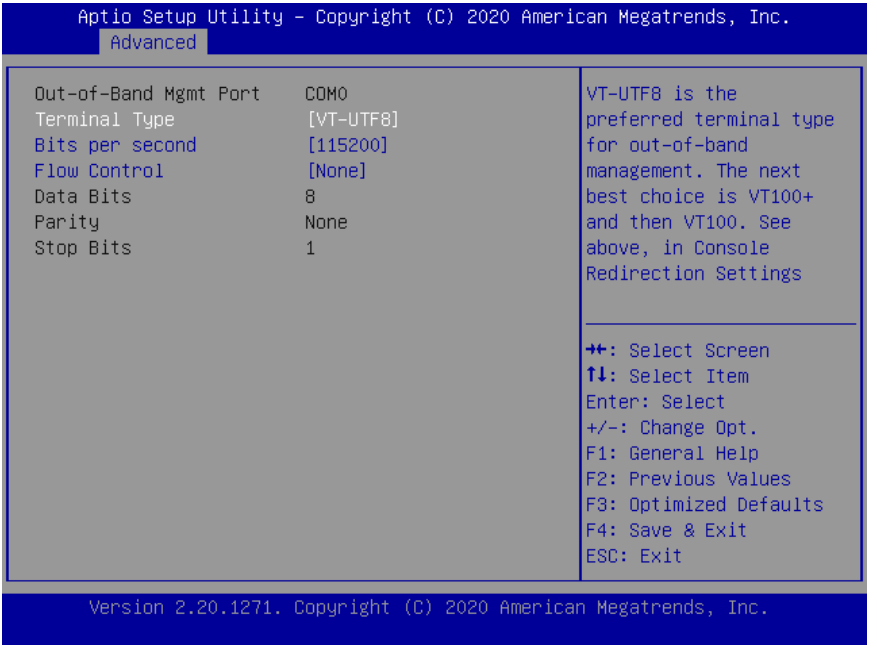
Options Summary		
Data bit	7	
	8	Optimal Default, Failsafe Default
Data Bits		
Parity	None	Optimal Default, Failsafe Default
	Even	
	Odd	
	Mark	
	Space	
A Parity bit can be sent with the data bits to detect some transmission errors. Even: parity bit is 0 if the num of 1's in the data bits is even. Odd: parity bit is 0 if the num of 1's in the data bits is odd.		
Stop Bits	1	Optimal Default, Failsafe Default
	2	
Stop bits indicate the end of a serial data packet. (A start bit indicates the beginning). The standard setting is 1 stop bit. Communication with slow devices may require more than 1 stop bit.		
Flow control	None	Optimal Default, Failsafe Default
	Hardware RTS/CTS	
Flow control can prevent data loss from buffer overflow. When sending data, if the receiving buffers are full, a 'stop' signal can be sent to stop the data flow. Once the buffers are empty, a 'start' signal can be sent to re-start the flow. Hardware flow control uses two wires to send start/stop signals.		
VT-UTF8 Combo Key Support	Enabled	Optimal Default, Failsafe Default
	Disabled	
Enable VT-UTF8 Combination Key Support for ANSI/VT100 terminals.		
Recorder Mode	Disabled	Optimal Default, Failsafe Default
	Enabled	
With this mode enabled only text will be sent. This is to capture Terminal data.		
Resolution 100x31	Disabled	Optimal Default, Failsafe Default
	Enabled	
Enables or disables extended terminal resolution.		
Putty KeyPad	VT100	Optimal Default, Failsafe Default
	LINUX	
	XTERMR6	
	SCO	
	ESCN	
	VT400	
Select FunctionKey and KeyPad on Putty.		

3.4.2.2 Legacy Console Redirection Settings



Options Summary		
Redirection COM Port	COM0	Optimal Default, Failsafe Default
Select a COM port to display redirection of Legacy OS and Legacy OPROM Messages.		
Resolution	80x24	Optimal Default, Failsafe Default
	80x25	
On Legacy OS, the Number of Rows and Columns supported redirection.		
Redirection After POST	Always Enable	Optimal Default, Failsafe Default
	BootLoader	
When BootLoader is selected, then Legacy Console Redirection is disabled before booting to legacy OS. When Always Enable is selected, then Legacy Console Redirection is enabled for legacy OS. Default setting for this option is set to Always Enable.		

3.4.2.3 Out of Band Management Port/Windows EMS

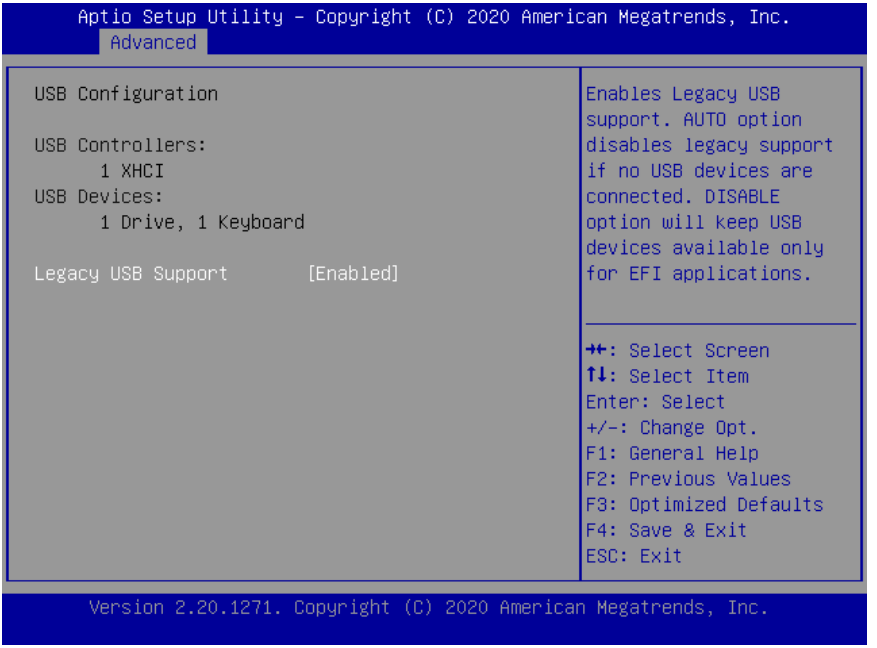


Options Summary		
Terminal Type	VT100	
	VY100+	
	VT-UTF8	Optimal Default, Failsafe Default
	ANSI	
VT-UTF8 is the preferred terminal type for out-of-band management. The next best choice is VT100+ and then VT100. See above, in Console Redirection Settings page, for more Help with Terminal Type/Emulation.		
Bits per second	9600	
	19200	
	57600	
	115200	Optimal Default, Failsafe Default
Selects serial port transmission speed. The speed must be matched on the other side. Long or noisy lines may require lower speeds.		

Table Continues on Next Page...

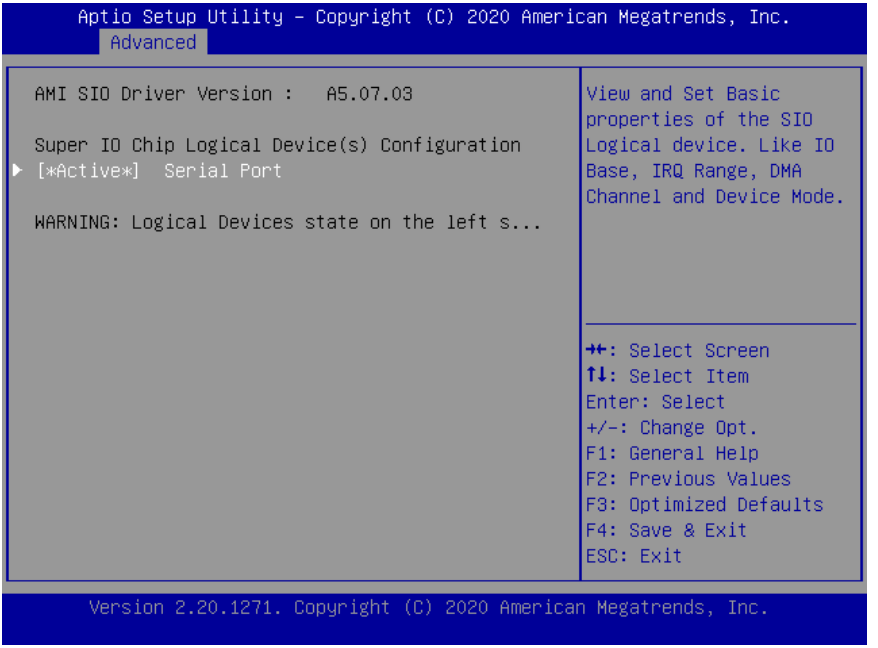
Options Summary		
Flow control	None	Optimal Default, Failsafe Default
	Hardware RTS/CTS	
	Software Xon/Xoff	
Flow control can prevent data loss from buffer overflow. When sending data, if the receiving buffers are full, a 'stop' signal can be sent to stop the data flow. Once the buffers are empty, a 'start' signal can be sent to re-start the flow. Hardware flow control uses two wires to send start/stop signals.		

3.4.3 USB Configuration

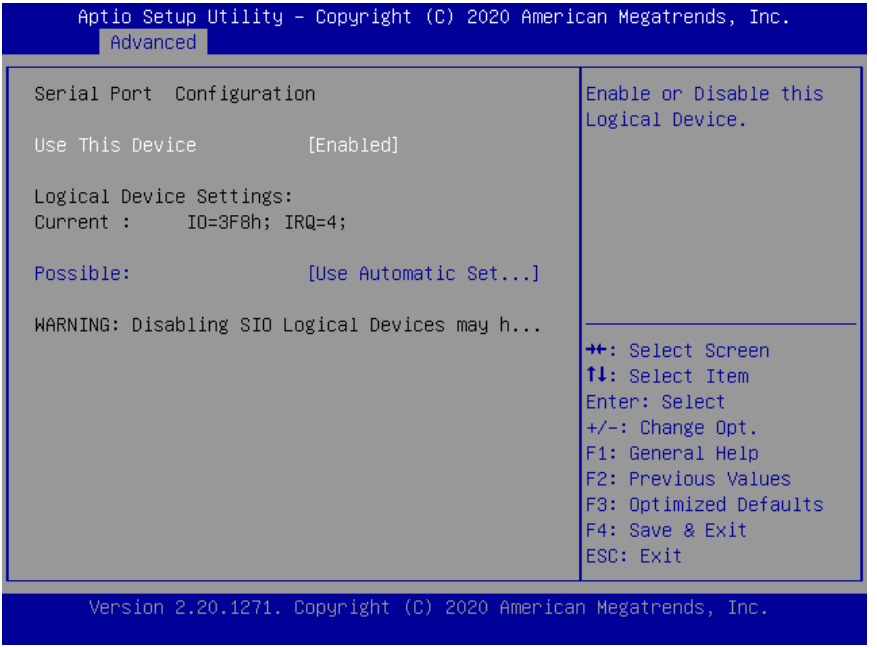


Options Summary		
Legacy USB Support	Disabled	
	Enabled	Optimal Default, Failsafe Default
Enables Legacy USB support. AUTO option disables legacy support if no USB devices are connected. DISABLE option will keep USB devices available only for EFI applications.		

3.4.4 SIO Configuration

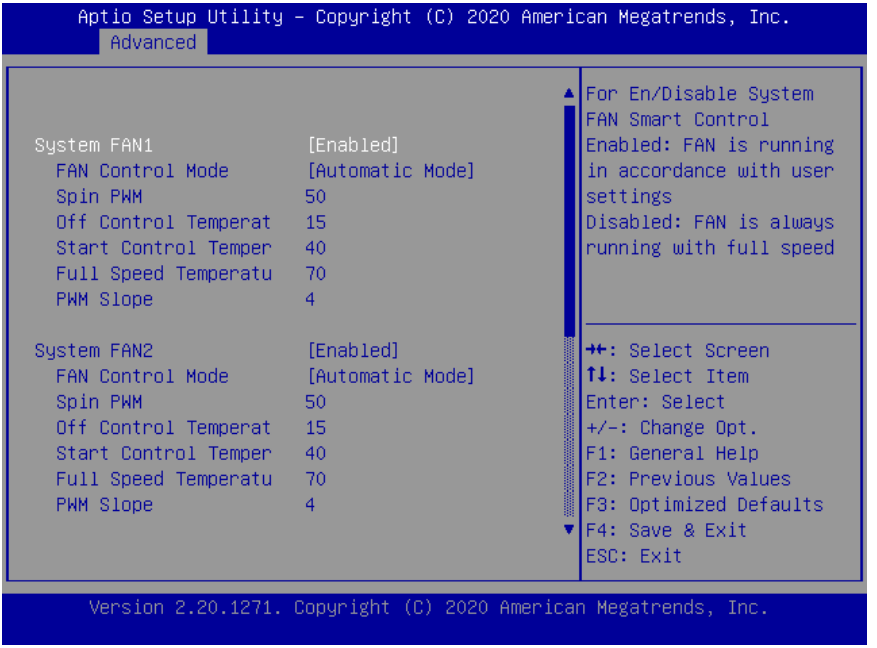


3.4.4.1 Serial Port Configuration



Options Summary		
Use This Device	Disabled	
	Enabled	Optimal Default, Failsafe Default
Enable/Disable this Logical Device		
Possible:	Use Automatic Settings	Optimal Default, Failsafe Default
	IO=3F8; IRQ=4; DMA;	
	IO=2C8; IRQ=11; DMA;	
Allow user to change Device's Resource settings. New settings will be reflected on This Setup Page after System restarts.		

3.4.5 Hardware Monitor

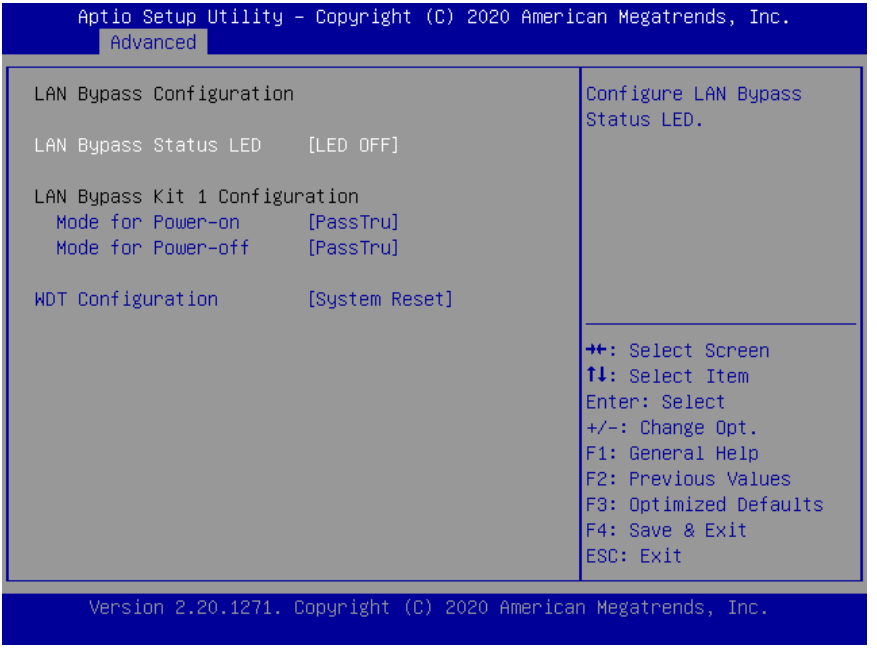


Options Summary		
System Fan	Enabled	Optimal Default, Failsafe Default
	Disabled	
For En/Disable System FAN Smart Control Enabled: FAN is running in accordance with user settings Disabled: FAN is always running with full speed		
FAN Control Mode	Automatic Mode	Optimal Default, Failsafe Default
	Manual Mode	
Manual Mode: Depends on PWM Duty Automatic Mode: FAN Speed depends on CPU Temperature		
Spin PWM	50	Optimal Default, Failsafe Default
The PWM Duty of FAN Spin Range: [0 - 255]		
Off Control Temperature	15	Optimal Default, Failsafe Default
Temperature Limit Value of Fan Off Note: Some fans have the minimum speed even if the PWM value is 0		

Table Continues on Next Page...

Options Summary		
Start Control Temperature	40	Optimal Default, Failsafe Default
Temperature Limit Value of FAN Start Control		
Full Speed Temperature	70	Optimal Default, Failsafe Default
Temperature Limit Value of FAN Full Speed		
PWM Slope	4	Optimal Default, Failsafe Default
Slope PWM value/Degree C for FAN Speed Control Range: [1-15]		

3.4.6 LAN Bypass Configuration

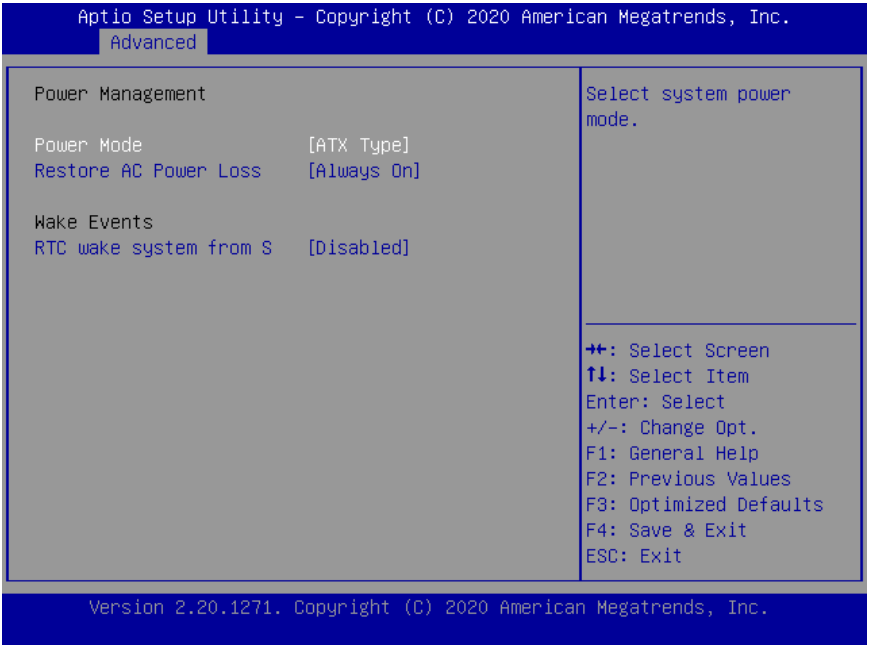


Options Summary		
LAN Bypass Status LED	LED OFF	Optimal Default, Failsafe Default
	RED LED ON	
	RED LED BLINK	
	RED LED FAST BLINK	
	GREEN LED ON	
	GREEN LED BLINK	
	GREEN LED FAST BLINK	
Configure LAN Bypass Status LED.		
Mode for Power-on	ByPass	
	PassTru	Optimal Default, Failsafe Default
Configure LAN kit behavior when system in power-on state. (Bypass/Pass Through)		
Mode for Power-off	ByPass	
	PassTru	Optimal Default, Failsafe Default
Configure LAN kit behavior when system in power-off state. (Bypass/Pass Through)		

Table Continues on Next Page

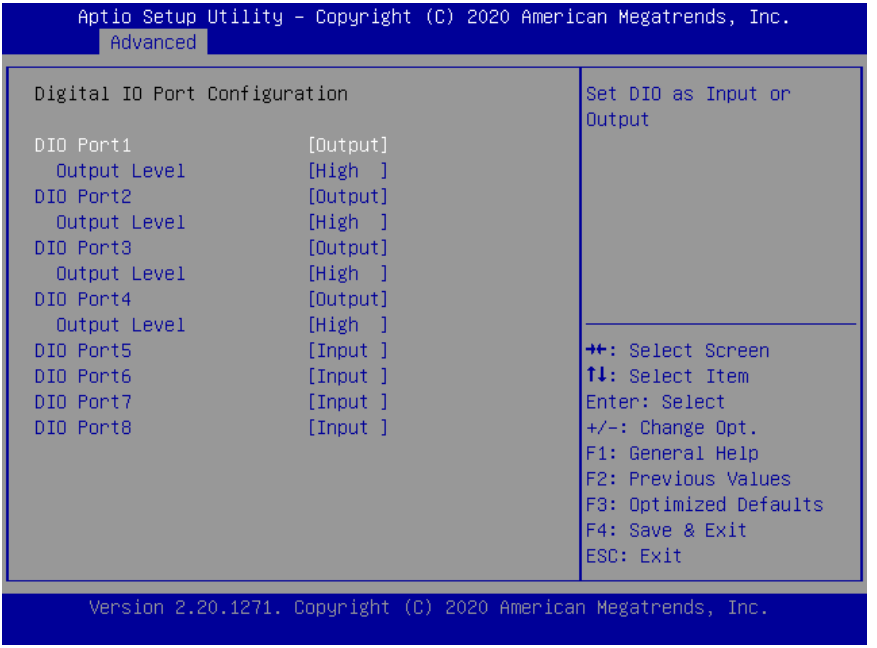
Options Summary		
WDT Configuration	System Reset	Optimal Default, Failsafe Default
	Force ByPass	
Configure WDT behavior, System Rest or Force Bypass		

3.4.7 Power Management



Options Summary		
Power Mode	ATX Type	Optimal Default, Failsafe Default
	AT Type	
Select power supply mode.		
Restore AC Power Loss	Last State	
	Always On	Optimal Default, Failsafe Default
	Always Off	
Select power state when power is re-applied after a power failure.		
RTC wake system from S5	Disabled	Optimal Default, Failsafe Default
	Fixed Time	
	Dynamic Time	
Fixed Time: System will wake on the hr::min::sec Specified Dynamic Time: System will wake on the current time + Increase minutes(s).		

3.4.8 Digital IO Port Configuration



Options Summary		
DIO Port1~4	Output	Optimal Default, Failsafe Default
	Input	
Set DIO as Input or Output		
Output Level	High	Optimal Default, Failsafe Default
	Low	
Set output level when DIO pin is output		
DIO Port5~8	Output	
	Input	Optimal Default, Failsafe Default
Set DIO as Input or Output		

3.5 Setup Submenu: Security

Change User/Administrator Password

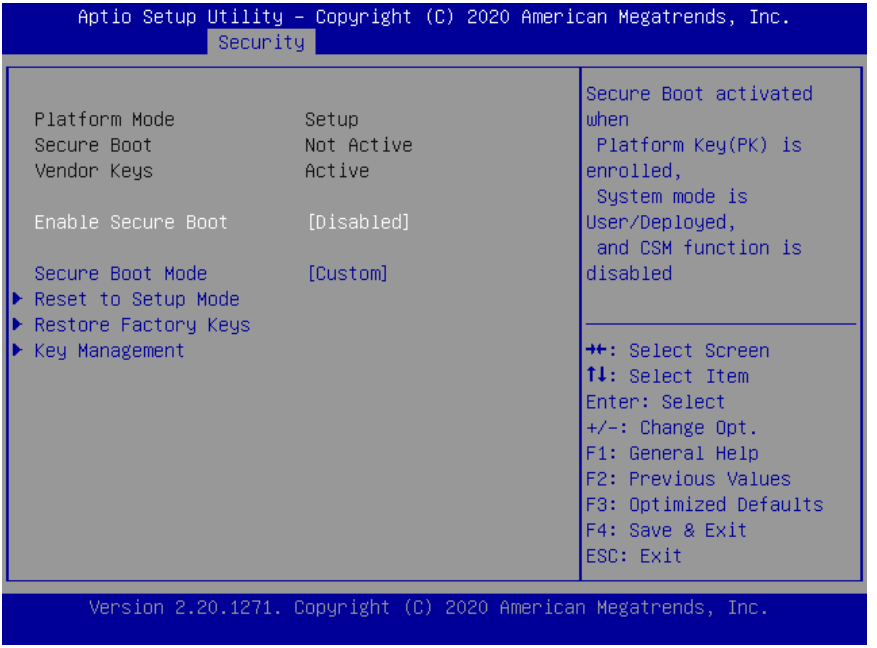
You can set an Administrator Password or User Password. An Administrator Password must be set before you can set a User Password. The password will be required during boot up, or when the user enters the Setup utility. A User Password does not provide access to many of the features in the Setup utility.

Select the password you wish to set, and press Enter. In the dialog box, enter your password (must be between 3 and 20 letters or numbers). Press Enter and retype your password to confirm. Press Enter again to set the password.

Removing the Password

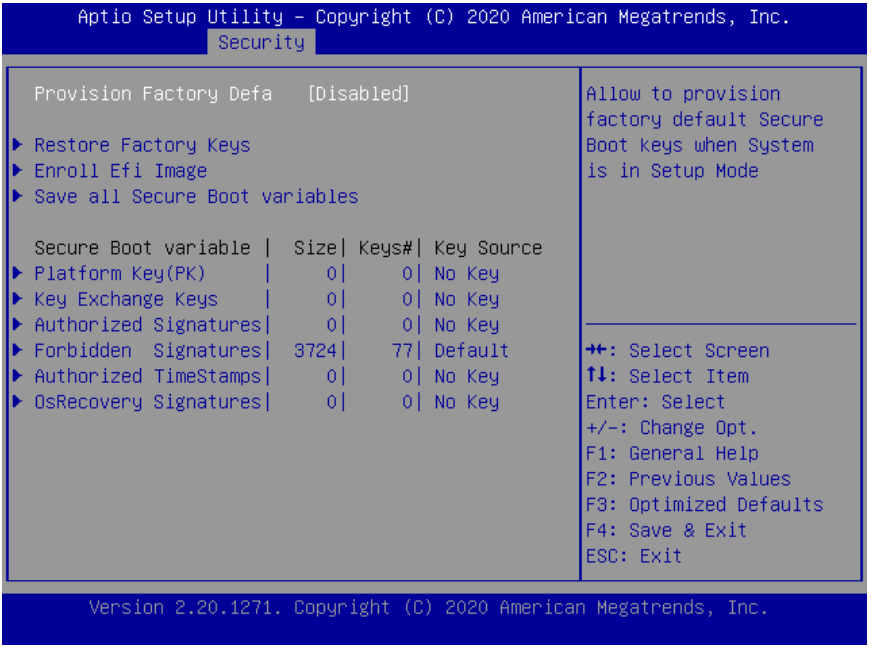
Select the password you want to remove and enter the current password. At the next dialog box press Enter to disable password protection.

3.5.1 Secure Boot



Options Summary		
Enable Secure Boot	Disabled	Optimal Default, Failsafe Default
	Enabled	
Secure Boot activated when Platform Key (PK) is enrolled, System mode is User/Deployed, and CSM function is disabled.		
Secure Boot Mode	Standard	
	Custom	Optimal Default, Failsafe Default
Secure Boot mode selector: Standard/Custom. In Custom mode Secure Boot Variables can be configured without authentication.		
Reset to Setup Mode	Force system to setup mode – delete all Secure Boot key databases.	
Restore Factory Keys	Force system to user mode – restore factory default Secure Boot key databases.	

3.5.1.1 Key Management

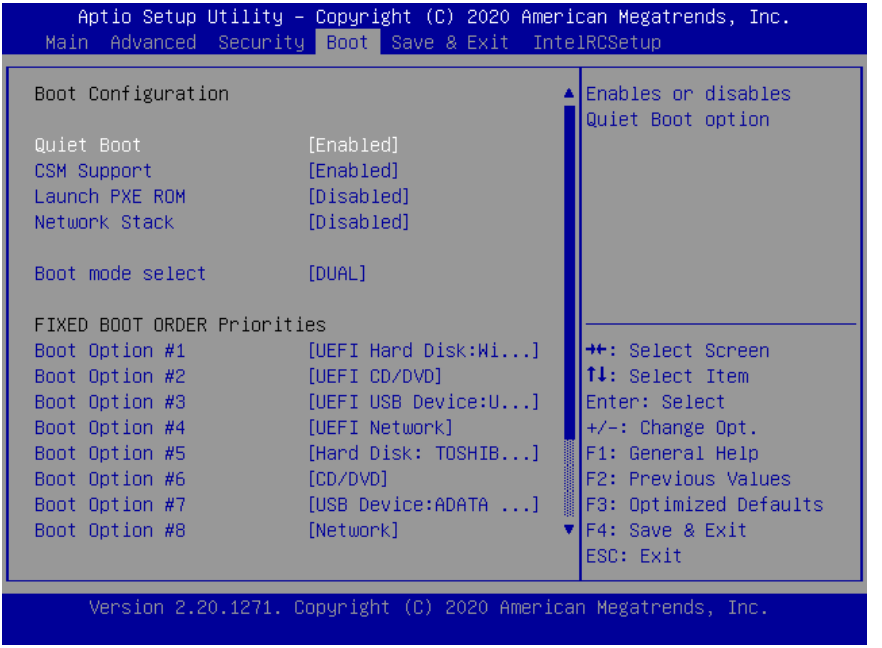


Options Summary		
Provision Factory Defaults	Disabled	Optimal Default, Failsafe Default
	Enabled	
Reset to Setup Mode	Force system to setup mode – delete all Secure Boot key databases.	
Enroll Efi Image	Allow the image to run in Secure Boot mode. Enroll SHA256 hash of the binary into Authorized Signature Database (db).	
Save all Secure Boot Variables.	Save NVRAM content of Secure Boot policy variables to the files (EFI_SIGNATURE_LIST data format) in root folder on a target file system device.	

Secure Boot Variables on Next Page…

Options Summary
Secure Boot Variables Enroll Factory Defaults or load certificates from a file: 1. Public Key Certificate in: a) EFI_SIGNATURE_LIST b) EFI_CERT_X509 (DER encoded) c) EFI_CERT_RSA2048 (bin) d) EFI_CERT_SHA256,384,512 2. Authenticated UEFI Variable 3. EFI PE/COFF Image (SHA256) Key Source: Default, External, Mixed, Test

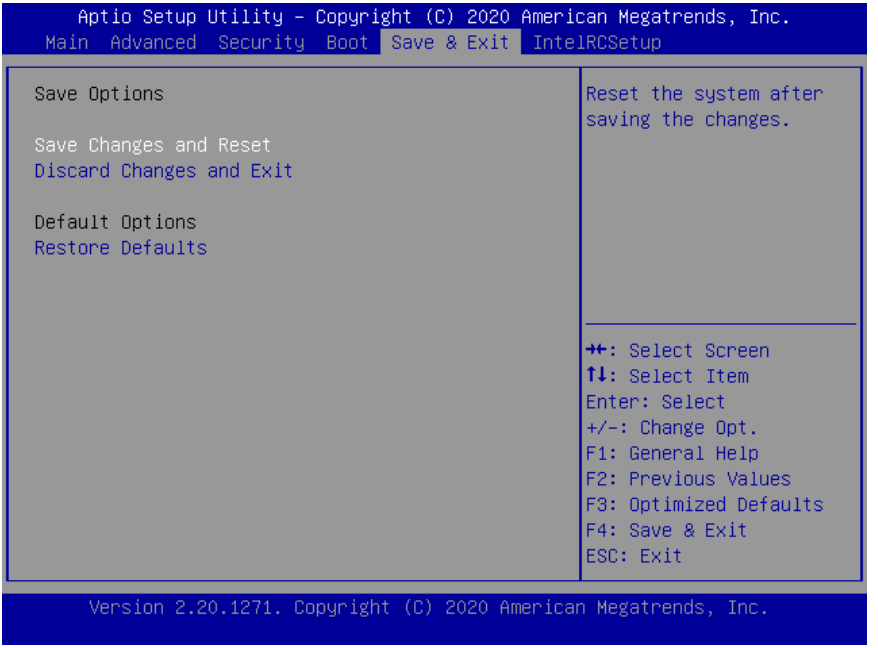
3.6 Setup Submenu: Boot



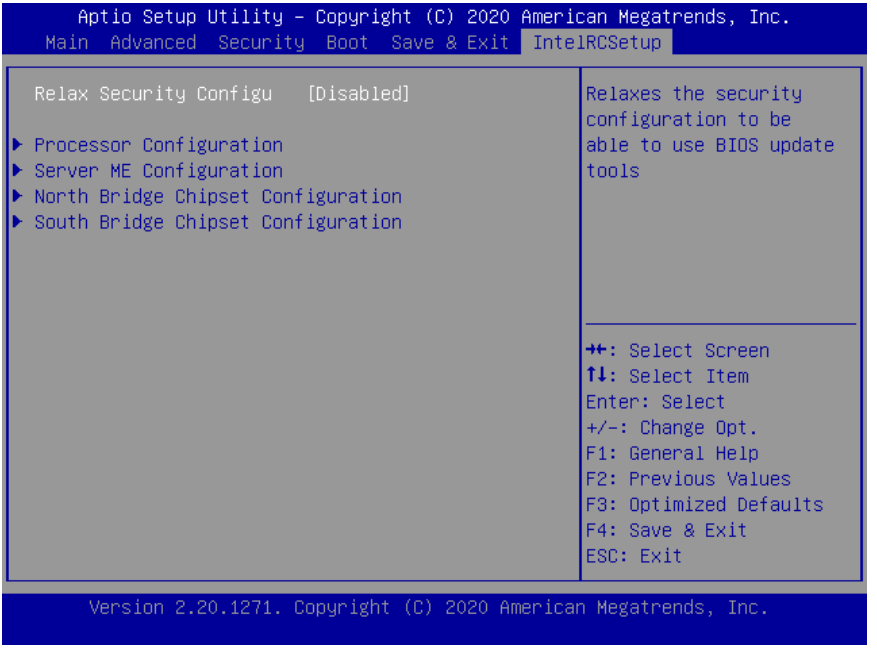
Options Summary		
Quiet Boot	Disabled	
	Enabled	Optimal Default, Failsafe Default
Enable / Disable Quiet Boot option.		
CSM Support	Enabled	Optimal Default, Failsafe Default
	Disabled	
Enable/Disable CSM Support.		
Launch PXE Rom	Disabled	Optimal Default, Failsafe Default
	Enabled	
Controls the execution of UEFI and Legacy PXE OpROM.		
Network Stack	Disabled	Optimal Default, Failsafe Default
	Enabled	
Enable/Disable UEFI Network Stack.		
Boot mode Select	Legacy	
	UEFI	
	Dual	Optimal Default, Failsafe Default
Select boot mode Legacy/UEFI.		

Options Summary	
UEFI Hard Disk Drive BBS Priorities.	Specifies the Boot Device Priority sequence from available UEFI Hard Disk Drives.
UEFI USB Drive BBS Priorities.	Specifies the Boot Device Priority sequence from available UEFI USB Drives.
SD Drive BBS Priorities.	Specifies the Boot Device Priority sequence from available SD Drives.
USB Drive BBS Priorities	Specifies the Boot Device Priority sequence from available USB Drives.

3.7 Setup Submenu: Save & Exit

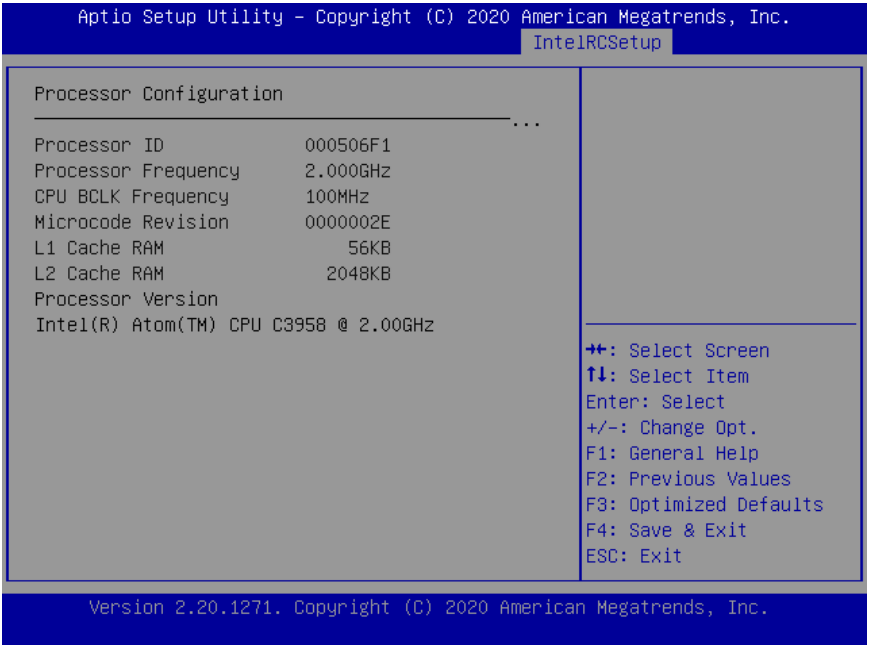


3.8 Setup Submenu: Intel RC Setup

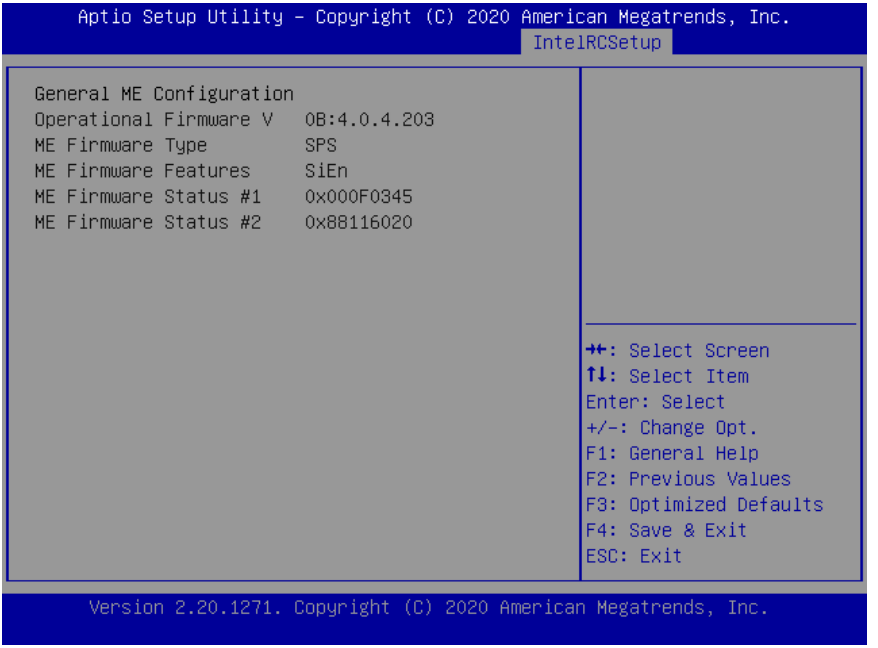


Options Summary		
Relax Security Configuration	Disabled	Optimal Default, Failsafe Default
	Enabled	
Relaxes the security configuration to be able to use BIOS update tools.		

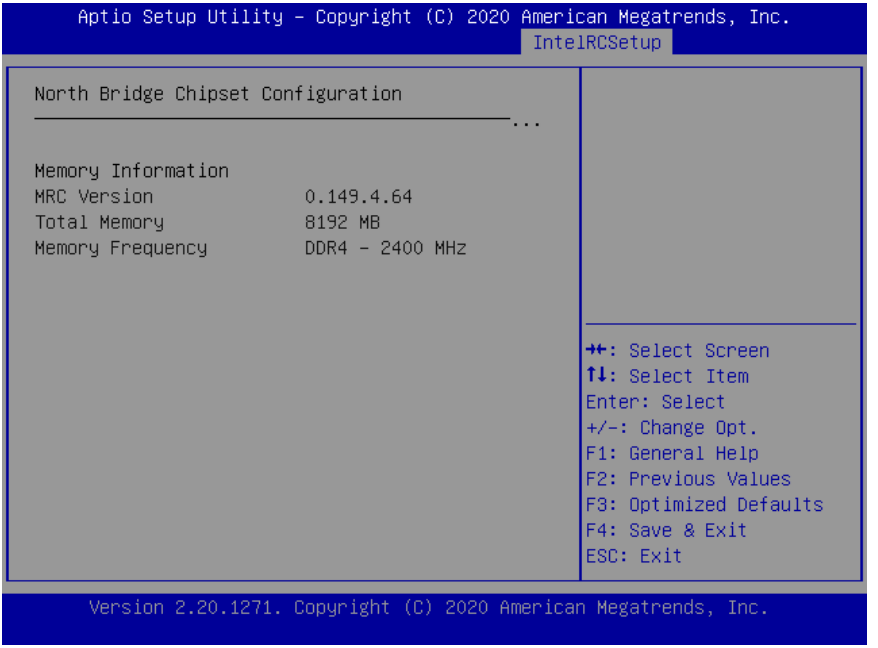
3.8.1 Processor Configuration



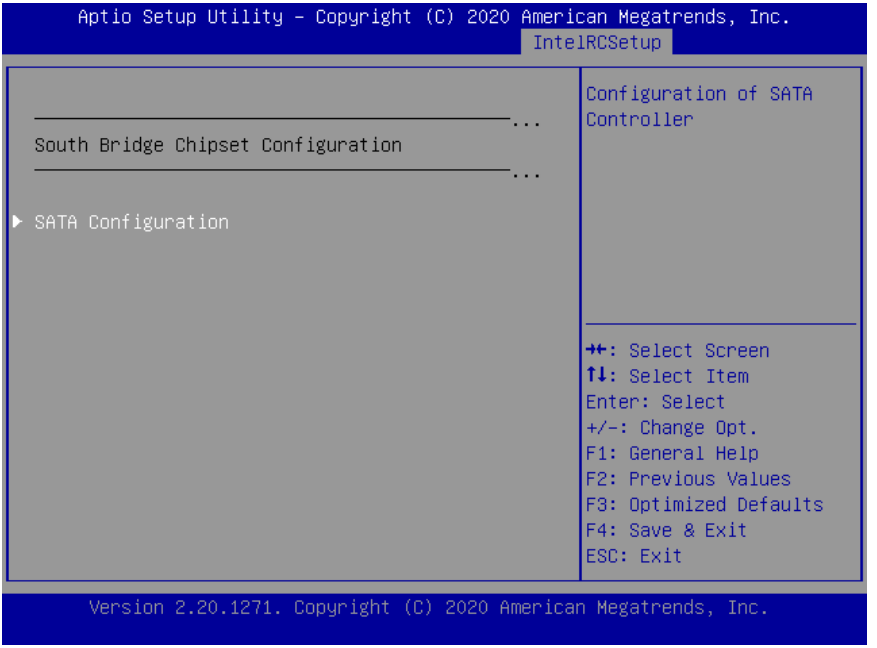
3.8.2 Server ME Configuration



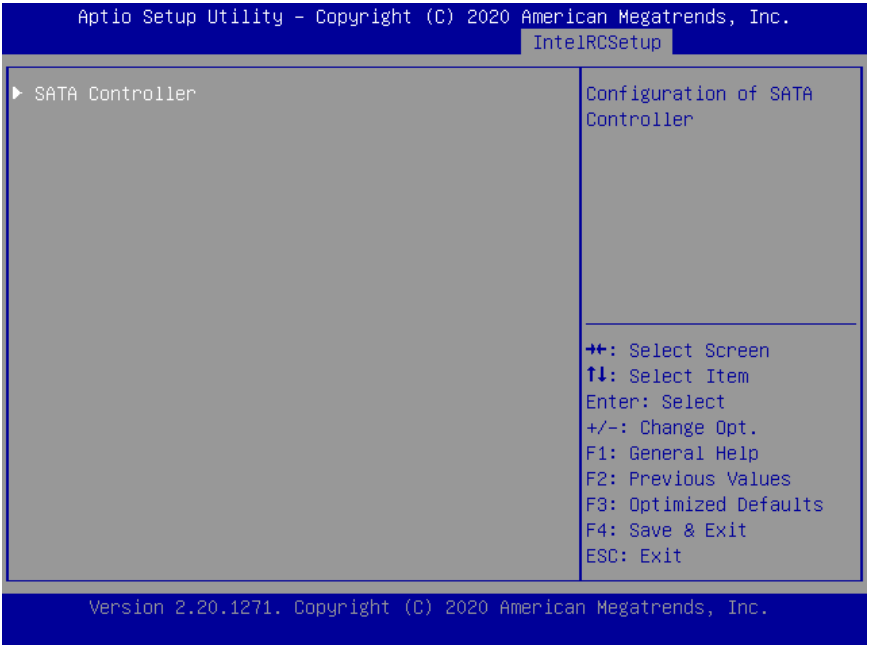
3.8.3 North Bridge Chipset Configuration



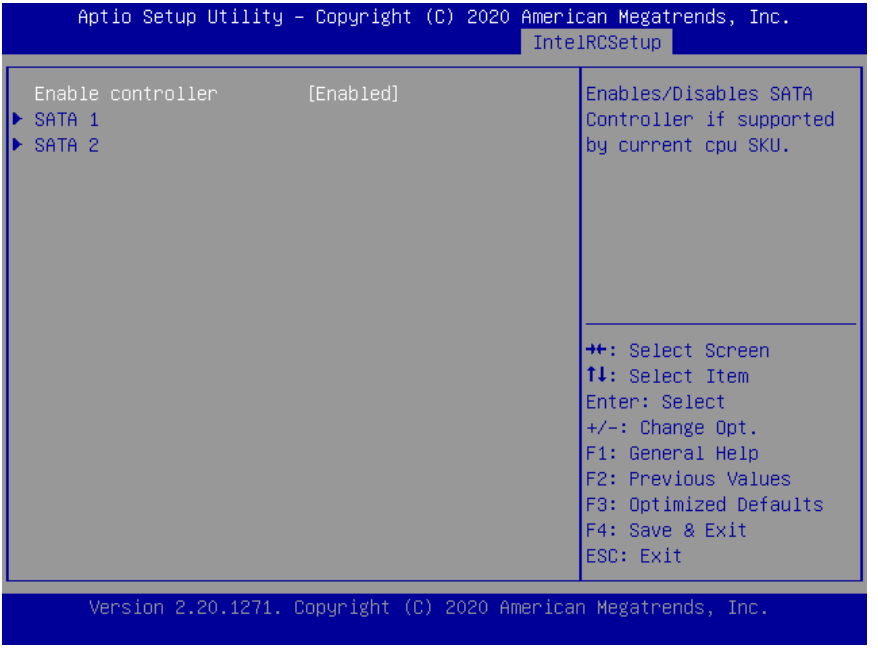
3.8.4 South Bridge Chipset Configuration



3.8.4.1 SATA Configuration

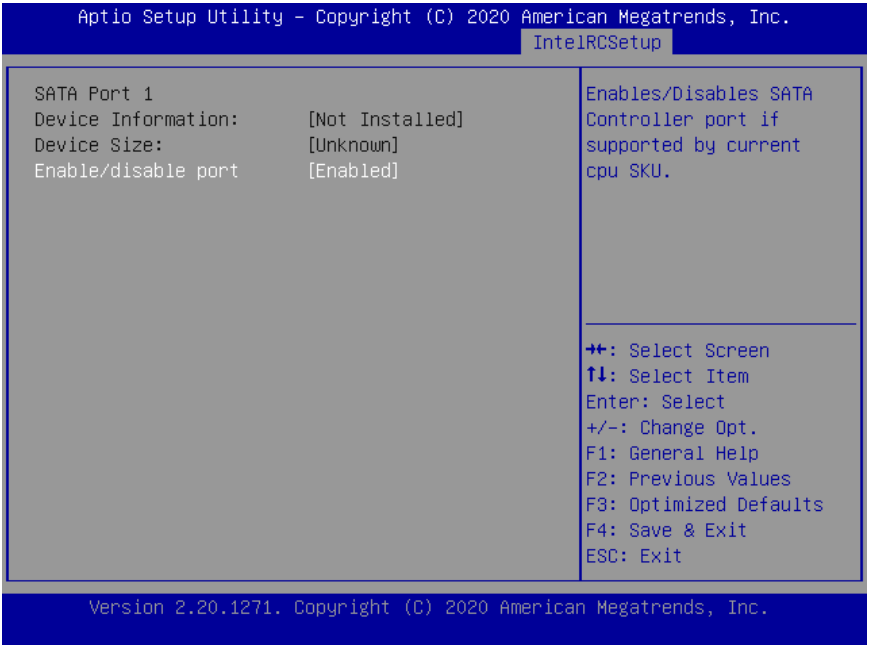


3.8.4.1.1 SATA Controller



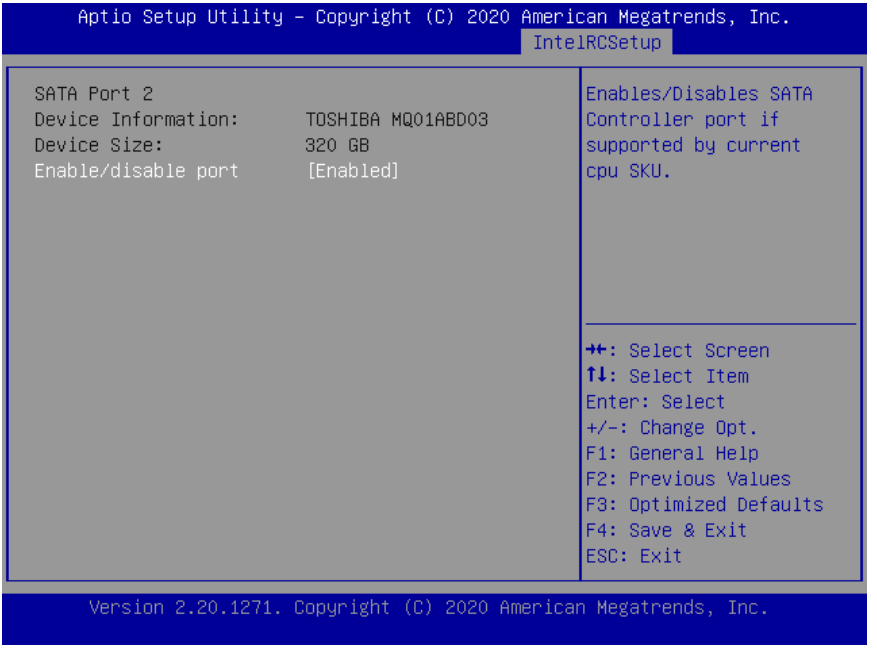
Options Summary		
Enable controller	Disabled	
	Enabled	Optimal Default, Failsafe Default
Enables/Disables SATA Controller if supported by current CPU SKU.		

3.8.4.1.1.1 SATA 1



Options Summary		
Enable controller	Enabled	Optimal Default, Failsafe Default
	Disabled	
Enables/Disables SATA Controller port if supported by current cpu SKU.		

3.8.4.1.1.2 SATA 2



Options Summary		
Enable controller	Enabled	Optimal Default, Failsafe Default
	Disabled	
Enables/Disables SATA Controller port if supported by current cpu SKU.		

Chapter 4

Driver Installation

4.1 Driver Download and Installation

Drivers for the FWS-2365 can be downloaded from the product page on the AAEON website by following this link:

https://www.aaeon.com/en/p/white-box-desktop-network-appliance-fws-2365

Download the driver(s) you need and follow the steps below to install them.

For Linux:

LAN Driver

Appendix A

Watchdog Timer Programming

A.1 Watchdog Timer Initial Program

Table 1 : SuperIO relative register table		
	Default Value	Note
Index	0x2E(Note1)	SIO MB PnP Mode Index Register 0x2E or 0x4E
Data	0x2F(Note2)	SIO MB PnP Mode Data Register 0x2F or 0x4F

Table 2 : Watchdog relative register table					
	LDN	Register	BitNum	Value	Note
Timer Counter	0x07(Note3)	0x73(Note4)		(Note24)	Time of watchdog timer (0~255) This register is byte access
Counting Unit	0x07(Note5)	0x72(Note6)	7(Note7)	1(Note8)	Select time unit. 1: second 0: minute
Watchdog Enable (KRST)	0x07(Note9)	0x72(Note10)	6(Note11)	1(Note12)	0: Disable 1: Enable
Timeout Status	0x07(Note13)	0x71(Note14)	0(Note15)	1	1: Clear timeout status

```
*********************************************************************************
// SuperIO relative definition (Please reference to Table 1)
#define byte   SIOIndex   //This parameter is represented from Note1
#define byte   SIOData   //This parameter is represented from Note2
#define   void   IOWriteByte(byte IOPort, byte Value);
#define   byte   IOReadByte(byte IOPort);
// Watch Dog relative definition (Please reference to Table 2)
#define byte   TimerLDN   //This parameter is represented from Note3
#define byte   TimerReg   //This parameter is represented from Note4
#define byte   TimerVal   // This parameter is represented from Note24
#define byte   UnitLDN   //This parameter is represented from Note5
#define byte   UnitReg   //This parameter is represented from Note6
#define byte   UnitBit   //This parameter is represented from Note7
#define byte   UnitVal   //This parameter is represented from Note8
#define byte   EnableLDN   //This parameter is represented from Note9
#define byte   EnableReg   //This parameter is represented from Note10
#define byte   EnableBit   //This parameter is represented from Note11
#define byte   EnableVal   //This parameter is represented from Note12
#define byte   StatusLDN   // This parameter is represented from Note13
#define byte   StatusReg   // This parameter is represented from Note14
#define byte   StatusBit   // This parameter is represented from Note15
*********************************************************************************
```

```
*********************************************************************************
VOID   Main(){
        // Procedure : AaeonWDTConfig
        // (byte)Timer : Time of WDT timer.(0x00~0xFF)
        // (boolean)Unit : Select time unit(0: second, 1: minute).
        AaeonWDTConfig();

        // Procedure : AaeonWDTEnable
         // This procudure will enable the WDT counting.
        AaeonWDTEnable();
}
*********************************************************************************
```

```
*****************************************************************************
// Procedure : AaeonWDTEnable
VOID    AaeonWDTEnable (){
WDTEnableDisable(EnableLDN, EnableReg, EnableBit, 1);
}

// Procedure : AaeonWDTConfig
VOID    AaeonWDTConfig (){
// Disable WDT counting
WDTEnableDisable(EnableLDN, EnableReg, EnableBit, 0);
// Clear Watchdog Timeout Status
WDTClearTimeoutStatus();
// WDT relative parameter setting
WDTParameterSetting();
}

VOID    WDTEnableDisable(byte LDN, byte Register, byte BitNum, byte Value){
        SIOBitSet(LDN, Register, BitNum, Value);
}

VOID    WDTParameterSetting(){
// Watchdog Timer counter setting
SIOByteSet(TimerLDN, TimerReg, TimerVal);
        // WDT counting unit setting
        SIOBitSet(UnitLDN, UnitReg, UnitBit, UnitVal);
}

VOID    WDTClearTimeoutStatus(){
        SIOBitSet(StatusLDN, StatusReg, StatusBit, 1);
}
*****************************************************************************
```

```
*******************************************************************************
OID   SIOEnterMBPnPMode(){
      Switch(SIOIndex){
            Case 0x2E:
                  IOWriteByte(SIOIndex, 0x87);
                  IOWriteByte(SIOIndex, 0x01);
IOWriteByte(SIOIndex, 0x55);
IOWriteByte(SIOIndex, 0x55);
Break;
            Case 0x4E:
                  IOWriteByte(SIOIndex, 0x87);
                  IOWriteByte(SIOIndex, 0x01);
IOWriteByte(SIOIndex, 0x55);
IOWriteByte(SIOIndex, 0xAA);
                  Break;
      }
}

VOID   SIOExitMBPnPMode(){
      IOWriteByte(SIOIndex, 0x02);
      IOWriteByte(SIOData, 0x02);
}

VOID   SIOSelectLDN(byte LDN){
IOWriteByte(SIOIndex, 0x07); // SIO LDN Register Offset = 0x07
      IOWriteByte(SIOData, LDN);
}
*******************************************************************************
```

```
*****************************************************************************
VOID   SIOBitSet(byte LDN, byte Register, byte BitNum, byte Value){
       Byte TmpValue;

       SIOEnterMBPnPMode();
SIOSelectLDN(byte LDN);
       IOWriteByte(SIOIndex, Register);
       TmpValue = IOReadByte(SIOData);
       TmpValue &= ~(1 << BitNum);
       TmpValue |= (Value << BitNum);
       IOWriteByte(SIOData, TmpValue);
       SIOExitMBPnPMode();
}

VOID   SIOByteSet(byte LDN, byte Register, byte Value){
       SIOEnterMBPnPMode();
SIOSelectLDN(LDN);
       IOWriteByte(SIOIndex, Register);
IOWriteByte(SIOData, Value);
SIOExitMBPnPMode();
}
*****************************************************************************
```

Appendix B

Hardware and LAN Bypass Programming

B.1 Status LED

B.1.1 Introduction

The FWS-2365 features several LED indicators which can be programmed using the AAEON SDK. The user can program the LED indicators to display different status modes.

B.1.2 Status LED Configuration

Table1: LED Status

STA_LED2	STA_LED1	STA_LED0	LED Status
0	0	0	LED Off
0	0	1	Red
0	1	0	Red Blinking (Slowly)
0	1	1	Red Blinking (Quickly)
1	0	0	Reserved
1	0	1	Green Blinking (Slowly)
1	1	0	Green Blinking (Quickly)
1	1	1	Green

Table2: Status LED relative register mapping table

CPLD Slave Address 0x90 (Note1)				
	Attribute	Offset(SMBUS)	BitNum	Value
STA_LED2	R/W	0x00 (Note2)	2	(Table 1)
STA_LED1	R/W	0x00 (Note2)	1	(Table 1)
STA_LED0	R/W	0x00 (Note2)	0	(Table 1)

B.1.3 Sample Code

```
*************************************************************
#define Byte      CPLD_SLAVE_ADDRESS  //This parameter is represented from Note1
#define Byte      OFFSET              //This parameter is represented from Note2
*************************************************************
bData = aaeonSmbusReadByte(CPLD_SLAVE_ADDRESS, OFFSET);

switch( LED_FLAG)
{
case 0:
{
        //LED Off
        //BIT2=0, BIT1=0, BIT0=0
        bData = bData & 0xF8;
        break;
}
case 1:
{
        //Red LED On
        //BIT2=0, BIT1=0, BIT0=1
        bData = (bData & 0xF8) | 0x01;
        break;
}
case 2:
{
        //Red LED Blink
        //BIT2=0, BIT1=1, BIT0=0
        bData = (bData & 0xF8) | 0x02;
        break;
}
case 3:
{
        //Red LED Fast Blink
        //BIT2=0, BIT1=1, BIT0=1
        bData = (bData & 0xF8) | 0x03;
        break;
}
case 4:
```

```
{
        //Green LED On
        //BIT2=1, BIT1=1, BIT0=1
        bData = (bData & 0xF8) | 0x07;
        break;
}
case 5:
{
        //Green LED Blink
        //BIT2=1, BIT1=0, BIT0=1
        bData = (bData & 0xF8) | 0x05;
        break;
}
case 6:
{
        //Green LED Fast Blink
        //BIT2=1, BIT1=1, BIT0=0
        bData = (bData & 0xF8) | 0x06;
        break;
}
default:
        break;
}
SmbusWriteByte(CPLD_SLAVE_ADDRESS, 0x00, bData);
************************************************************
```

B.2 LAN Bypass

B.2.1 Introduction

The FWS-2365 supports LAN Bypass to allow uninterrupted network traffic even if a single in-line appliance is shut down or hangs.

B.2.1 LAN Bypass Configuration

Table1: LAN Kit ID Select

LAN_ID2	LAN_ID1	LAN_ID0	LAN kit selected
0	0	0	LAN Kit 1 Selected
0	0	1	LAN Kit 2 Selected

Table2: LAN Bypass relative register table

Function	Description
LAN_ID3	Used to select which LAN Kit will be configured (see Table 1 of this section). These parameters should be set before ACT_EN
LAN_ID2	
LAN_ID1	
LAN_ID0	
PWR_ON	Use for configuring LAN Bypass function behavior for selected LAN kit, when system power is on. 1: Bypass 0: Pass Through
PWR_OFF	Use for configuring LAN Bypass function behavior for selected LAN kit, when system power is off. 1: Bypass 0: Pass Through
WDT_EN	Use for configuring WDT function behavior for selected LAN kit, when WDT is triggered. 0: Normal WDT reset (Default) 1: Force Bypass
ACT_EN	Use for activating programming of LAN kit. It is edge triggering (falling edge 1 to 0) and should be set to high(1) as its normal state.

Table3: LAN Bypass relative register mapping table

CPLD Slave Address 0x90 (Note1)				
	Attribute	Offset(SMBUS)	BitNum	Value
LAN_ID3	R/W	0x01(Note2)	3	(Table 1)
LAN_ID2	R/W	0x01(Note2)	2	(Table 1)
LAN_ID1	R/W	0x01(Note2)	1	(Table 1)
LAN_ID0	R/W	0x01(Note2)	0	(Table 1)
PWR_ON	R/W	0x01(Note2)	6	(Table 2)
PWR_OFF	R/W	0x01(Note2)	5	(Table 2)
WDT_EN	R/W	0x01(Note2)	4	(Table 2)
ACT_EN	R/W	0x01(Note2)	7	(Table 2)

B.2.3 Sample Code

```
*************************************************************
#define Byte      CPLD_SLAVE_ADDRESS  //This parameter is represented from Note1
#define Byte      OFFSET              //This parameter is represented from Note2
*************************************************************
// Select Lan Pair
BYTE bLanSel = LAN_PAIR;

BYTE bData = SmbusReadByte(CPLD_SLAVE_ADDRESS, OFFSET);
// Set Reg01h bit3
if(bLanSel & 0x08)
        bData = bData | 0x08;
else
        bData = bData & 0xF7;
// Set Reg01h bit2
if(bLanSel & 0x04)
        bData = bData | 0x04;
else
        bData = bData & 0xFB;
// Set Reg01h bit1
if(bLanSel & 0x02)
        bData = bData | 0x02;
else
        bData = bData & 0xFD;
// Set Reg01h bit0
if(bLanSel & 0x01)
        bData = bData | 0x01;
```

```
else
        bData = bData & 0xFE;

// Power On Action (Reg01h bit6)
if(SET_PASS_THROUGH) // Pass Through
        bData = bData & 0xBF;
else                                    // Bypass
        bData = bData | 0x40;

// Power Off Action (Reg01h bit5)
if(SET_PASS_THROUGH) // Pass Through
        bData = bData & 0xDF;
else                                    // Bypass
        bData = bData | 0x20;

// WDT Action (Reg01h bit4)
if(SET_WDT_RESET)       // Reset
        bData = bData & 0xEF;
else                            // Bypass
        bData = bData | 0x10;

SmbusWriteByte(CPLD_SLAVE_ADDRESS, OFFSET, bData);

// Apply Settings (Reg01h bit7)
bData = SmbusReadByte(CPLD_SLAVE_ADDRESS, OFFSET);
SmbusWriteByte(CPLD_SLAVE_ADDRESS, OFFSET, bData & 0x7F);
Sleep(500);
bData = SmbusReadByte(CPLD_SLAVE_ADDRESS, OFFSET);
```

SmbusWriteByte(CPLD_SLAVE_ADDRESS, OFFSET, bData | 0x80);

****

B.3 Software Reset Button (General Propose Input)

B.3.1 Introduction

The FWS-2365 features a general-purpose input button which can be programed with the AAEON SDK.

B.3.2 Soft Reset Button Configuration

Table 2: LAN Bypass relative register table

Function	Description
BTN_STS	Reading this register returns the pin level status which is normal high active low. 0: Pin Level States Low 1: Pin Level States High

Table 1 : Soft Reset Button register mapping table

	Attribute	Register(I/O)	BitNum	Value
BTN_STS	R	0xA05(Note1)	4(Note2)	(Note3)

B.3.3 Sample Code

```
*************************************************************
#define Word      BTN_STS      //This parameter is represented from Note1
#define Byte      BTN_STS_R          //This parameter is represented from Note2
*************************************************************
Byte   GET_Value (Word IoAddr, Byte BitNum,Byte Value){
       BYTE  TmpValue;

       TmpValue = inportb (IoAddr);
return   (TmpValue & (1 << BitNum))
}
*************************************************************
VOID   Main(){
       Byte RstBtn;

       RstBtn = GET_Value (BTN_STS, BTN_STS_R);       // Active Low
}
*************************************************************
```

Appendix C

Digital IO Programming

C.1 Digital I/O Register

Table 1: Digital I/O relative register table				
	Register			
DIO access Base Address	0xA00 (Note3)			
	Register	BitNum	Value	Note
DIO-1 Pin Status	Base Address (Note4)	0 (Note5)	(Note6)	GP11
DIO-2 Pin Status	Base Address (Note7)	1 (Note8)	(Note9)	GP12
DIO-3 Pin Status	Base Address (Note10)	2 (Note11)	(Note12)	GP14
DIO-4 Pin Status	Base Address (Note13)	3 (Note14)	(Note15)	GP15
DIO-5 Pin Status	Base Address+2 (Note16)	4 (Note17)	(Note18)	GP34
DIO-6 Pin Status	Base Address+2 (Note19)	5 (Note20)	(Note21)	GP35
DIO-7 Pin Status	Base Address+5 (Note22)	6 (Note23)	(Note24)	GP63
DIO-8 Pin Status	Base Address+3 (Note25)	7 (Note26)	(Note27)	GP47

C.2 Digital I/O Sample Program

```
*********************************************************************************
#define   void   IOWriteByte(byte IOPort, byte Value);
#define   byte   IOReadByte(byte IOPort);
// Digital Input Status relative definition (Please reference to Table 1)
#define byte   DIOBaseAddress   // This parameter is represented from Note3
#define byte   DIO1Reg   // This parameter is represented from Note4
#define byte   DIO1Bit   // This parameter is represented from Note5
#define byte   DIO1Val   // This parameter is represented from Note6
#define byte   DIO2Reg   // This parameter is represented from Note7
#define byte   DIO2Bit   // This parameter is represented from Note8
#define byte   DIO2Val   // This parameter is represented from Note9
#define byte   DIO3Reg   // This parameter is represented from Note10
#define byte   DIO3Bit   // This parameter is represented from Note11
#define byte   DIO3Val   // This parameter is represented from Note12
#define byte   DIO4Reg   // This parameter is represented from Note13
#define byte   DIO4Bit   // This parameter is represented from Note14
#define byte   DIO4Val   // This parameter is represented from Note15
#define byte   DIO5Reg   // This parameter is represented from Note16
#define byte   DIO5Bit   // This parameter is represented from Note17
#define byte   DIO5Val   // This parameter is represented from Note18
#define byte   DIO6Reg   // This parameter is represented from Note19
#define byte   DIO6Bit   // This parameter is represented from Note20
#define byte   DIO6Val   // This parameter is represented from Note21
#define byte   DIO7Reg   // This parameter is represented from Note22
#define byte   DIO7Bit   // This parameter is represented from Note23
#define byte   DIO7Val   // This parameter is represented from Note24
#define byte   DIO8Reg   // This parameter is represented from Note25
#define byte   DIO8Bit   // This parameter is represented from Note26
#define byte   DIO8Val   // This parameter is represented from Note27
*********************************************************************************
```

```
*********************************************************************************
VOID   Main(){
       Boolean PinStatus ;

       // Procedure : AaeonReadPinStatus
       // Input :
       //       Example, Read Digital I/O Pin 3 status
        // Output :
        //       InputStatus :
        //              0: Digital I/O Pin level is low
        //              1: Digital I/O Pin level is High
       PinStatus = AaeonReadPinStatus(DIO3Reg, DIO3Bit);

       // Procedure : AaeonSetOutputLevel
       // Input :
       //       Example, Set Digital I/O Pin 6 level
       AaeonSetOutputLevel(DIO6Reg, DIO6Bit, DIO6Val);
}
*********************************************************************************
```

```
*******************************************************************************
Boolean   AaeonReadPinStatus(byte Register, byte BitNum){
        Boolean PinStatus ;

        PinStatus = DIOBitRead(Register, BitNum);
        Return PinStatus ;
}
VOID   AaeonSetOutputLevel(byte Register, byte BitNum, byte Value){
        DIOBitSet(Register, BitNum, Value);
}

Boolean   DIOBitRead(byte Register, byte BitNum){
        Byte TmpValue;

        TmpValue = IOReadByte(Register);
        TmpValue &= (1 << BitNum);
        If(TmpValue == 0)
                Return 0;
        Return 1;
}

VOID   DIOBitSet(byte Register, byte BitNum, byte Value){
        Byte TmpValue;

        TmpValue = IOReadByte(Register);
        TmpValue &= ~(1 << BitNum);
        TmpValue |= (Value << BitNum);
        IOWriteByte(Register, TmpValue);
}
*******************************************************************************
```