

# BOXER-6640

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Fanless Embedded Box PC

User's Manual 3<sup>rd</sup> Ed

## Copyright Notice

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## Packing List

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Before setting up your product, please make sure the following items have been shipped:

Item	Quantity
● BOXER-6640	1
● Wallmount bracket	2
● Screw Package	1
● Thermal Pad	1
● 3 Pin DC-In Power Connector	1
● 2 Pin Remote on/off Connector	1
● Product DVD	1

If any of these items are missing or damaged, please contact your distributor or sales representative immediately.

## About this Document

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This User's Manual contains all the essential information, such as detailed descriptions and explanations on the product's hardware and software features (if any), its specifications, dimensions, jumper/connector settings/definitions, and driver installation instructions (if any), to facilitate users in setting up their product.

Users may refer to the [AAEON.com](http://AAEON.com) for the latest version of this document.

## Safety Precautions

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Please read the following safety instructions carefully. It is advised that you keep this manual for future references

1. All cautions and warnings on the device should be noted.
2. Make sure the power source matches the power rating of the device.
3. Position the power cord so that people cannot step on it. Do not place anything over the power cord.
4. Always completely disconnect the power before working on the system's hardware.
5. No connections should be made when the system is powered as a sudden rush of power may damage sensitive electronic components.
6. If the device is not to be used for a long time, disconnect it from the power supply to avoid damage by transient over-voltage.
7. Always disconnect this device from any power supply before cleaning.
8. While cleaning, use a damp cloth instead of liquid or spray detergents.
9. Make sure the device is installed near a power outlet and is easily accessible.
10. Keep this device away from humidity.
11. Place the device on a solid surface during installation to prevent falls.
12. Do not cover the openings on the device to ensure optimal heat dissipation.
13. Watch out for high temperatures when the system is running.
14. Do not touch the heat sink or heat spreader when the system is running
15. Never pour any liquid into the openings. This could cause fire or electric shock.
16. As most electronic components are sensitive to static electrical charge, be sure to ground yourself to prevent static charge when installing the internal components. Use a grounding wrist strap and contain all electronic components in any static-shielded containers.

17. If any of the following situations arises, please contact our service personnel:
  - i. Damaged power cord or plug
  - ii. Liquid intrusion to the device
  - iii. Exposure to moisture
  - iv. Device is not working as expected or in a manner as described in this manual
  - v. The device is dropped or damaged
  - vi. Any obvious signs of damage displayed on the device
18. Do not leave this device in an uncontrolled environment with temperatures beyond the device's permitted storage temperatures (see chapter 1) to prevent damage.
19. Do NOT disassemble the motherboard so as not to damage the system or void your warranty.
20. If the thermal pad had been damaged, please contact AAEON's salesperson to purchase a new one. Do NOT use those of other brands.
21. The Hex Cylinder Coppers on the front panel are not removable.
22. Repeatedly assemble and disassemble the system may cause damages to the exterior paint and surface and screw holes.
23. Use the right size screwdriver.
24. Use the screwdriver correctly to remove screws from the system.

## FCC Statement

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### **Warning!**



This device complies with Part 15 FCC Rules. Operation is subject to the following two conditions: (1) this device may not cause harmful interference, and (2) this device must accept any interference received including interference that may cause undesired operation.

### **Caution:**

*There is a danger of explosion if the battery is incorrectly replaced. Replace only with the same or equivalent type recommended by the manufacturer. Dispose of used batteries according to the manufacturer's instructions and your local government's recycling or disposal directives.*

### **Attention:**

*Il y a un risque d'explosion si la batterie est remplacée de façon incorrecte. Ne la remplacer qu'avec le même modèle ou équivalent recommandé par le constructeur. Recycler les batteries usées en accord avec les instructions du fabricant et les directives gouvernementales de recyclage.*



## China RoHS Requirements (CN)

产品中有毒有害物质或元素名称及含量

AAEON Embedded Box PC/ Industrial System

部件名称	有毒有害物质或元素					
	铅 (Pb)	汞 (Hg)	镉 (Cd)	六价铬 (Cr(VI))	多溴联苯 (PBB)	多溴二苯醚 (PBDE)
印刷电路板 及其电子组件	○	○	○	○	○	○
外部信号 连接器及线材	○	○	○	○	○	○
外壳	○	○	○	○	○	○
中央处理器 与内存	○	○	○	○	○	○
硬盘	○	○	○	○	○	○
电源	○	○	○	○	○	○
<p>○: 表示该有毒有害物质在该部件所有均质材料中的含量均在 SJ/T 11363-2006 标准规定的限量要求以下。</p> <p>X: 表示该有毒有害物质至少在该部件的某一均质材料中的含量超出 SJ/T 11363-2006 标准规定的限量要求。</p> <p>备注: 一、此产品所标示之环保使用期限, 系指在一般正常使用状况下。 二、上述部件物质中央处理器、内存、硬盘、电源为选购品。</p>						

## China RoHS Requirement (EN)

Poisonous or Hazardous Substances or Elements in Products  
 AAEON Embedded Box PC/ Industrial System

Component	Poisonous or Hazardous Substances or Elements					
	Lead (Pb)	Mercury (Hg)	Cadmium (Cd)	Hexavalent Chromium (Cr(VI))	Polybrominated Biphenyls (PBB)	Polybrominated Diphenyl Ethers (PBDE)
PCB & Other Components	○	○	○	○	○	○
Wires & Connectors for External Connections	○	○	○	○	○	○
Chassis	○	○	○	○	○	○
CPU & RAM	○	○	○	○	○	○
Hard Disk	○	○	○	○	○	○
PSU	○	○	○	○	○	○

O: The quantity of poisonous or hazardous substances or elements found in each of the component's parts is below the SJ/T 11363-2006-stipulated requirement.

X: The quantity of poisonous or hazardous substances or elements found in at least one of the component's parts is beyond the SJ/T 11363-2006-stipulated requirement.

**Note: The Environment Friendly Use Period as labeled on this product is applicable under normal usage only**

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# Chapter 1

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Product Specifications

## 1.1 Specifications

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### System

<b>CPU</b>	Intel® Core™ i7-7700T, Quad Core, 2.9 GHz Intel® Core™ i5-7600T, Quad Core, 2.8 GHz Intel® Core™ i3-7300T, Dual Core, 3.5 GHz Intel® Core™ i7-6700TE, Quad Core, 2.4 GHz Intel® Core™ i5-6500TE, Quad Core, 2.3 GHz Intel® Core™ i3-6100TE, Dual Core, 2.7 GHz
<b>Chipset</b>	Intel® H110
<b>System Memory</b>	DDR4 SODIMM socket (double deck) x 2 Supports 1866/2133MHz DDR4 and up to 32GB  Supports un-buffered and ECC / non-ECC type SODIMM
<b>Display Interface</b>	VGA x 1, HDMI x 2 (Combo DP x 2) – A1 SKU VGA x 1 – A2 SKU
<b>Storage Device</b>	mSATA, SATA HDD/SSD
<b>Ethernet</b>	Intel® I211AT x 1, I219LM x 1
<b>I/O</b>	2 pin Remote power on/off connector Audio x1 (MIC-in, Line-out) USB 2.0 x 3 DB-9 x 3 for RS-232 8-bit DIO DB-9 x 1 for RS-232/422/485 with auto flow control Power ON/OFF switch x 1 3 pin 9~36V DC Power input x 1 (+, -, GND) VGA x 1 HDMI x 2 (Combo DP x 2) USB 3.0 x 4 RJ-45 x 2 for GbE (i211AT x 1, i219LM x 1)

## System

Expansion	Full-size Mini-Card x 1 (PCI-E + USB, w/ SIM slot) Full-size Mini-Card x 1 (mSATA + USB) LPC x 1
Indicator	Power LED HDD active LED
OS Support	Windows® 10 64 bit (Kabylake, Skylake CPU) Windows® 8.1 64 bit (Skylake CPU only) Windows® embedded 8 standard 64 bit (Skylake CPU only)

## Mechanical

Mounting	Wallmount
Dimensions (W x H x D)	10.39" x 3.8" x 7.33" (264mm x 96.4mm x 186.2mm)
Gross Weight	12.76 lb (5.8 kg)
Net Weight	9.9 lb (4.5 kg)

## Environmental

Operating Temperature	-4°F ~ 131°F (-20°C ~ 55°C) (according to IEC68-2-14 with 0.5 m/s AirFlow; with industrial devices)
Storage Temperature	-49 °F ~ 176°F (-45°C ~ 80°C)
Storage Humidity	5 ~ 95% @ 40°C, non-condensing
Anti-Vibration	2 Grms/ 5 ~ 500Hz/ operation – SSD 1 Grms/ 5 ~ 500Hz/ operation – HDD
Certification	CE/FCC class A



## Power Supply

Power Requirement

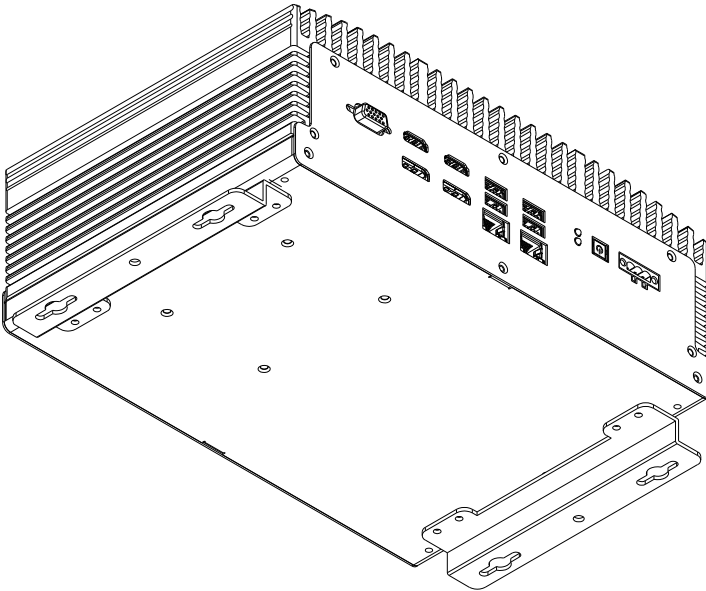
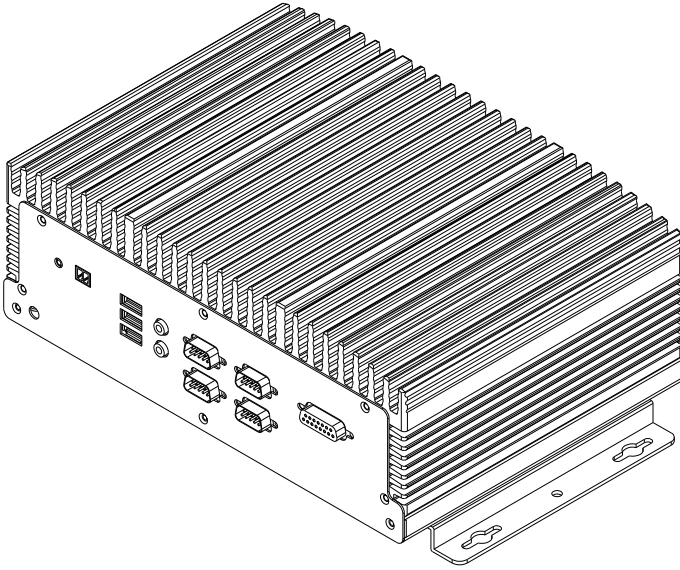
3-pin Phoenix DC Input 9~36V

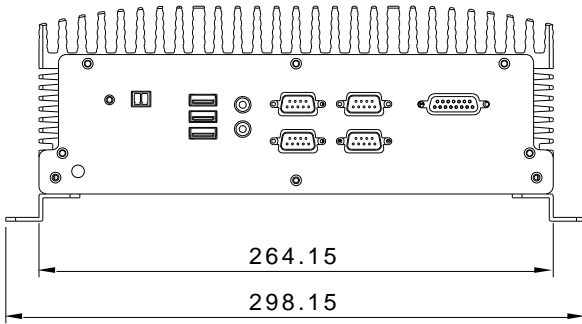
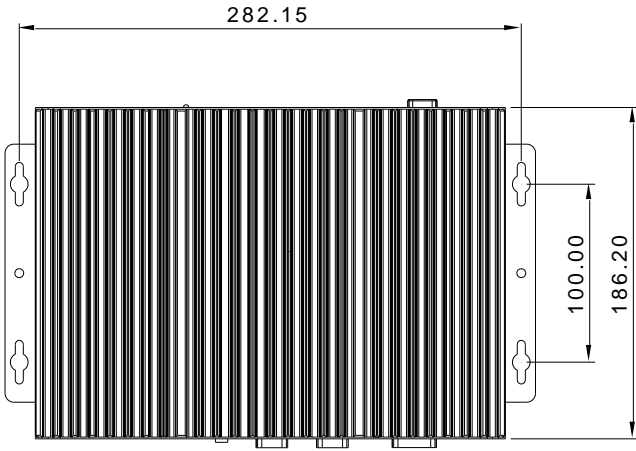
# Chapter 2

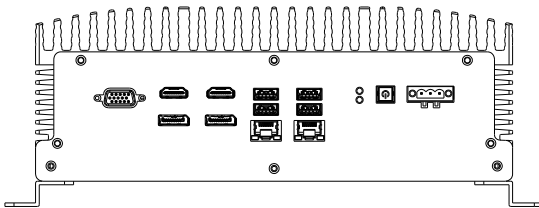
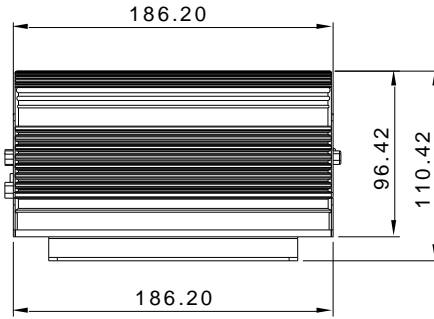
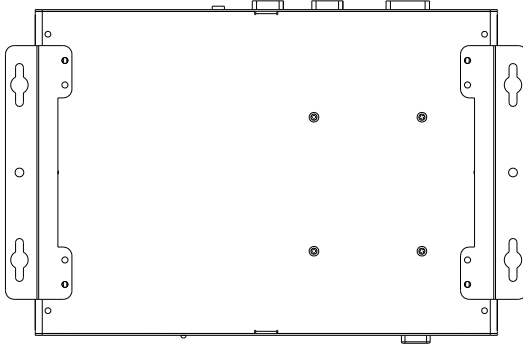
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Hardware Information

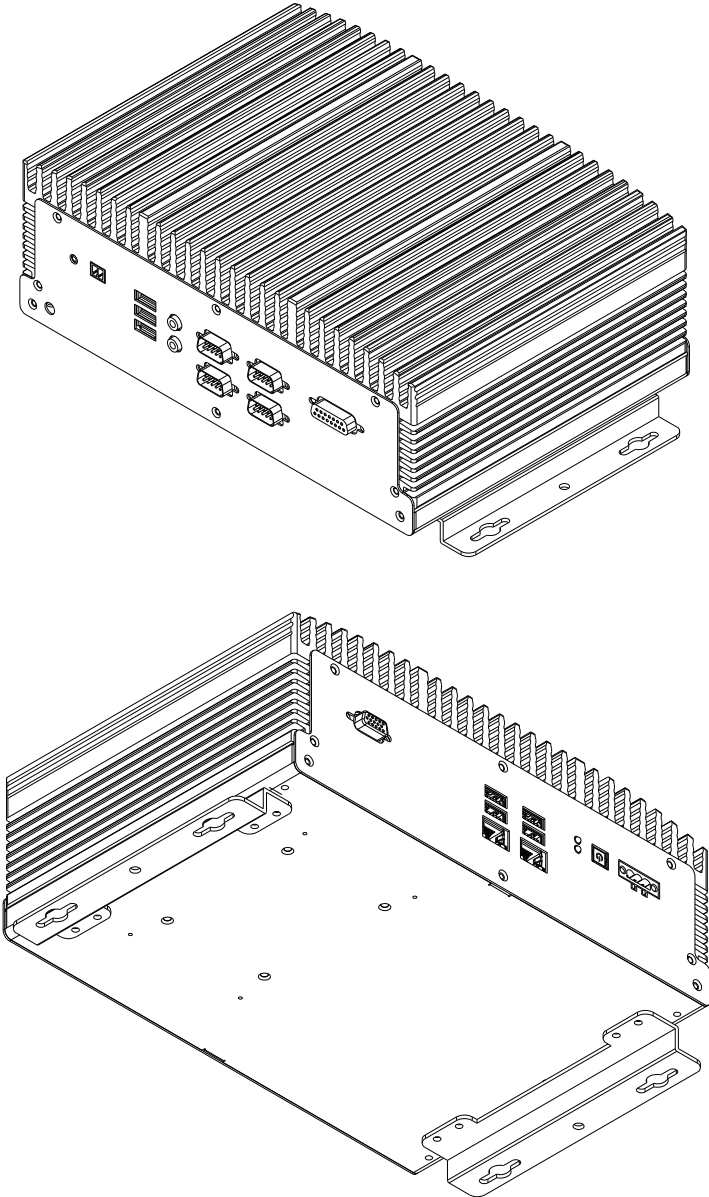
## 2.1 BOXER-6640-A1 Dimensions

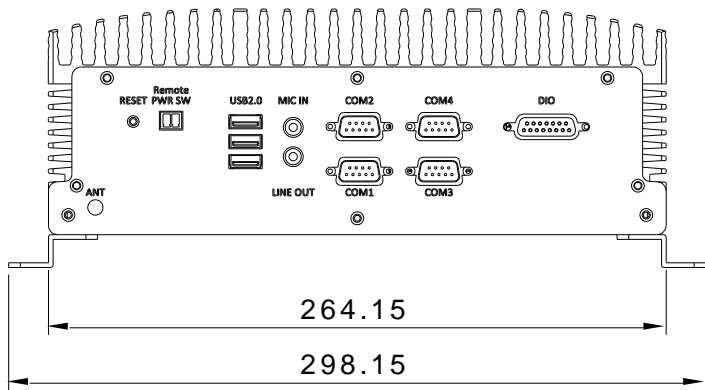
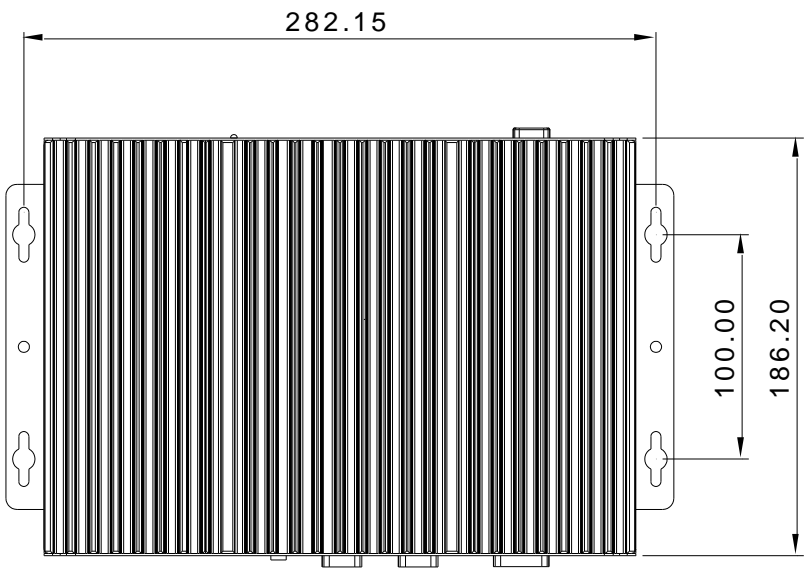


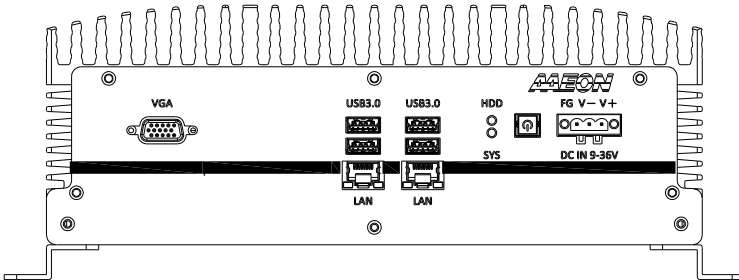
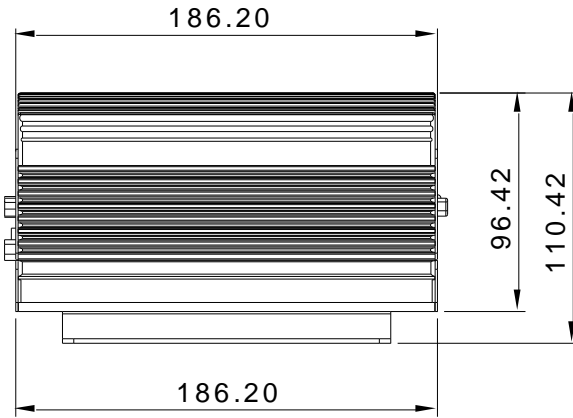
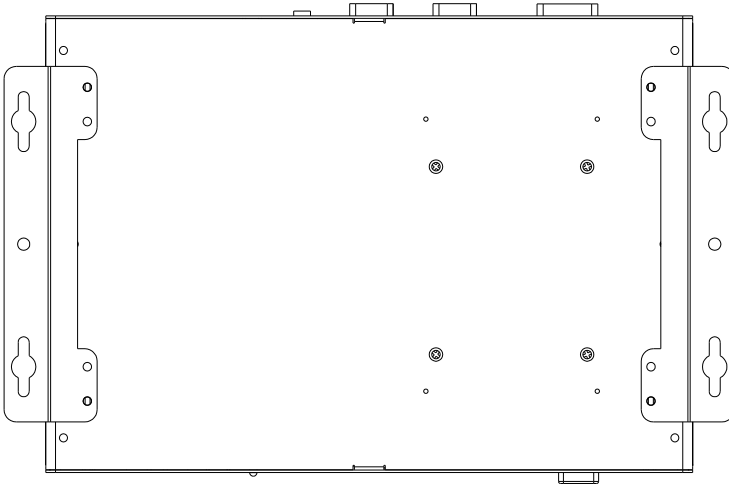




## 2.2 BOXER-6640-A2 Dimensions



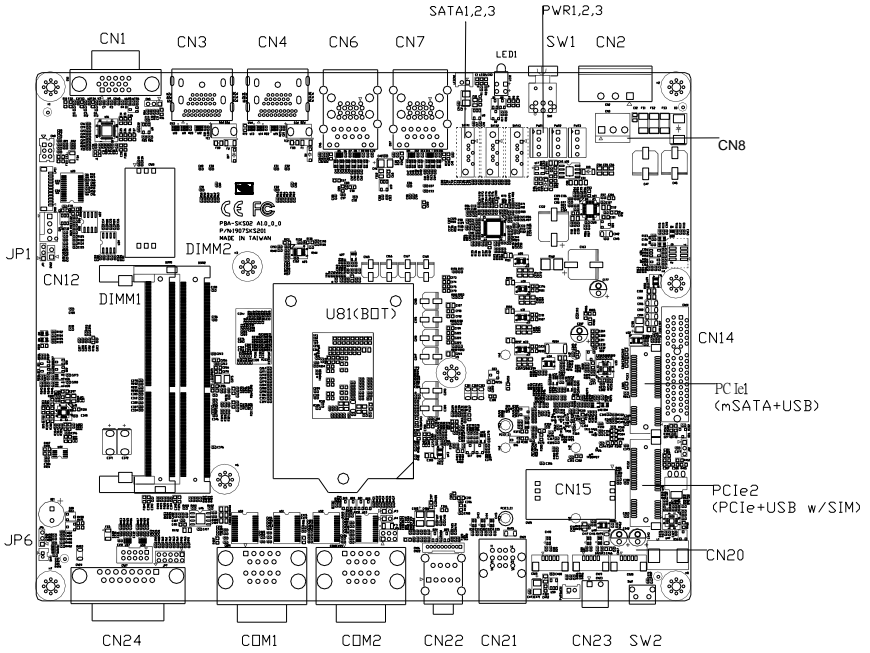




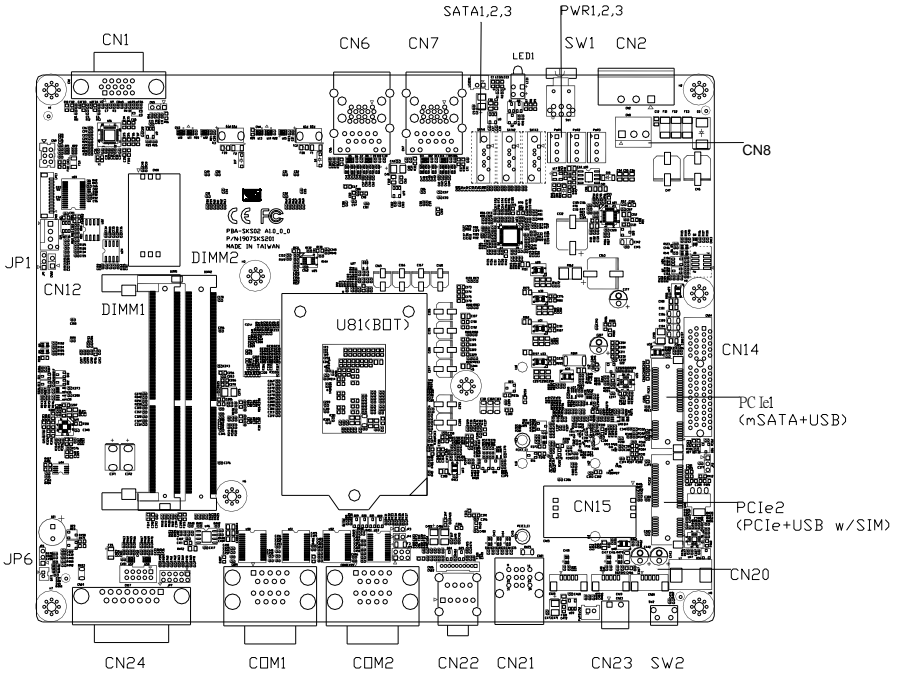


## 2.3 Jumpers and Connectors

### BOXER-6640-A1 (board with HDMI)



BOXER-6640-A2 (board without HDMI)



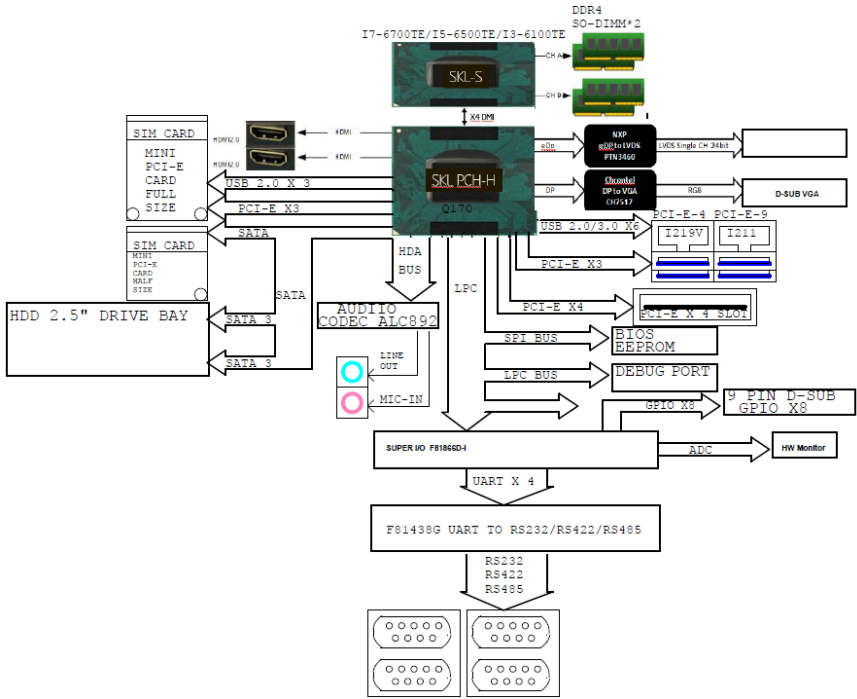
## 2.4 List of Jumpers

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Please refer to the table below for all of the system's jumpers that you can configure for your application.

Label	Function
JP1	AT/ATX mode select
JP6	Clear CMOS

## 2.5 Block Diagram



## 2.6 List of Connectors

Please refer to the table below for all of the system's connectors that you can configure for your application

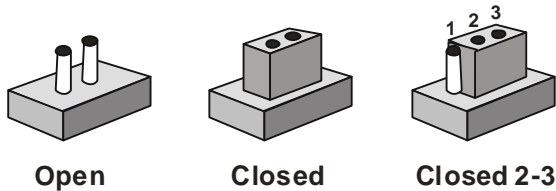
Label	Function
CN1	CRT port
CN2/CN8	DC-IN
CN3	HDMI2/DP2 connector
CN4	HDMI1/DP2 connector
CN13	SPI ROM connector
CN24	DIO connector
CN6	Dual stack USB (3.0) + LAN
CN7	Dual stack USB (3.0) + LAN
CN22	Audio Jack
CN23	Remote button cable connector
CN20	USB 2.0 Connector (BOX connector for backup)
SW1	Power switch
SW2	H/W Reset switch
PWRWCN1	Power switch (BOX connector for backup)
PWR1	SATA PWR connector
PWR2	SATA PWR connector
PWR3	SATA PWR connector
SATA1	SATA connector
SATA2	SATA connector
SATA3	SATA connector
BAT1	RTC battery connector
LPC1	Debug port connector
COM1	Dual COM port (COM1/ COM2)

COM2	Dual COM port (COM3/ COM4)
PCIE1	Minicard connector(SATA Only)
PCIE2	Minicard connector
CN15	SIM card connector

## 2.6.1 Setting Jumpers

You configure your card to match the needs of your application by setting jumpers. A jumper is the simplest kind of electric switch. It consists of two metal pins and a small metal clip (often protected by a plastic cover) that slides over the pins to connect them. To “close” a jumper you connect the pins with the clip.

To “open” a jumper you remove the clip. Sometimes a jumper will have three pins, labeled 1, 2 and 3. In this case you would connect either pins 1 and 2 or 2 and 3.

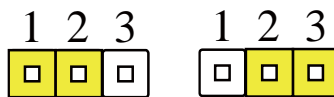


A pair of needle-nose pliers may be helpful when working with jumpers.

If you have any doubts about the best hardware configuration for your application, contact your local distributor or sales representative before you make any change.

Generally, you simply need a standard cable to make most connections.

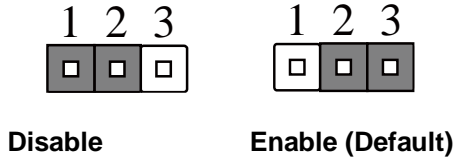
## 2.6.2 Clear CMOS (JP6)



**Normal (Default)**      **Clear CMOS**

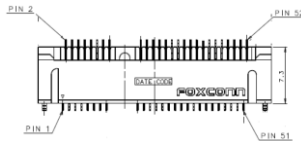
JP1	Function
1-2	Normal (Default)
2-3	Clear CMOS

### 2.6.3 Auto Power Button (JP1)



JP1	Function
1-2	Normal (Default)
2-3	Clear CMOS

### 2.6.4 Mini Card Connector With on board SIM

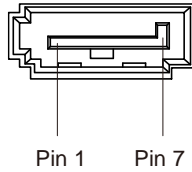


Pin	Signal	Pin	Signal
1	PCIE_WAKE#	2	+V3.3A
3	NC	4	GND
5	NC	6	+1.5V
7	PCIE_CLK_REQ#	8	UIM_PWR
9	GND	10	UIM_DATA
11	PCIE_REF_CLK-	12	UIM_CLK
13	PCIE_REF_CLK+	14	UIM_RST
15	GND	16	UIM_VPP



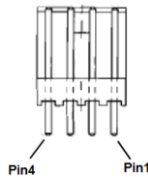
17	NC	18	GND
19	NC	20	W_DISABLE#
21	GND	22	PCIE_RST#
23	PCIE_RX-	24	+V3.3A
25	PCIE_RX+	26	GND
27	GND	28	+1.5V
29	GND	30	SMB_CLK
31	PCIE_TX-	32	SMB_DATA
33	PCIE_TX+	34	GND
35	GND	36	USB_D-
37	GND	38	USB_D+
39	+V3.3A	40	GND
41	+V3.3A	42	NC
43	GND	44	NC
45	NC	46	NC
47	NC	48	+1.5V
49	NC	50	GND
51	NC	52	+V3.3A

## 2.6.5 (SATA1/ SATA2/ SATA3) SATA Port



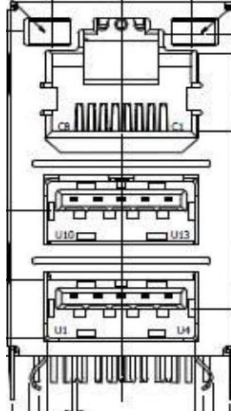
Pin	Pin Name	Signal Type	Signal level
1	GND	GND	
2	SATA_TX+	DIFF	
3	SATA_TX-	DIFF	
4	GND	GND	
5	SATA_RX-	DIFF	
6	SATA_RX+	DIFF	
7	GND	GND	

## 2.6.6 (PWR1/ PWR2/ PWR3) SATA PWR Port



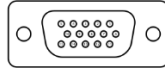
Pin	Pin Name	Level
1	+12V	12V
2	GND	GND
3	GND	GND
4	+5V	5V

## 2.6.7 LAN + USB 3.0



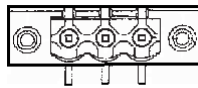
Pin	Signal	Pin	Signal
C1	MDI0+	U2	MDI0-
C3	MDI1+	U4	MDI2+
C5	MDI2-	U6	MDI1-
C7	MDI3+	U8	MDI3-
U1	VBUS_1	U10	VBUS_2
U2	(A)D-	U11	(B)D-
U3	(A)D+	U12	(B)D+
U4	GND	U13	GND
U5	(A)SSRX-	U14	(B)SSRX-
U6	(A)SSRX+	U15	(B)SSRX+
U7	GND	U16	GND
U8	(A)SSTX-	U17	(B)SSTX-
U9	(A)SSTX+	U18	(B)SSTX+

## 2.6.8 VGA port



Pin	Signal	Pin	Signal
1	Red	2	Green
3	Blue	4	NC
5	GND	6	GND
7	GND	8	GND
9	VGA_VCC	10	GND
11	NC	12	DDC_DATA
13	VGA_HSYNC	14	VGA_VSYNC
15	DDC_CLK		

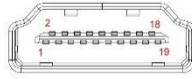
## 2.6.9 DC-IN



PIN1 PIN2 PIN3

Pin	Signal	Pin	Signal
1	PWR_IN	2	GND
3	NC		

## 2.6.10 HDMI port



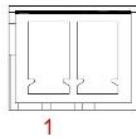
Pin	Signal	Pin	Signal
1	HDMI_DATA2_P	2	GND
3	HDMI_DATA2_N	4	HDMI_DATA1_P
5	GND	6	HDMI_DATA1_N
7	HDMI_DATA0_P	8	GND
9	HDMI_DATA0_N	10	HDMI_CLK_P
11	GND	12	HDMI_CLK_N
13	NC	14	NC
15	HDMI_SCL	16	HDMI_SDA
17	GND	18	HDMI_PWR
19	HDMI_HDP		
1	HDMI_DATA2_P	2	GND
3	HDMI_DATA2_N	4	HDMI_DATA1_P
5	GND	6	HDMI_DATA1_N
7	HDMI_DATA0_P	8	GND
9	HDMI_DATA0_N	10	HDMI_CLK_P
11	GND	12	HDMI_CLK_N
13	NC	14	NC
15	HDMI_SCL	16	HDMI_SDA
17	GND	18	HDMI_PWR
19	HDMI_HDP		

## 2.6.11 DIO port



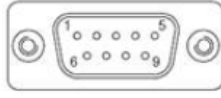
Pin	Signal	Pin	Signal
1	DIO0	2	DIO1
3	DIO2	4	DIO3
5	DIO4	6	DIO5
7	DIO6	8	DIO7
9	GND	10	GND
11	GND	12	GND
13	GND	14	GND
15	+5V		

## 2.6.12 Remote switch connector



Pin	Signal	Pin	Signal
1	PANSWH#	2	GND

## 2.6.13 COM Port



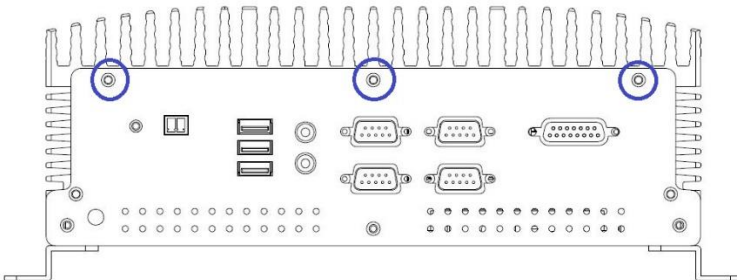
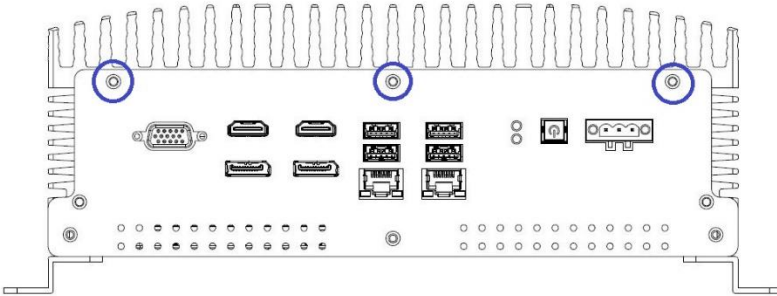
Pin	RS-232	RS422	RS-485
1	DCD	TX-	DATA-
2	RXD	TX+	DATA+
3	TXD	RX+	NC
4	DTR	RX-	NC
5	GND	NC	NC
6	DSR	NC	NC
7	RTS	NC	NC
8	CTS	NC	NC
9	RI	NC	NC

## 2.7 CPU Installation

- Turn off the system, unplug the power cord and make sure the system is off.
- Have Intel KabyLake or Intel SkyLake-S FCLGA1151 Processor (Max. TDP 35W) ready.

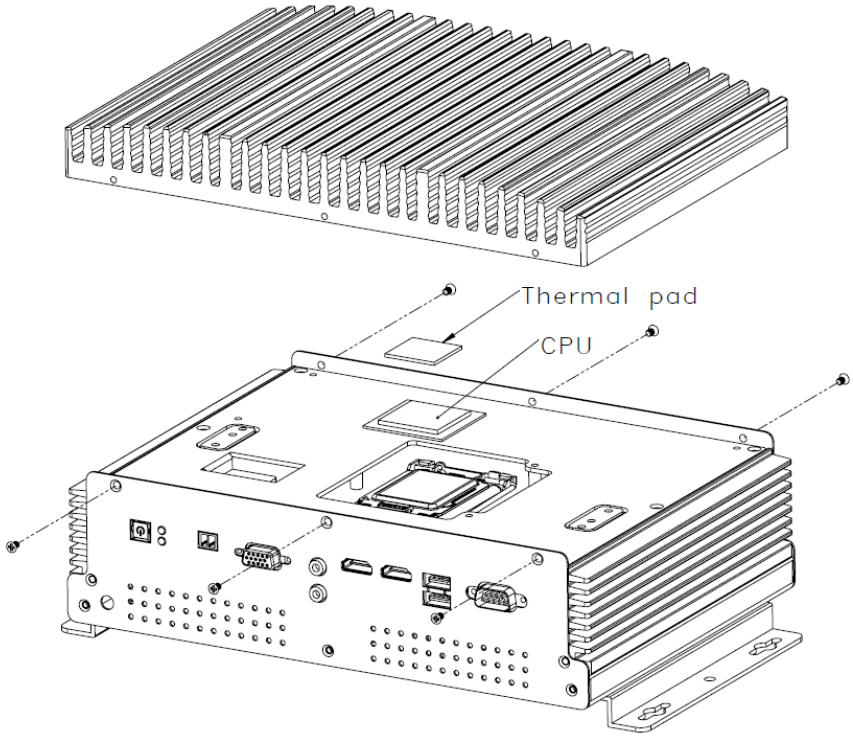


Step 1: Remove the screws as instructed below and remove the heatsink.

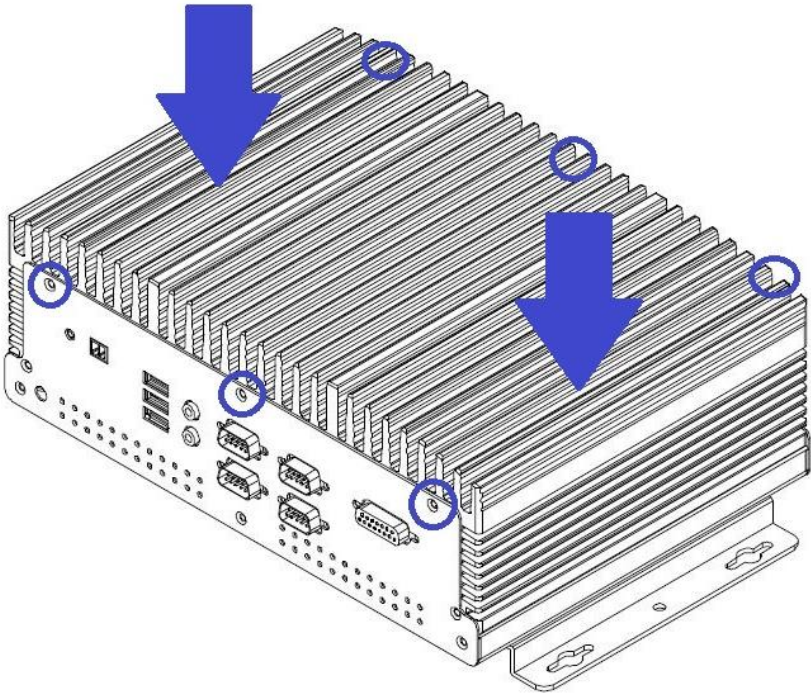




Step 2: Install the CPU into the socket and place the thermal pad onto it.

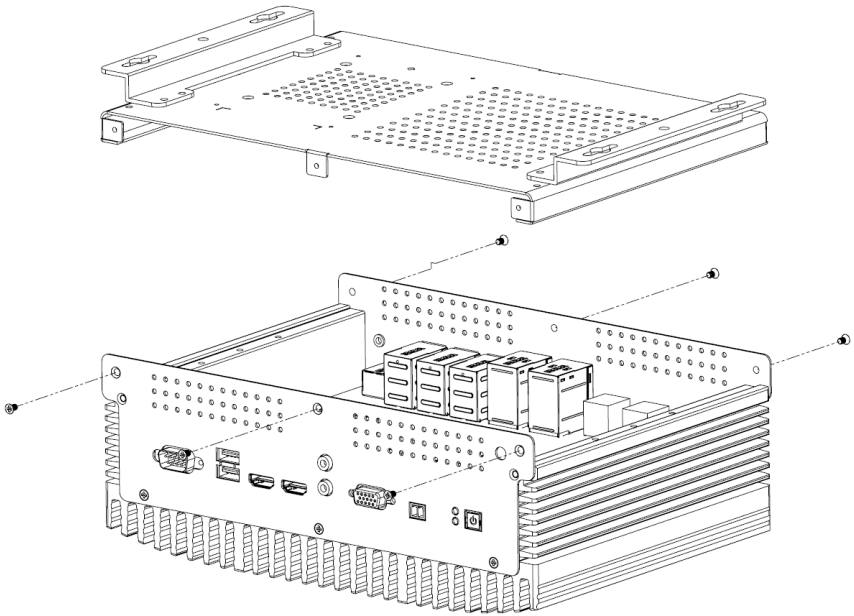


Step 3: Place the heatsink back on and fasten the screws as instructed below.

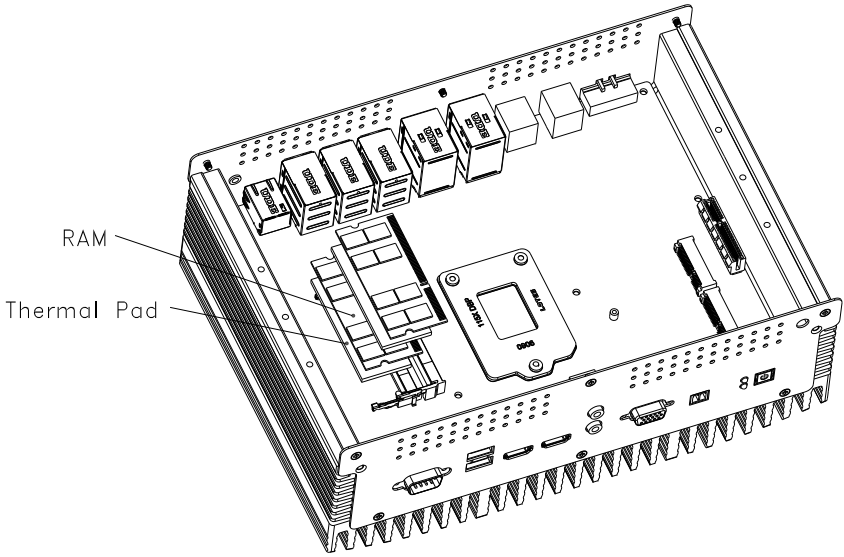


## 2.8 DDR4 Memory Module Installation

Step 1. Turn off the system, unplug the power cord to make sure the system is power off.



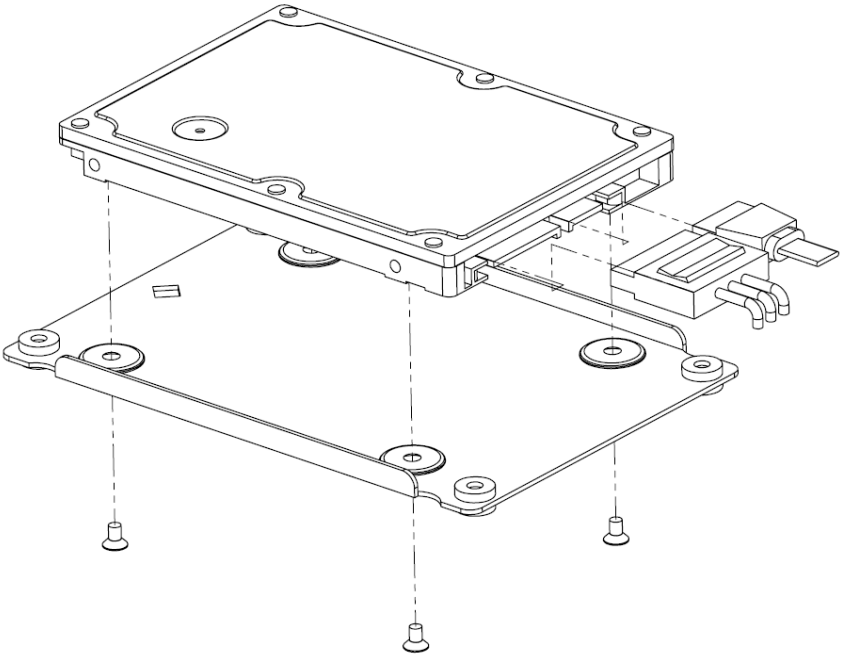
Step 2. Place the thermal pads onto the RAM modules as instructed below.



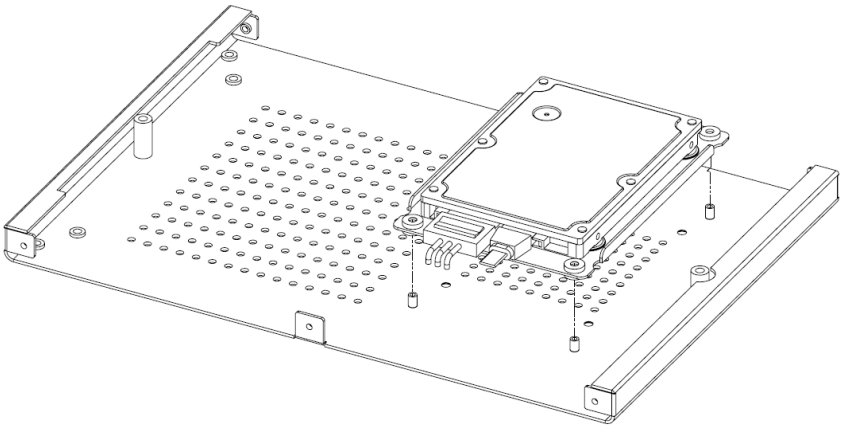
## 2.9 2.5" SATA Drive Installation

- Turn off the system, unplug the power cord to make sure the system is power off.

Step 1: Use the HDD screws provided to assemble 2.5" SATA drive with the HDD Bracket



Step 2: Assemble the 2.5" HDD Driver kit with bottom case and connect the SATA signal cable and SATA power cable with the 2.5" SATA HDD Drive.

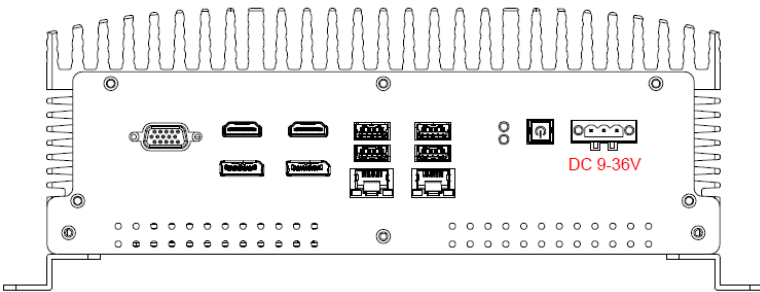


## 2.10 Power Connector Installation

Step 1: Take out 3-pin green phoenix power connector from the accessory kit



Step 2: Refer to below power pin out



# Chapter 3

---

AMI BIOS Setup



## 3.1 System Test and Initialization

---

The system uses certain routines to perform testing and initialization. If an error, fatal or non-fatal, is encountered, a few short beeps or an error message will be outputted. The board can usually continue the boot up sequence with non-fatal errors.

The system configuration verification routines check the current system configuration against the values stored in the CMOS memory. If they do not match, an error message will be outputted, in which case you will need to run the BIOS setup program to set the configuration information in memory.

There are three situations in which you will need to change the CMOS settings:

- You are starting your system for the first time
- You have changed your system's hardware
- The CMOS memory has lost power and the configuration information is erased

The system's CMOS memory uses a backup battery for data retention, which is to be replaced once emptied.

## 3.2 AMI BIOS Setup

---

The AMI BIOS ROM has a pre-installed Setup program that allows users to modify basic system configurations, which is stored in the battery-backed CMOS RAM and BIOS NVRAM so that the information is retained when the power is turned off.

To enter BIOS Setup, press <Del> or <F2> immediately while your computer is powering up.

The function for each interface can be found below.

**Main** – Date and time can be set here. Press <Tab> to switch between date elements

**Advanced** – Enable/ Disable boot option for legacy network devices

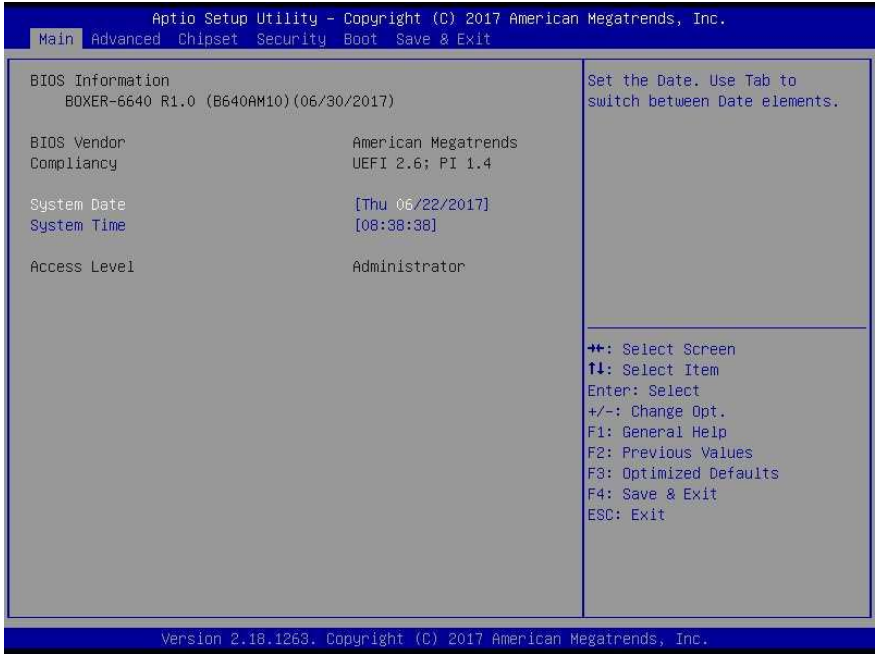
**Chipset** – For hosting bridge parameters

**Boot** – Enable/ Disable quiet Boot Option

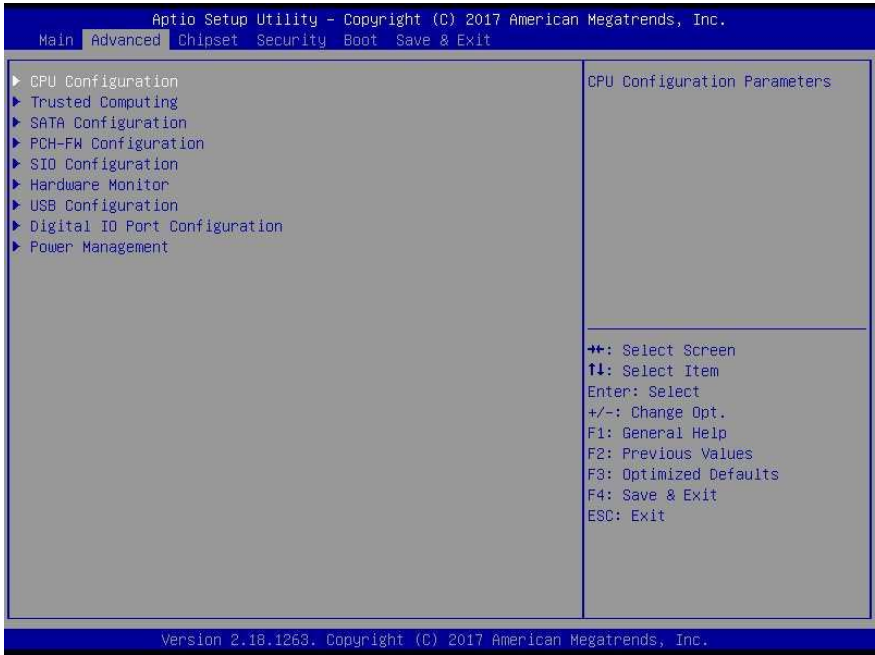
**Security** – The setup administrator password can be set here

**Save & Exit** – Save your changes and exit the program

### 3.3 Setup Submenu: Main



### 3.4 Setup Submenu: Advanced



### 3.4.1 Advanced: CPU Configuration



**Options summary:**

Hyper-Threading	Disabled	
	Enabled	Optimal Default, Failsafe Default
Enabled for Windows XP and Linux (OS optimized for Hyper-Threading Technology) and Disabled for other OS (OS not optimized for Hyper-Threading Technology).		
Intel (VMX) Virtualization Technology	Disabled	
	Enabled	Optimal Default, Failsafe Default
When enabled, a VMM can utilize the additional hardware capabilities provided by Vanderpool Technology.		
Active Processor Cores	1	
	All	Optimal Default, Failsafe Default
Number of cores to enable in each processor package.		

### 3.4.2 Advanced: SATA Configuration



#### Options summary:

SATA Controller(s)	Enabled	Optimal Default, Failsafe Default
	Disabled	
Enable or Disable SATA Device.		
SATA Mode Selection	AHCI Mode	Optimal Default, Failsafe Default
Determines how SATA controller(s) operate.		
Port 1/2, Mini-Card	Enabled	Optimal Default, Failsafe Default
	Disabled	
Enable or Disable SATA Port.		
Hot Plug	Enabled	
	Disabled	Optimal Default, Failsafe Default
Designates this port as Hot Pluggable.		

### 3.4.3 Advanced: PCH-FW Configuration



### 3.4.3.1 PCH-FW Configuration: Firmware Update Configuration



**Options summary:**

ME FW Image Re-Flash	Enabled	Optimal Default, Failsafe Default
	Disabled	
Enable or Disable ME FW Image Re-Flash function.		



### 3.4.4 Advanced: SIO Configuration



### 3.4.4.1 SIO Configuration: Serial Port 1 Configuration



#### Options summary:

Use This Device	Disabled	Optimal Default, Failsafe Default
	Enabled	
Enable or Disable Serial Port (COM)		
Possible:	Use Automatic Settings	Optimal Default, Failsafe Default
	IO=2F8; IRQ=3;	
	IO=3F8; IRQ=4;	
Select an optimal setting for IO device		
Mode:	RS232	Optimal Default, Failsafe Default
	RS422	
	RS485	
UART RS232, 422, 485 selection		

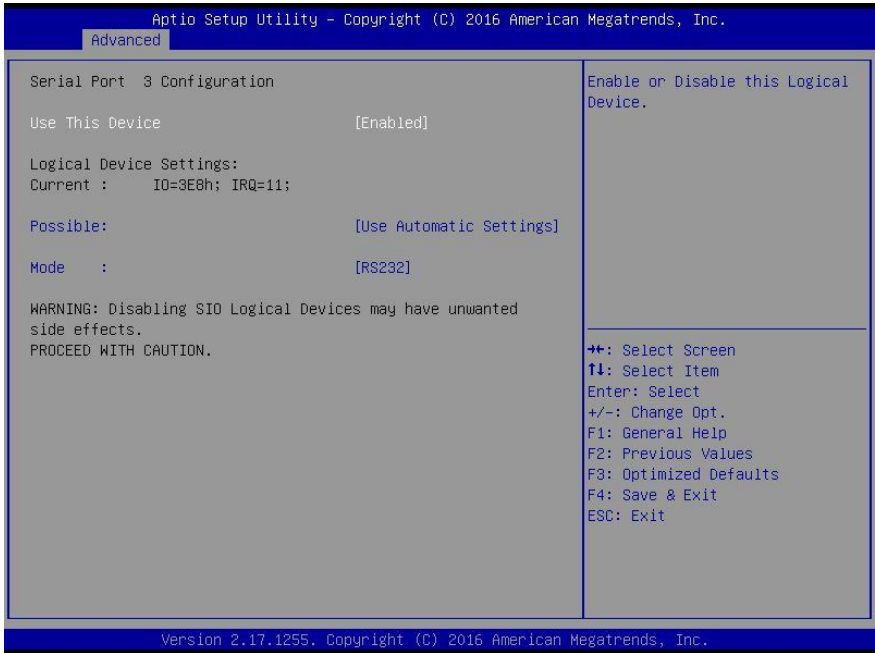
### 3.4.4.2 SIO Configuration: Serial Port 2 Configuration



#### Options summary:

Use This Device	Disabled	Optimal Default, Failsafe Default
	Enabled	
Enable or Disable Serial Port (COM)		
Possible:	Use Automatic Settings	Optimal Default, Failsafe Default
	IO=2F8; IRQ=3;	
	IO=3F8; IRQ=4;	
Select an optimal setting for IO device		

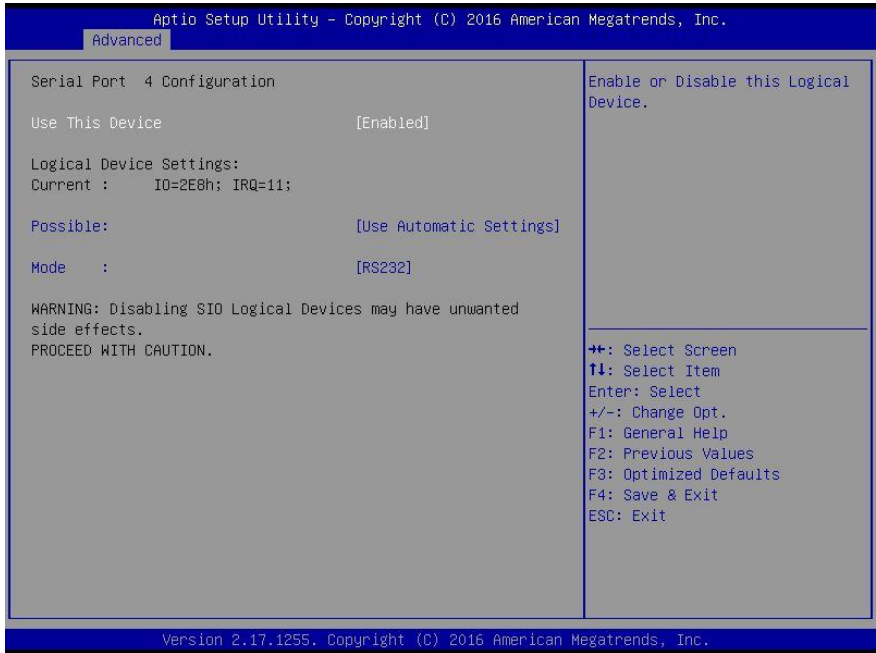
### 3.4.4.3 SIO Configuration: Serial Port 3 Configuration



#### Options summary:

Use This Device	Disabled	Optimal Default, Failsafe Default
	Enabled	
Enable or Disable Serial Port (COM)		
Possible:	Use Automatic Settings	Optimal Default, Failsafe Default
	IO=2F8; IRQ=11;	
	IO=3F8; IRQ=11;	
Select an optimal setting for IO device		

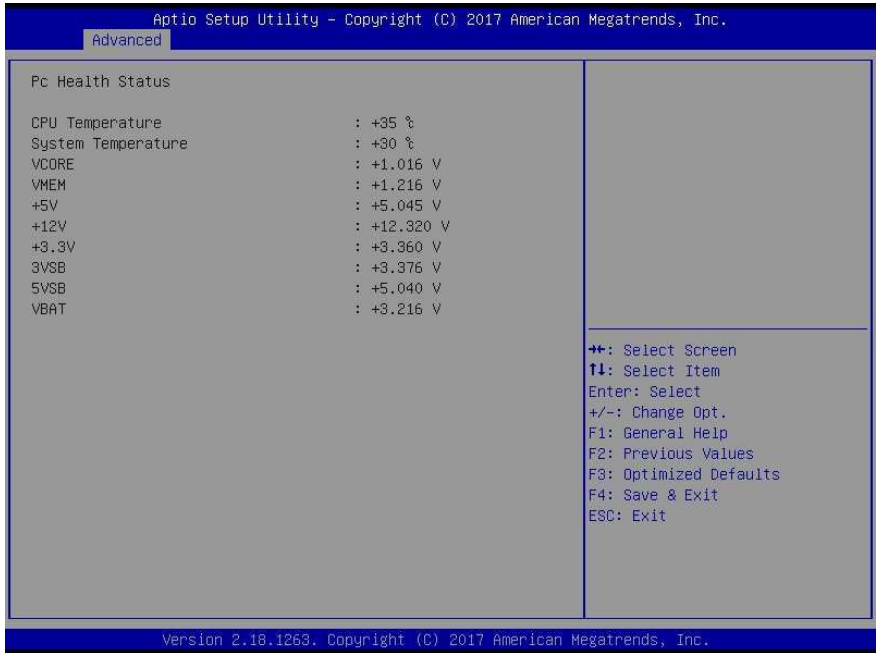
### 3.4.4.4 SIO Configuration: Serial Port 4 Configuration



#### Options summary:

Use This Device	Disabled	Optimal Default, Failsafe Default
	Enabled	
Enable or Disable Serial Port (COM)		
Possible:	Use Automatic Settings	Optimal Default, Failsafe Default
	IO=2F8; IRQ=11;	
	IO=3F8; IRQ=11;	
Select an optimal setting for IO device		

### 3.4.5 Advanced: Hardware Monitor



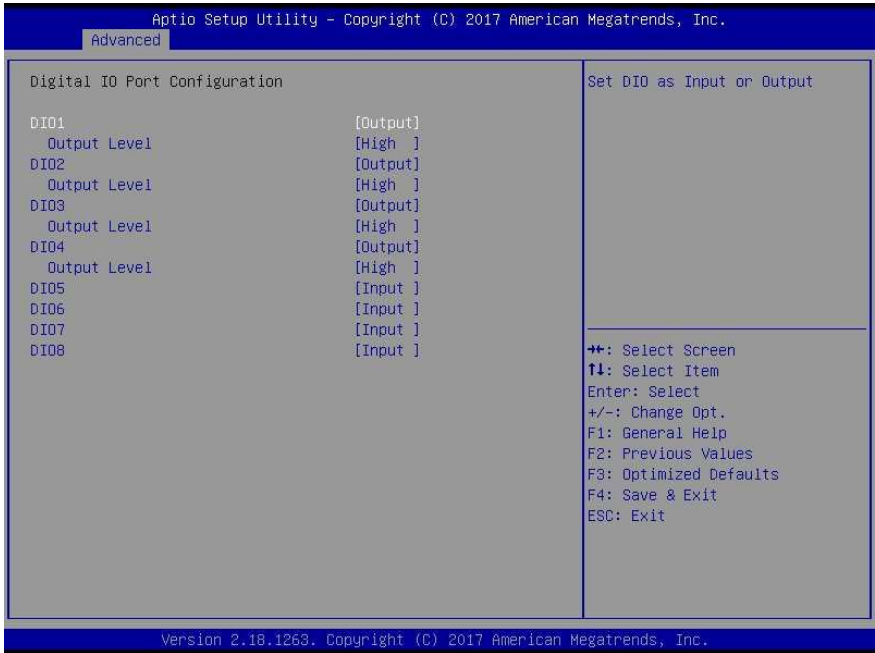
### 3.4.6 Advanced: USB Configuration



**Options summary:**

Legacy USB Support	Enabled	Optimal Default, Failsafe Default
	Disabled	
	Auto	
<p>Enables BIOS Support for Legacy USB Support. When enabled, USB can be functional in legacy environment like DOS.          AUTO option disables legacy support if no USB devices are connected</p>		

### 3.4.7 Advanced: Digital IO Port Configuration



**Options summary:**

DIO Type	Output	Optimal Default, Failsafe Default
	Input	
DIO Direction Type Setting		
DIO Data	Low	Optimal Default, Failsafe Default
	High	
DIO Output High/Low Setting		



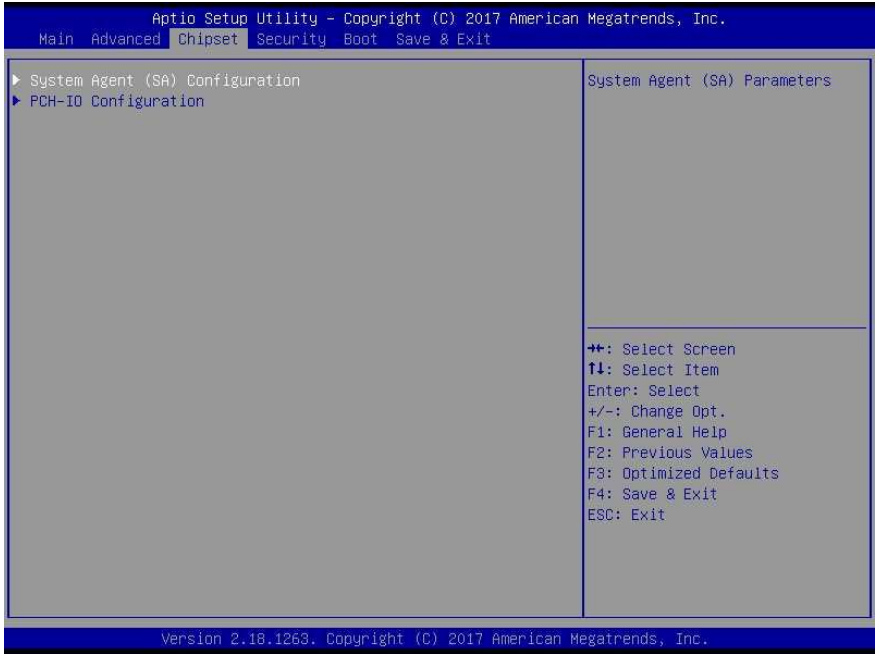
### 3.4.8 Advanced: Power Management



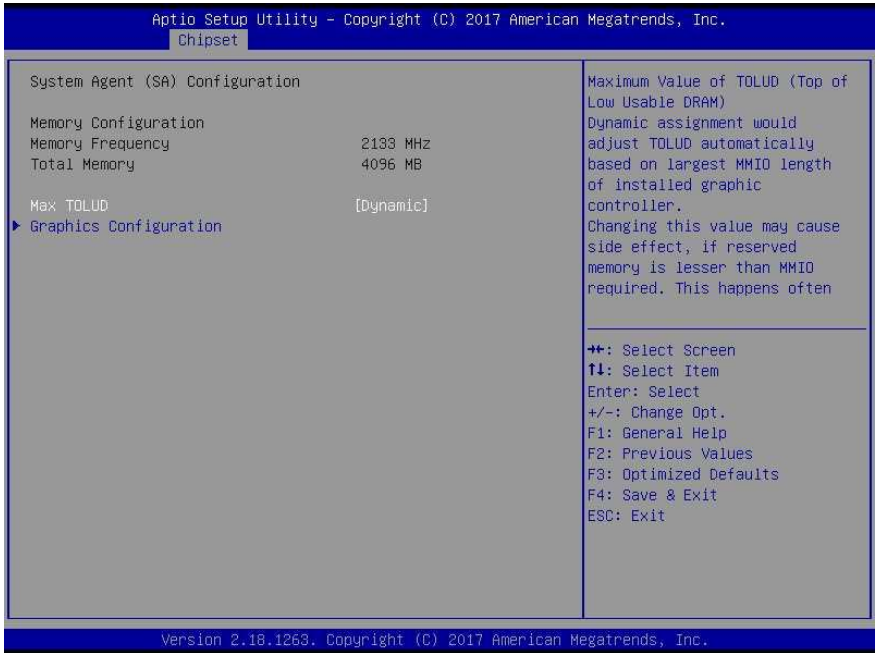
#### Options summary:

Power Mode	ATX Type	Optimal Default, Failsafe Default
	AT Type	
Select power supply mode.		
AC Power Loss	Last State	Optimal Default, Failsafe Default
	Power On	
	Power Off	
Select power state when power is re-applied after a power failure.		
RTC wake system from S5	Disabled	Optimal Default, Failsafe Default
	Fixed Time	
	Dynamic Time	
Enable or disable System wake on alarm event. When enabled, System will wake on the hr::min::sec specified		

### 3.5 Setup submenu: Chipset



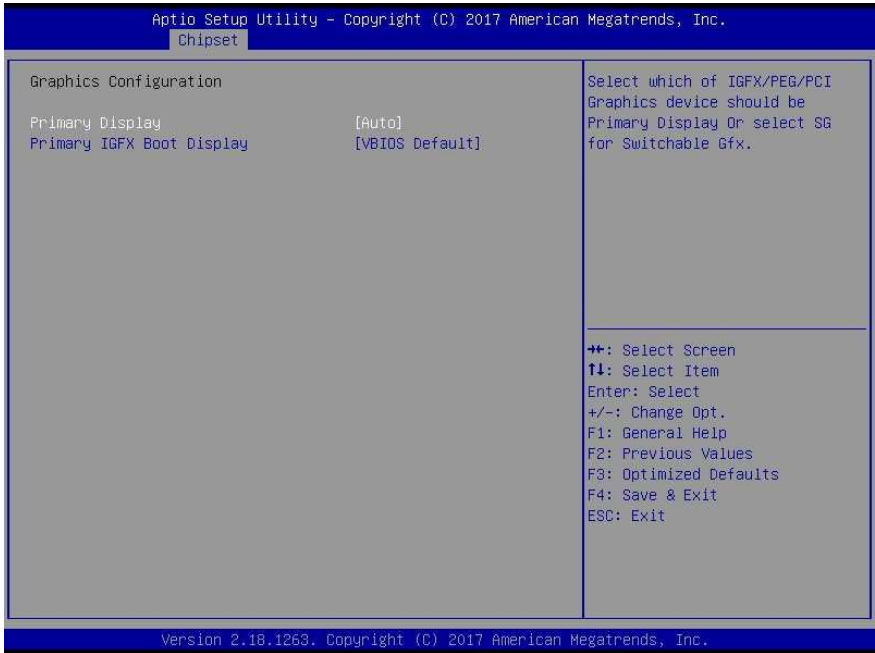
### 3.5.1 Chipset: System Agent (SA) Configuration



#### Options summary:

Max TOLUD	Dynamic	Optimal Default, Failsafe Default
	1 GB	
	1.25 GB	
	1.5 GB	
	1.75 GB	
	2 GB	
	2.25 GB	
	2.5 GB	
	2.75 GB	
	3 GB	
	3.25 GB	
	3.5 GB	
Maximum Value of TOLUD. Dynamic assignment would adjust TOLUD automatically based on largest MMIO length of installed graphic controller.		

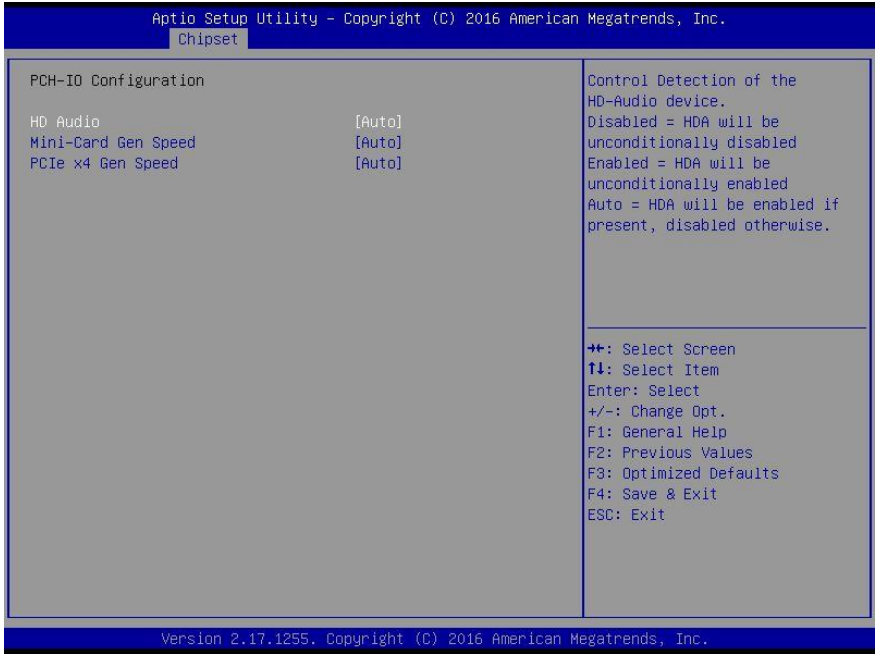
### 3.5.1.1 System Agent (SA) Configuration: Graphics Configuration



#### Options summary:

Primary Display	Auto	Optimal Default, Failsafe Default
	IGFX	
	PCI-E	
Primary IGFX Boot Display	VBIOS default	Optimal Default, Failsafe Default
	HDMI/DP 1	
	CRT	
	HDMI/DP 2	
Secondary IGFX Boot Display	Disable	Optimal Default, Failsafe Default
	HDMI/DP 1	
	CRT	
	HDMI/DP 2	

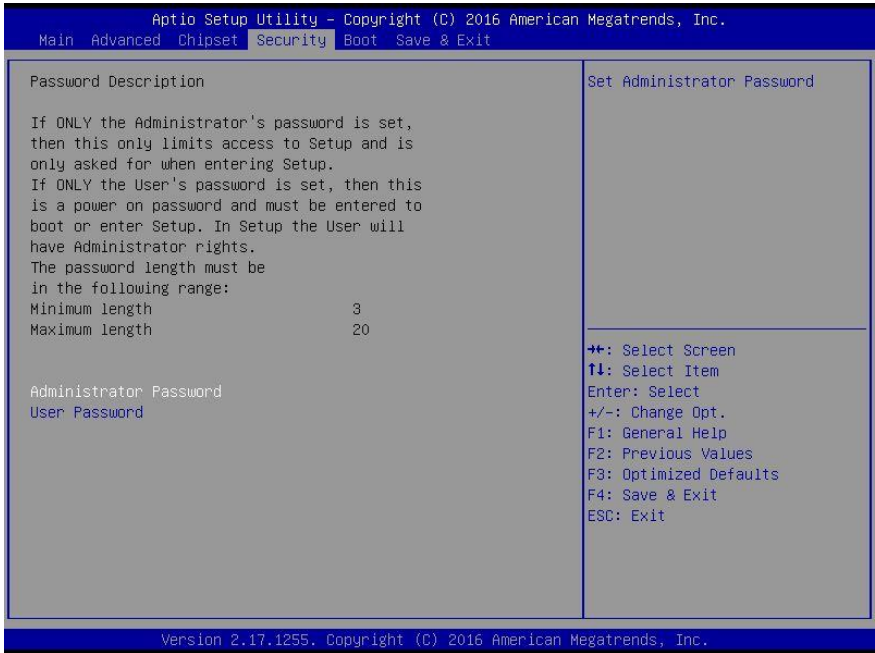
### 3.5.2 Chipset: PCH-IO Configuration



#### Options summary:

HD Audio	Disabled	Optimal Default, Failsafe Default
	Enabled	
	Auto	
Control Detection of the HD-Audio device.		
Mini-Card Gen Speed	Auto	Optimal Default, Failsafe Default
	Gen1	
	Gen2	
	Gen3	
Select PCI Express port speed		
PCIe x4 Gen Speed	Auto	Optimal Default, Failsafe Default
	Gen1	
	Gen2	
	Gen3	
Select PCI Express port speed		

## 3.6 Setup submenu: Security



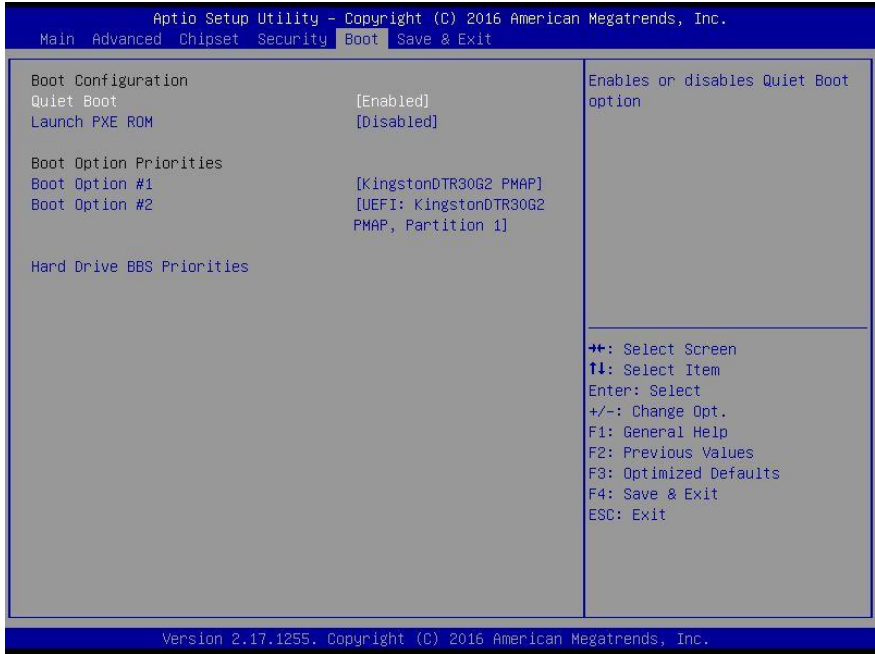
### Change User/Administrator Password

You can set a User Password once an Administrator Password is set. The password will be required during boot up, or when the user enters the Setup utility. Please Note that a User Password does not provide access to many of the features in the Setup utility. Select the password you wish to set, press Enter to open a dialog box to enter your password (you can enter no more than six letters or numbers). Press Enter to confirm your entry, after which you will be prompted to retype your password for a final confirmation. Press Enter again after you have retyped it correctly.

### Removing the Password

Highlight this item and type in the current password. At the next dialog box press Enter to disable password protection.

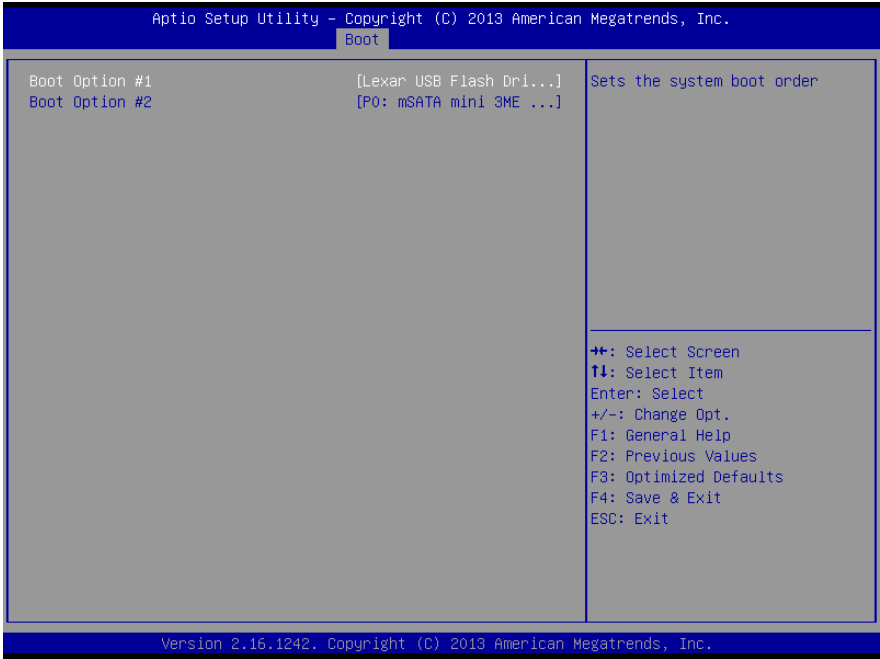
### 3.7 Setup submenu: Boot



#### Options summary:

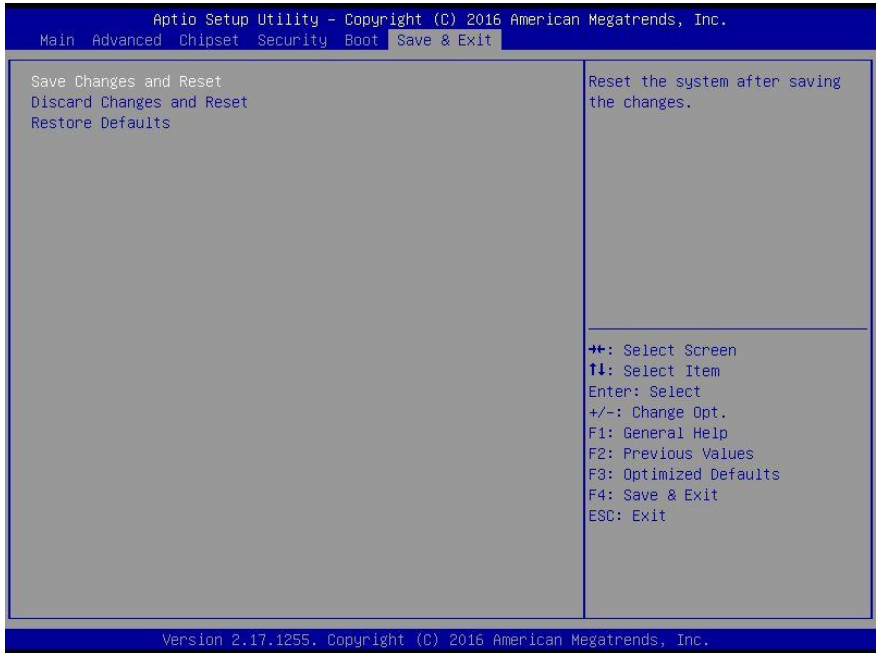
Quiet Boot	Disabled	Optimal Default, Failsafe Default
	Enabled	
Enables or disables Quiet Boot option.		
Launch PXE OpROM	Disabled	Optimal Default, Failsafe Default
	Enabled	
Controls the execution of UEFI and Legacy PXE OpROM.		

### 3.8 Boot: BBS Priorities





### 3.9 Setup submenu: Save & Exit



# Chapter 4

---

Drivers Installation

## 4.1 Product CD/DVD

---

The BOXER-6640 comes with a product DVD that contains all the drivers and utilities you need to setup your product. Insert the DVD and follow the steps in the autorun program to install the drivers.

In case the program does not start, follow the sequence below to install the drivers.

### Step 1 – Install Chipset Driver

1. Open the **Step1 - Chipset** folder and select your OS
2. Open the **SetupChipset.exe** file in the folder
3. Follow the instructions
4. Drivers will be installed automatically

### Step 2 – Install Graphics Driver

1. Open the **Step2 - Graphic** folder and select your OS
2. Open the **Setup.exe** file in the folder
3. Follow the instructions
4. Drivers will be installed automatically

### Step 3 – Install LAN Driver

1. Open the **Step3 - LAN** folder and select your OS
2. Open the **.exe** file in the folder
3. Follow the instructions
4. Drivers will be installed automatically

#### Step 4 – Install Audio Driver

1. Open the **Step4 - Audio** folder and select your OS
2. followed by the **.exe** file in the folder
3. Follow the instructions
4. Drivers will be installed automatically

#### Step 5 – Install USB3.0 Driver

1. Open the **Step5 – USB3.0** folder and select your OS
2. Open the **.exe** file in the folder
3. Follow the instructions
4. Drivers will be installed automatically

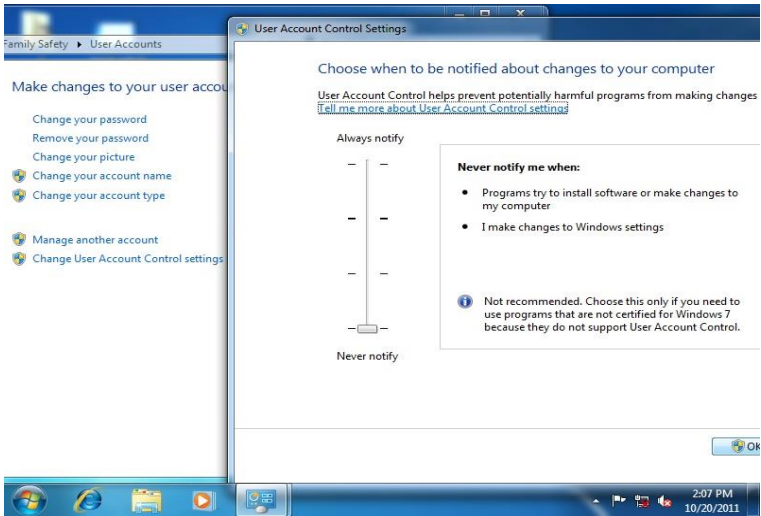
#### Step 6 – Install ME Driver

1. Open the **Step6 - ME** folder and select your OS
2. Open the **SetupME.exe** file in the folder
3. Follow the instructions
4. Drivers will be installed automatically

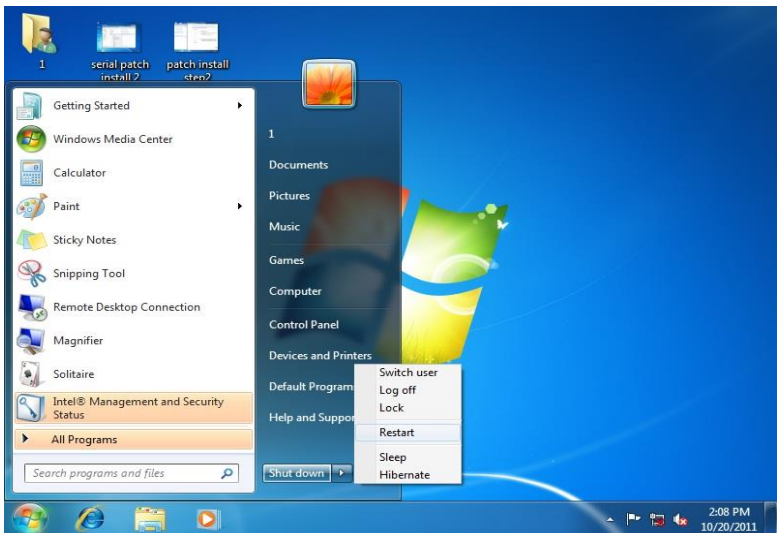
## Step 7 – Install Serial Port Driver (Optional)

For Windows 7:

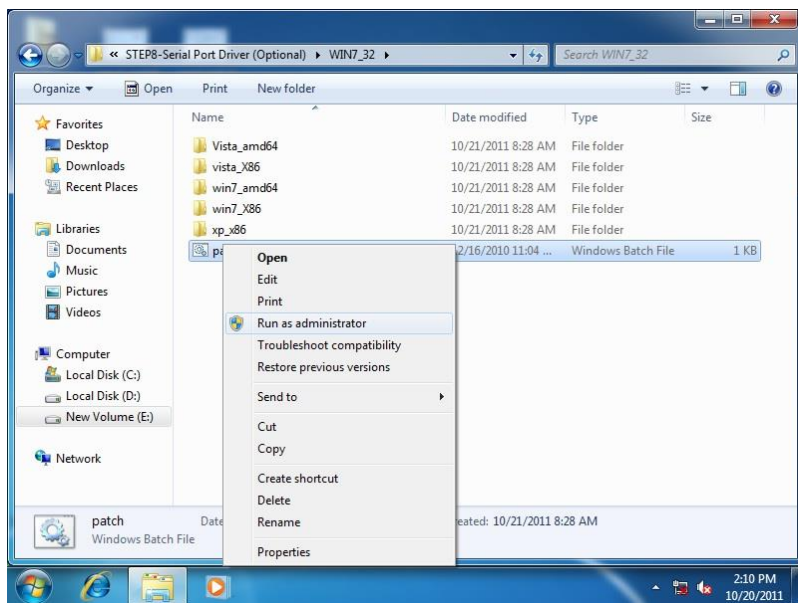
1. Change User Account Control settings to **Never notify**



2. Reboot and log in as administrator



3. Run **patch.bat** as administrator



For Windows 8 and Windows 10:

1. Open the **Step 7 - Serial Port Driver (Optional)** folder and select your OS
2. Open the **Setup.exe** file in the folder
3. Follow the instructions
4. Drivers will be installed automatically

# Appendix A

---

## Watchdog Timer Programming

## A.1 Watchdog Timer Initial Program

Table 1 : SuperIO relative register table		
	Default Value	Note
Index	0x2E(Note1)	SIO MB PnP Mode Index Register 0x2E or 0x4E
Data	0x2F(Note2)	SIO MB PnP Mode Data Register 0x2F or 0x4F

Table 2 : Watchdog relative register table					
	LDN	Register	BitNum	Value	Note
Timer Counter	0x07(Note3)	0xF6(Note4)		(Note24)	Time of watchdog timer (0~255) This register is byte access
Counting Unit	0x07(Note5)	0xF5(Note6)	3(Note7)	0(Note8)	Select time unit. 0: second 1: minute
Watchdog Enable	0x07(Note9)	0xF5(Note10)	5(Note11)	1(Note12)	0: Disable 1: Enable
Timeout Status	0x07(Note13)	0xF5(Note14)	6(Note15)	1	1: Clear timeout status
Output Mode	0x07(Note16)	0xF5(Note17)	4(Note18)	1(Note19)	Select WDRST# output mode 0: level 1: pulse
WDRST output	0x07(Note20)	0xFA(Note21)	0(Note22)	1(Note23)	Enable/Disable time out output via WDRST# 0: Disable 1: Enable



```

*****
// SuperIO relative definition (Please reference to Table 1)
#define byte SIOIndex //This parameter is represented from Note1
#define byte SIOData //This parameter is represented from Note2
#define void IOWriteByte(byte IOPort, byte Value);
#define byte IOReadByte(byte IOPort);
// Watch Dog relative definition (Please reference to Table 2)
#define byte TimerLDN //This parameter is represented from Note3
#define byte TimerReg //This parameter is represented from Note4
#define byte TimerVal // This parameter is represented from Note24
#define byte UnitLDN //This parameter is represented from Note5
#define byte UnitReg //This parameter is represented from Note6
#define byte UnitBit //This parameter is represented from Note7
#define byte UnitVal //This parameter is represented from Note8
#define byte EnableLDN //This parameter is represented from Note9
#define byte EnableReg //This parameter is represented from Note10
#define byte EnableBit //This parameter is represented from Note11
#define byte EnableVal //This parameter is represented from Note12
#define byte StatusLDN // This parameter is represented from Note13
#define byte StatusReg // This parameter is represented from Note14
#define byte StatusBit // This parameter is represented from Note15
#define byte ModeLDN // This parameter is represented from Note16
#define byte ModeReg // This parameter is represented from Note17
#define byte ModeBit // This parameter is represented from Note18
#define byte ModeVal // This parameter is represented from Note19
#define byte WDRstLDN // This parameter is represented from Note20
#define byte WDRstReg // This parameter is represented from Note21
#define byte WDRstBit // This parameter is represented from Note22
#define byte WDRstVal // This parameter is represented from Note23
*****

```

```
*****
VOID Main() {
    // Procedure : AaeonWDTConfig
    // (byte)Timer : Time of WDT timer.(0x00~0xFF)
    // (boolean)Unit : Select time unit(0: second, 1: minute).
    AaeonWDTConfig();

    // Procedure : AaeonWDTEnable
    // This procedure will enable the WDT counting.
    AaeonWDTEnable();
}
*****
```

```

*****
// Procedure : AaeonWDTEnable
VOID AaeonWDTEnable (){
    WDTEnableDisable(EnableLDN, EnableReg, EnableBit, 1);
}

// Procedure : AaeonWDTConfig
VOID AaeonWDTConfig (){
    // Disable WDT counting
    WDTEnableDisable(EnableLDN, EnableReg, EnableBit, 0);
    // Clear Watchdog Timeout Status
    WDTClearTimeoutStatus();
    // WDT relative parameter setting
    WDTParameterSetting();
}

VOID WDTEnableDisable(byte LDN, byte Register, byte BitNum, byte Value){
    SIOBitSet(LDN, Register, BitNum, Value);
}

VOID WDTParameterSetting(){
    // Watchdog Timer counter setting
    SIOByteSet(TimerLDN, TimerReg, TimerVal);
    // WDT counting unit setting
    SIOBitSet(UnitLDN, UnitReg, UnitBit, UnitVal);
    // WDT output mode setting, level / pulse
    SIOBitSet(ModeLDN, ModeReg, ModeBit, ModeVal);
    // Watchdog timeout output via WDTRST#
    SIOBitSet(WDTRstLDN, WDTRstReg, WDTRstBit, WDTRstVal);
}

VOID WDTClearTimeoutStatus(){
    SIOBitSet(StatusLDN, StatusReg, StatusBit, 1);
}
*****

```

```

*****
VOID SIOEnterMBPnPMode(){
    IOWriteByte(SIOIndex, 0x87);
    IOWriteByte(SIOIndex, 0x87);
}

VOID SIOExitMBPnPMode(){
    IOWriteByte(SIOIndex, 0xAA);
}

VOID SIOSelectLDN(byte LDN){
    IOWriteByte(SIOIndex, 0x07); // SIO LDN Register Offset = 0x07
    IOWriteByte(SIOData, LDN);
}

VOID SIOBitSet(byte LDN, byte Register, byte BitNum, byte Value){
    Byte TmpValue;

    SIOEnterMBPnPMode();
    SIOSelectLDN(byte LDN);
    IOWriteByte(SIOIndex, Register);
    TmpValue = IOReadByte(SIOData);
    TmpValue &= ~(1 << BitNum);
    TmpValue |= (Value << BitNum);
    IOWriteByte(SIOData, TmpValue);
    SIOExitMBPnPMode();
}

VOID SIOByteSet(byte LDN, byte Register, byte Value){
    SIOEnterMBPnPMode();
    SIOSelectLDN(LDN);
    IOWriteByte(SIOIndex, Register);
    IOWriteByte(SIOData, Value);
    SIOExitMBPnPMode();
}
*****

```

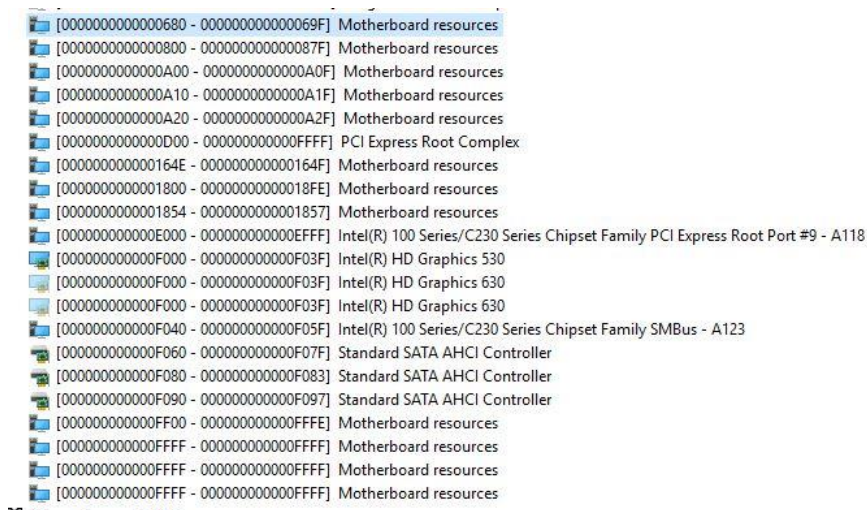
# Appendix B

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I/O Information

## B.1 I/O Address Map














Input/output (IO)	
[0000000000000000 - 000000000000CF7]	PCI Express Root Complex
[0000000000000020 - 0000000000000021]	Programmable interrupt controller
[0000000000000024 - 0000000000000025]	Programmable interrupt controller
[0000000000000028 - 0000000000000029]	Programmable interrupt controller
[000000000000002C - 000000000000002D]	Programmable interrupt controller
[000000000000002E - 000000000000002F]	Motherboard resources
[0000000000000030 - 0000000000000031]	Programmable interrupt controller
[0000000000000034 - 0000000000000035]	Programmable interrupt controller
[0000000000000038 - 0000000000000039]	Programmable interrupt controller
[000000000000003C - 000000000000003D]	Programmable interrupt controller
[0000000000000040 - 0000000000000043]	System timer
[000000000000004E - 000000000000004F]	Motherboard resources
[0000000000000050 - 0000000000000053]	System timer
[0000000000000061 - 0000000000000061]	Motherboard resources
[0000000000000063 - 0000000000000063]	Motherboard resources
[0000000000000065 - 0000000000000065]	Motherboard resources
[0000000000000067 - 0000000000000067]	Motherboard resources
[0000000000000070 - 0000000000000070]	Motherboard resources
[0000000000000070 - 0000000000000077]	System CMOS/real time clock
[0000000000000080 - 0000000000000080]	Motherboard resources
[0000000000000092 - 0000000000000092]	Motherboard resources
[00000000000000A0 - 00000000000000A1]	Programmable interrupt controller
[00000000000000A4 - 00000000000000A5]	Programmable interrupt controller
[00000000000000A8 - 00000000000000A9]	Programmable interrupt controller
[00000000000000AC - 00000000000000AD]	Programmable interrupt controller
[00000000000000B0 - 00000000000000B1]	Programmable interrupt controller
[00000000000000B2 - 00000000000000B3]	Motherboard resources
[00000000000000B4 - 00000000000000B5]	Programmable interrupt controller
[00000000000000B8 - 00000000000000B9]	Programmable interrupt controller
[00000000000000BC - 00000000000000BD]	Programmable interrupt controller
[00000000000000F0 - 00000000000000F0]	Numeric data processor
[00000000000002E8 - 00000000000002EF]	Communications Port (COM4)
[00000000000002F8 - 00000000000002FF]	Communications Port (COM2)
[00000000000003B0 - 00000000000003BB]	Intel(R) HD Graphics 530
[00000000000003C0 - 00000000000003DF]	Intel(R) HD Graphics 530
[00000000000003E8 - 00000000000003EF]	Communications Port (COM3)
[00000000000003F8 - 00000000000003FF]	Communications Port (COM1)
[00000000000004D0 - 00000000000004D1]	Programmable interrupt controller
[0000000000000680 - 000000000000069F]	Motherboard resources



[0000000000000680 - 00000000000069F]	Motherboard resources
[000000000000800 - 00000000000087F]	Motherboard resources
[000000000000A00 - 000000000000A0F]	Motherboard resources
[000000000000A10 - 000000000000A1F]	Motherboard resources
[000000000000A20 - 000000000000A2F]	Motherboard resources
[000000000000D00 - 000000000000FFFF]	PCI Express Root Complex
[00000000000164E - 00000000000164F]	Motherboard resources
[000000000001800 - 0000000000018FE]	Motherboard resources
[000000000001854 - 000000000001857]	Motherboard resources
[00000000000E000 - 00000000000EFFF]	Intel(R) 100 Series/C230 Series Chipset Family PCI Express Root Port #9 - A118
[00000000000F000 - 00000000000F03F]	Intel(R) HD Graphics 530
[00000000000F000 - 00000000000F03F]	Intel(R) HD Graphics 630
[00000000000F000 - 00000000000F03F]	Intel(R) HD Graphics 630
[00000000000F040 - 00000000000F05F]	Intel(R) 100 Series/C230 Series Chipset Family SMBus - A123
[00000000000F060 - 00000000000F07F]	Standard SATA AHCI Controller
[00000000000F080 - 00000000000F083]	Standard SATA AHCI Controller
[00000000000F090 - 00000000000F097]	Standard SATA AHCI Controller
[00000000000FF00 - 00000000000FFFE]	Motherboard resources
[00000000000FFFF - 00000000000FFFF]	Motherboard resources
[00000000000FFFF - 00000000000FFFF]	Motherboard resources
[00000000000FFFF - 00000000000FFFF]	Motherboard resources

## B.3 IRQ Mapping Chart

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▼		Interrupt request (IRQ)	
		(ISA) 0x00000000 (00)	System timer
		(ISA) 0x00000003 (03)	Communications Port (COM2)
		(ISA) 0x00000004 (04)	Communications Port (COM1)
		(ISA) 0x00000005 (05)	Intel(R) Ethernet Connection (2) I219-LM
		(ISA) 0x00000005 (05)	Intel(R) HD Graphics 630
		(ISA) 0x00000005 (05)	Intel(R) HD Graphics 630
		(ISA) 0x00000005 (05)	Intel(R) I211 Gigabit Network Connection
		(ISA) 0x00000008 (08)	System CMOS/real time clock
		(ISA) 0x0000000B (11)	Communications Port (COM3)
		(ISA) 0x0000000B (11)	Communications Port (COM4)
		(ISA) 0x0000000D (13)	Numeric data processor
		(ISA) 0x0000000E (14)	Motherboard resources



# Appendix C

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Electrical Specifications for I/O Ports

## C.1 DIO Programming

---

BOXER-6640 utilizes FINTEK 81866 chipset as its Digital I/O controller.

Below are the procedures to complete its configuration and the AAEON initial watchdog timer program is also attached based on which you can develop customized program to fit your application.

There are three steps to complete the configuration setup: (1) Enter the MB PnP Mode; (2) Modify the data of configuration registers; (3) Exit the MB PnP Mode. Undesired result may occur if the MB PnP Mode is not exited normally.(These three steps are the same as programming WDT)

## C.2 DIO Register

Table 1 : SuperIO relative register table		
	Default Value	Note
Index	0x2E(Note1)	SIO MB PnP Mode Index Register 0x2E or 0x4E
Data	0x2F(Note2)	SIO MB PnP Mode Data Register 0x2F or 0x4F

Table 2 : Digital Input relative register table					
	LDN	Register	BitNum	Value	Note
DIO-1 Pin Status	0x06(Note3)	0xA2(Note4)	0(Note5)		GPIO50
DIO-2 Pin Status	0x06(Note6)	0xA2(Note7)	1(Note8)		GPIO51
DIO-3 Pin Status	0x06(Note9)	0xA2(Note10)	2(Note11)		GPIO52
DIO-4 Pin Status	0x06(Note12)	0xA2(Note13)	3(Note14)		GPIO53
DIO-5 Pin Status	0x06(Note15)	0xA2(Note16)	4(Note17)		GPIO54
DIO-6 Pin Status	0x06(Note18)	0xA2(Note19)	5(Note20)		GPIO55
DIO-7 Pin Status	0x06(Note21)	0xA2(Note22)	6(Note23)		GPIO56
DIO-8 Pin Status	0x06(Note24)	0xA2(Note25)	7(Note26)		GPIO57

Table 3 : Digital Output relative register table					
	LDN	Register	BitNum	Value	Note
DIO-1 Output Data	0x06(Note27)	0xA1(Note28)	0(Note29)	(Note30)	GPIO50
DIO-2 Output Data	0x06(Note31)	0xA1(Note32)	1(Note33)	(Note34)	GPIO51
DIO-3 Output Data	0x06(Note35)	0xA1(Note36)	2(Note37)	(Note38)	GPIO52
DIO-4 Output Data	0x06(Note39)	0xA1(Note40)	3(Note41)	(Note42)	GPIO53
DIO-5 Output Data	0x06(Note43)	0xA1(Note44)	4(Note45)	(Note46)	GPIO54
DIO-6 Output Data	0x06(Note47)	0xA1(Note48)	5(Note49)	(Note50)	GPIO55
DIO-7 Output Data	0x06(Note51)	0xA1(Note52)	6(Note53)	(Note54)	GPIO56
DIO-8 Output Data	0x06(Note55)	0xA1(Note56)	7(Note57)	(Note58)	GPIO57

### C.3 DIO Sample Program

---

```
*****
// SuperIO relative definition (Please reference to Table 1)
#define byte SIOIndex //This parameter is represented from Note1
#define byte SIOData //This parameter is represented from Note2
#define void IOWriteByte(byte IOPort, byte Value);
#define byte IOReadByte(byte IOPort);
// Digital Input Status relative definition (Please reference to Table 2)
#define byte DInput1LDN // This parameter is represented from Note3
#define byte DInput1Reg // This parameter is represented from Note4
#define byte DInput1Bit // This parameter is represented from Note5
#define byte DInput2LDN // This parameter is represented from Note6
#define byte DInput2Reg // This parameter is represented from Note7
#define byte DInput2Bit // This parameter is represented from Note8
#define byte DInput3LDN // This parameter is represented from Note9
#define byte DInput3Reg // This parameter is represented from Note10
#define byte DInput3Bit // This parameter is represented from Note11
#define byte DInput4LDN // This parameter is represented from Note12
#define byte DInput4Reg // This parameter is represented from Note13
#define byte DInput4Bit // This parameter is represented from Note14
#define byte DInput5LDN // This parameter is represented from Note15
#define byte DInput5Reg // This parameter is represented from Note16
#define byte DInput5Bit // This parameter is represented from Note17
#define byte DInput6LDN // This parameter is represented from Note18
#define byte DInput6Reg // This parameter is represented from Note19
#define byte DInput6Bit // This parameter is represented from Note20
#define byte DInput7LDN // This parameter is represented from Note21
#define byte DInput7Reg // This parameter is represented from Note22
#define byte DInput7Bit // This parameter is represented from Note23
#define byte DInput8LDN // This parameter is represented from Note24
#define byte DInput8Reg // This parameter is represented from Note25
#define byte DInput8Bit // This parameter is represented from Note26
*****
```

\*\*\*\*\*

```
// Digital Output control relative definition (Please reference to Table 3)
#define byte   DOutput1LDN // This parameter is represented from Note27
#define byte   DOutput1Reg // This parameter is represented from Note28
#define byte   DOutput1Bit // This parameter is represented from Note29
#define byte   DOutput1Val // This parameter is represented from Note30
#define byte   DOutput2LDN // This parameter is represented from Note31
#define byte   DOutput2Reg // This parameter is represented from Note32
#define byte   DOutput2Bit // This parameter is represented from Note33
#define byte   DOutput2Val // This parameter is represented from Note34
#define byte   DOutput3LDN // This parameter is represented from Note35
#define byte   DOutput3Reg // This parameter is represented from Note36
#define byte   DOutput3Bit // This parameter is represented from Note37
#define byte   DOutput3Val // This parameter is represented from Note38
#define byte   DOutput4LDN // This parameter is represented from Note39
#define byte   DOutput4Reg // This parameter is represented from Note40
#define byte   DOutput4Bit // This parameter is represented from Note41
#define byte   DOutput4Val // This parameter is represented from Note42
#define byte   DOutput5LDN // This parameter is represented from Note43
#define byte   DOutput5Reg // This parameter is represented from Note44
#define byte   DOutput5Bit // This parameter is represented from Note45
#define byte   DOutput5Val // This parameter is represented from Note46
#define byte   DOutput6LDN // This parameter is represented from Note47
#define byte   DOutput6Reg // This parameter is represented from Note48
#define byte   DOutput6Bit // This parameter is represented from Note49
#define byte   DOutput6Val // This parameter is represented from Note50
#define byte   DOutput7LDN // This parameter is represented from Note51
#define byte   DOutput7Reg // This parameter is represented from Note52
#define byte   DOutput7Bit // This parameter is represented from Note53
#define byte   DOutput7Val // This parameter is represented from Note54
#define byte   DOutput8LDN // This parameter is represented from Note55
#define byte   DOutput8Reg // This parameter is represented from Note56
#define byte   DOutput8Bit // This parameter is represented from Note57
#define byte   DOutput8Val // This parameter is represented from Note58
```

\*\*\*\*\*

```
*****
VOID Main() {
    Boolean PinStatus ;

    // Procedure : AaeonReadPinStatus
    // Input :
    //     Example, Read Digital I/O Pin 3 status
    // Output :
    //     InputStatus :
    //         0: Digital I/O Pin level is low
    //         1: Digital I/O Pin level is High
    PinStatus = AaeonReadPinStatus(DInput3LDN, DInput3Reg, DInput3Bit);

    // Procedure : AaeonSetOutputLevel
    // Input :
    //     Example, Set Digital I/O Pin 6 level
    AaeonSetOutputLevel(DOutput6LDN, DOutput6Reg, DOutput6Bit, DOutput6Val);
}
*****
```

```
*****
Boolean AaeonReadPinStatus(byte LDN, byte Register, byte BitNum){
    Boolean PinStatus ;

    PinStatus = SIOBitRead(LDN, Register, BitNum);
    Return PinStatus ;
}
VOID AaeonSetOutputLevel(byte LDN, byte Register, byte BitNum, byte Value){
    ConfigToOutputMode(LDN, Register, BitNum);
    SIOBitSet(LDN, Register, BitNum, Value);
}
*****
```

```

*****
VOID SIOEnterMBPnPMode(){
    IOWriteByte(SIOIndex, 0x87);
    IOWriteByte(SIOIndex, 0x87);
}

VOID SIOExitMBPnPMode(){
    IOWriteByte(SIOIndex, 0xAA);
}

VOID SIOSelectLDN(byte LDN){
    IOWriteByte(SIOIndex, 0x07); // SIO LDN Register Offset = 0x07
    IOWriteByte(SIOData, LDN);
}

VOID SIOBitSet(byte LDN, byte Register, byte BitNum, byte Value){
    Byte TmpValue;

    SIOEnterMBPnPMode();
    SIOSelectLDN(byte LDN);
    IOWriteByte(SIOIndex, Register);
    TmpValue = IOReadByte(SIOData);
    TmpValue &= ~(1 << BitNum);
    TmpValue |= (Value << BitNum);
    IOWriteByte(SIOData, TmpValue);
    SIOExitMBPnPMode();
}

VOID SIOByteSet(byte LDN, byte Register, byte Value){
    SIOEnterMBPnPMode();
    SIOSelectLDN(LDN);
    IOWriteByte(SIOIndex, Register);
    IOWriteByte(SIOData, Value);
    SIOExitMBPnPMode();
}
*****

```



```

*****
Boolean SIOBitRead(byte LDN, byte Register, byte BitNum){
    Byte TmpValue;

    SIOEnterMBPnPMode();
    SIOSelectLDN(LDN);
    IOWriteByte(SIOIndex, Register);
    TmpValue = IOReadByte(SIOData);
    TmpValue &= (1 << BitNum);
    SIOExitMBPnPMode();
    If(TmpValue == 0)
        Return 0;
    Return 1;
}

VOID ConfigToOutputMode(byte LDN, byte Register, byte BitNum){
    Byte TmpValue, OutputEnableReg;

    OutputEnableReg = Register-1;
    SIOEnterMBPnPMode();
    SIOSelectLDN(LDN);
    IOWriteByte(SIOIndex, OutputEnableReg);
    TmpValue = IOReadByte(SIOData);
    TmpValue |= (1 << BitNum);
    IOWriteByte(SIOData, OutputEnableReg);
    SIOExitMBPnPMode();
}
*****

```