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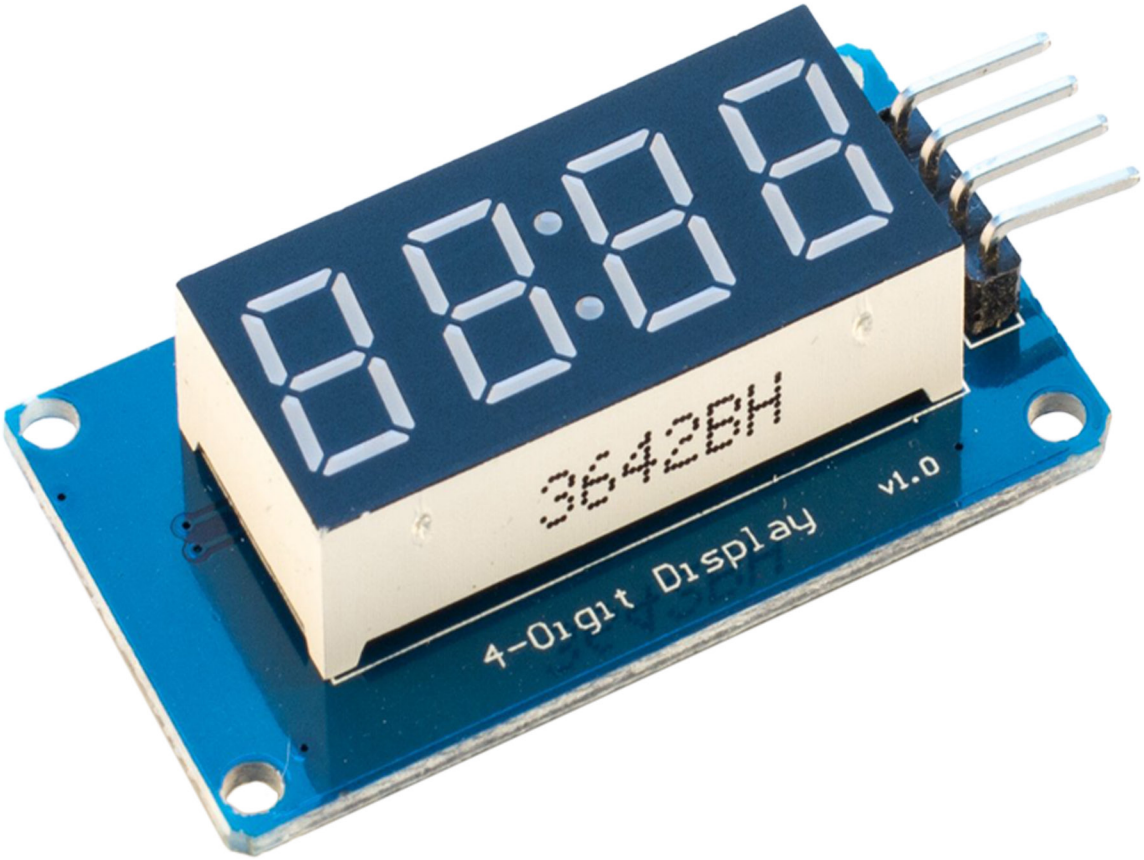
# 4 Digit 7 Segment Display Datenblatt

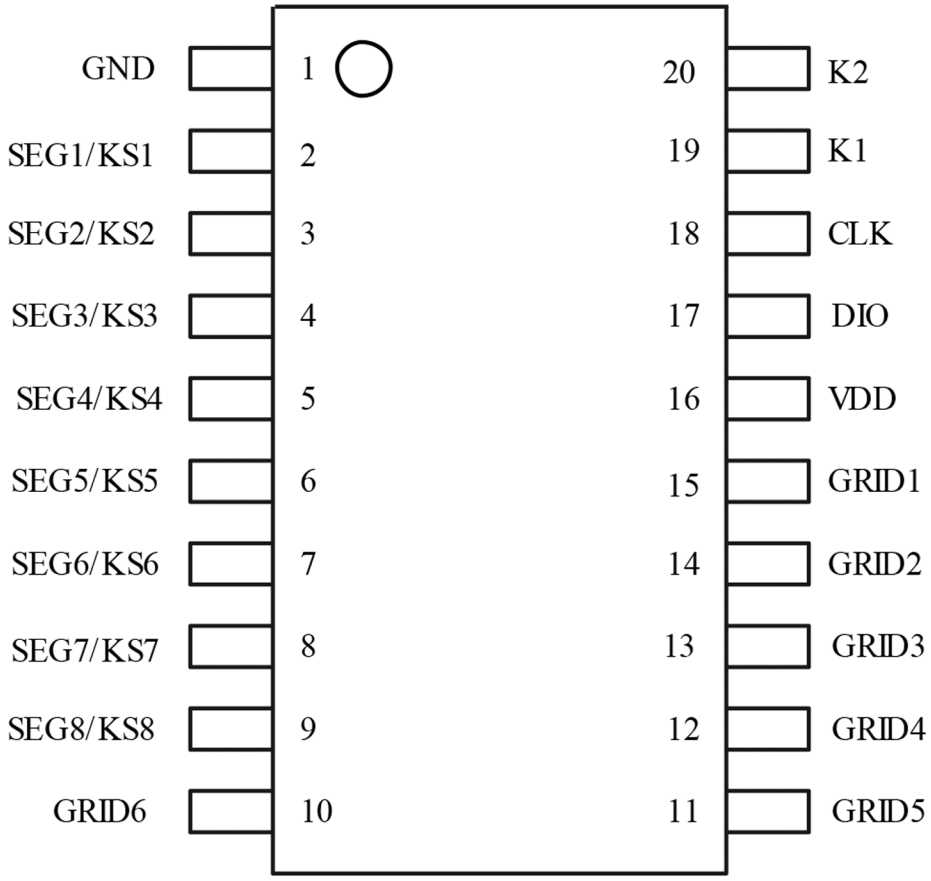


Contents:

## 1. Function features

- Applied power CMOS technique
- The display mode (8 segments*6 bit) supports output by common anode LED.
- Keyboard scan (8×2bit), with enhanced identification circuit with anti-interference keys
- Luminance adjustment circuit (adjustable 8 duty ratio)
- Two-wire serial interface (CLK, DIO)
- Oscillating type: Built-in RC oscillator
- Built-in power-on reset circuit
- Built-in automatic blanking circuit
- Package type: DIP20/SOP20

## 2. Pin information



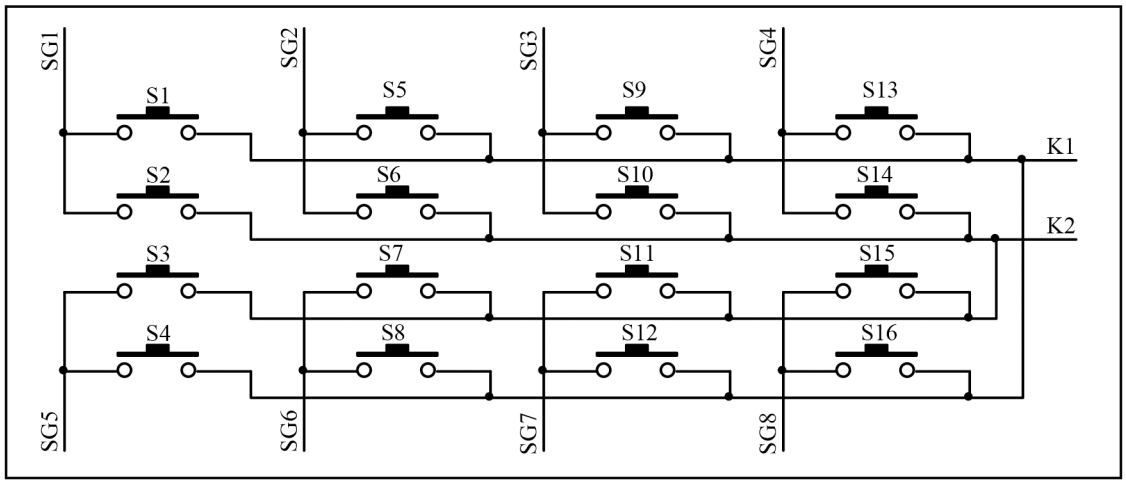
## 3. Pin functions

| Symbols | Pin name | Pin No. | Description |
|---|---|---|---|
| DIO | Data input/output | 17 | It is used for serial data input and output. The input data has a low level fluctuation while high level transfer at SCLK. Once one bit is transferred, one ACK is generated at failing edge of the 8th clock inside the chip. |
| CLK | Clock input | 18 | It is used for data input and output at rising edge. |
| K1~K2 | Data input by keyboard scan | 19-20 | Inputting the pin data here and it will be latched when the display cycle is over. |
| SG1~SG8 | Output (segment) | 2-9 | Segment Output (also keyboard scan) and N-channel open drain output |
| GRID6~GRID1 | Output (bit) | 10-15 | Bit output and P-channel open drain output |
| VDD | Logic Supply | 16 | Anode power connection |
| GND | logic ground | 1 | Grounding connection |

Electrostatic discharge led by much static at dry weather or environment could damage the integrated circuit. It is recommended for you to take every measure to protect integrated circuit. ESD damage or decreased performance by inappropriate operation or welding could lead to chip failure.

## 4. Read the key scan data

Key scan matrix of 8×2bit is shown as the following:




When a key is pressed, the key scan data is as follows: (Where low level is forward and high level is backward, 1110_1111 stands for 0xF7) .

| | SG1 | SG2 | SG3 | SG4 | SG5 | SG6 | SG7 | SG8 |
|---|---|---|---|---|---|---|---|---|
| K1 | 1110_1111 | 0110_1111 | 1010_1111 | 0010_1111 | 1100_1111 | 0100_1111 | 1000_1111 | 0000_1111 |
| K2 | 1111_0111 | 0111_0111 | 1011_0111 | 0011_0111 | 1101_0111 | 0101_0111 | 1001_0111 | 0001_0111 |

Note: Where there is no key pressed down, the key read data should be 1111_1111 with forward low level and backward high level. Since strong interference exists in the use of kitchen appliances, such as induction cooker, negative edge trigger mode was applied in TM1637 to avoid mistake trigger, which is also the called "key jumping". TM 1637 doesn't support combined key pressing.

## 5. Display register address

Stored data in the register is transferred to the TM1637 from outside elements by serial interface, with 6 bytes units of address from C0H to C5H in correspondence with the LED lights connected with SEG pin and GRID pin on the chip.LED data is displayed from low level to high level in respect of display address, and should be operated from low level to high level in respect of data bytes.

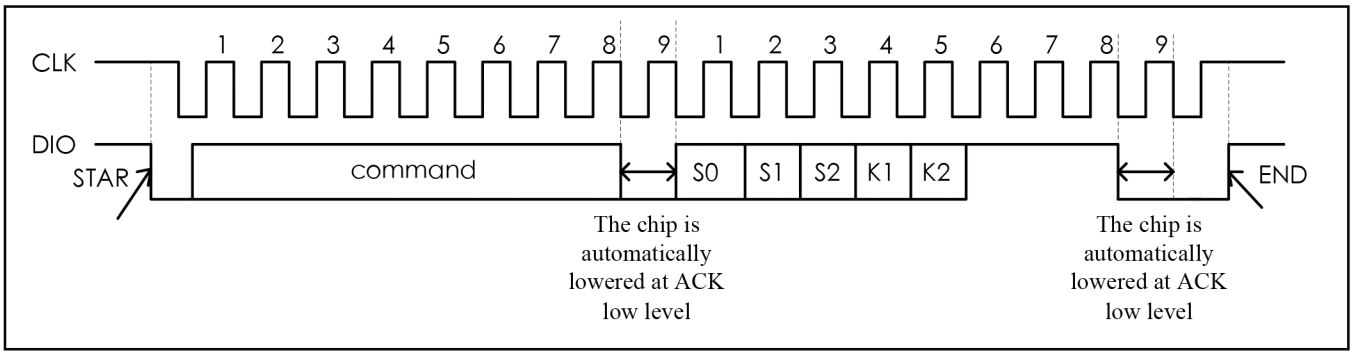
| SEG1 | SEG2 | SEG3 | SEG4 | SEG5 | SEG6 | SEG7 | SEG8 | |
|---|---|---|---|---|---|---|---|---|
| xxHL (low four bits) | | | | xxHU(high four bits) | | | | |
| B0 | B1 | B2 | B3 | B4 | B5 | B6 | B7 | |
| C0HL | | | | C0HU | | | | **GRID1** |
| C1HL | | | | C1HU | | | | **GRID2** |
| C2HL | | | | C2HU | | | | **GRID3** |
| C3HL | | | | C3HU | | | | **GRID4** |
| C4HL | | | | C4HU | | | | **GRID5** |
| C5HL | | | | C5HU | | | | **GRID6** |

## 6. Interface interpretation

Microprocessor data realize the communication with TM1637 by means of two-wire bus interface (Note: The communication method is not equal to 12C bus protocol totally because there is no slave address). When data is input, DIO signal should not change for high level CLK and DIO signal should change for low level CLK signal. When CLK is a high level and DIO changes from high to low level, data input starts. When CLK is a high level and DIO changes from low level to high level, data input ends.

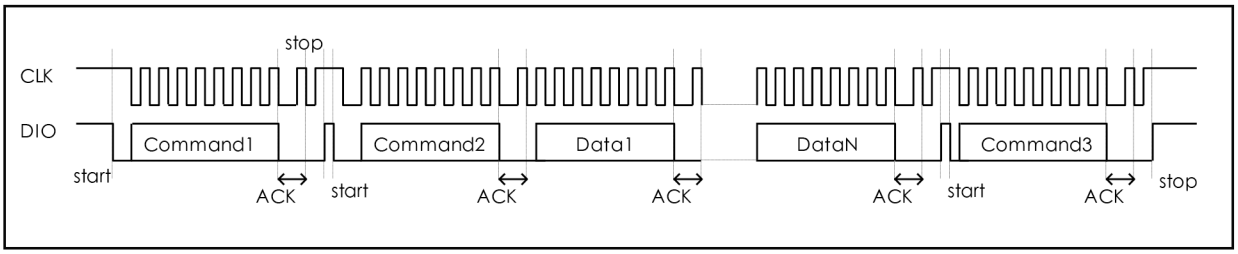
TM1637 data transfer carries with answering signal ACK. For a right data transfer, an answering signal ACK is generated inside the chip to lower the DIO pin at the failing edge of the 8th clock. DIO interface wire is released at the end of the 9th clock.

1. Command data transfer is as follows (Reading Key Data Timing)



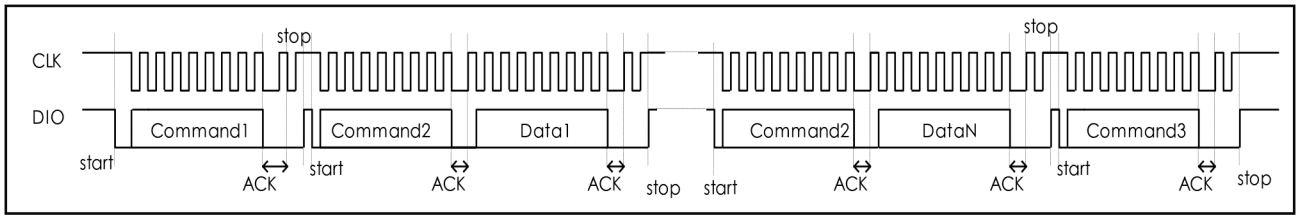

Command: command to read the keys; Key information coding consists of S0, S1, S2, K1 and K2. SGn coding consists of S0, S1, and S2. K1 and K2 are coding for K1 key and K2 key. The key should be read from low level to high level and the clock frequency should be less than 250K.

2. Write SRAM data in address auto increment 1 mode.




Command1: Set data
Command2: Set address
Data1~N: Transfer display data
Command3: Control display

### 3. Write SRAM data in a fixed address mode




Command1：Set data
Command2：Set data
Data1~N: Transfer display data
Command3: Control display

## 7. Data command

Command is used to set the display mode and the LED driver status.
The first byte input from DIO at CLK failing edge acts as a command. The highest B7 and B6 bytes after decoding are used to distinguish different commands.

| B7 | B6 | Command |
|---|---|---|
| 0 | 1 | Data command setting |
| 1 | 0 | Display and control command setting |
| 1 | 1 | Address command setting |

When STOP command is sent during command or data transfer, serial communication is initialized and command or data transferring becomes invalid (Command or data transferred before remain effective.).

#### 1. Data command setting

This command is to set data write and data read. 01 and 11 are not permitted to set for B1 and B0 bits.

| B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 | Function | Description |
|---|---|---|---|---|---|---|---|---|---|
| 0 | 1 | Zero should be inserted for irrelevant items. | | | | 0 | 0 | Data write and read mode setting | Write data to display register |
| 0 | 1 | | | | | 1 | 0 | | Read key scan data |
| 0 | 1 | | | | 0 | | | Address adding mode setting | Automatic address adding |
| 0 | 1 | | | | 1 | | | | Fix address |
| 0 | 1 | | | 0 | | | | Test mode setting (for internal) | Normal mode |
| 0 | 1 | | | 1 | | | | | Test mode |

## 2. Address command setting

| MSB | | | | | | | LSB | |
|---|---|---|---|---|---|---|---|---|
| **B7** | **B6** | **B5** | **B4** | **B3** | **B2** | **B1** | **B0** | **Display address** |
| 1 | 1 | Zero should be inserted for irrelevant items. | | 0 | 0 | 0 | 0 | C0H |
| 1 | 1 | | | 0 | 0 | 0 | 1 | C1H |
| 1 | 1 | | | 0 | 0 | 1 | 0 | C2H |
| 1 | 1 | | | 0 | 0 | 1 | 1 | C3H |
| 1 | 1 | | | 0 | 1 | 0 | 0 | C4H |
| 1 | 1 | | | 0 | 1 | 0 | 1 | C5H |

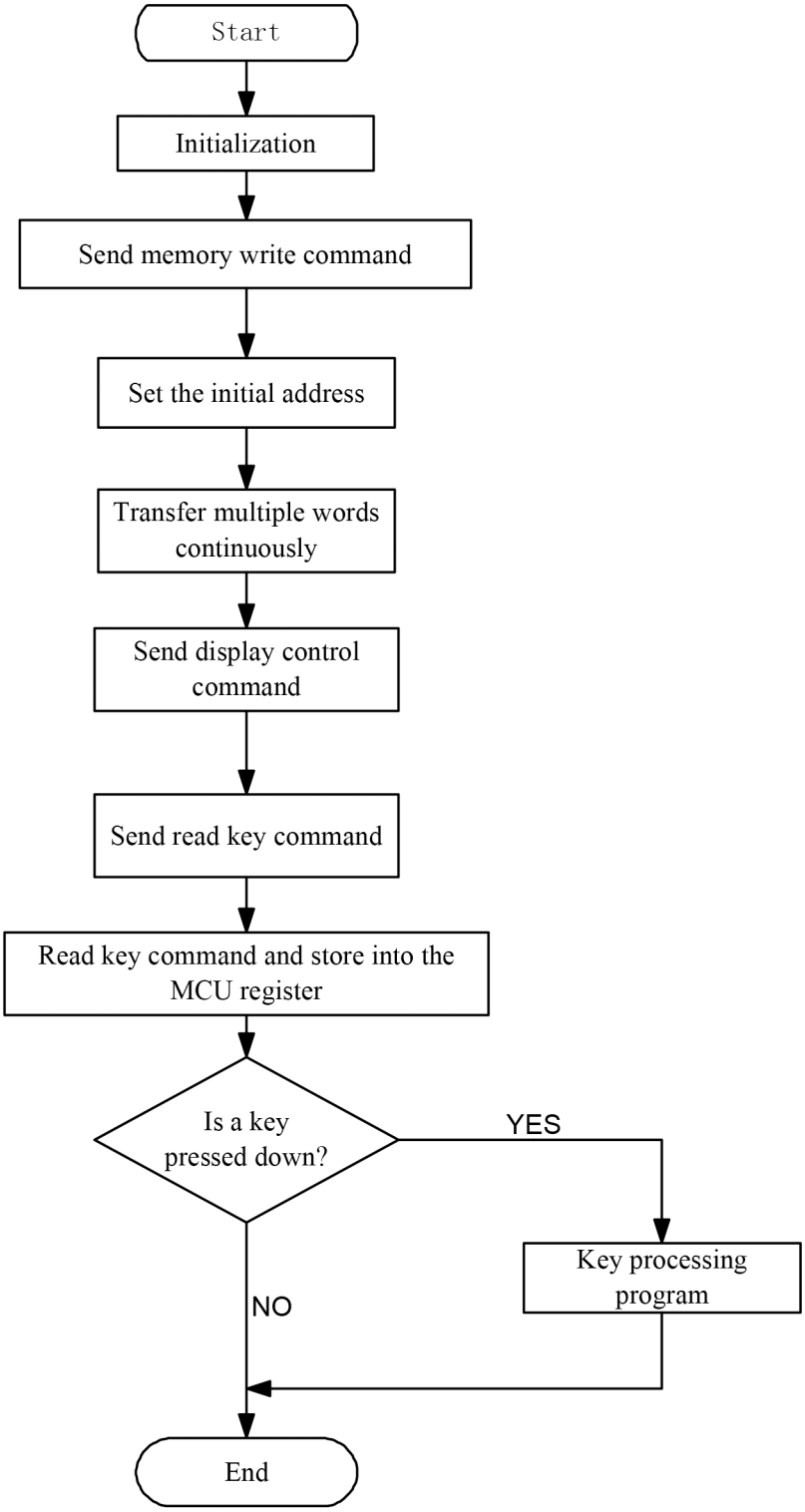
The command is used to set the display register address. If the address is set as C6H or a higher one, the data will be ignored until effective address is set. Once electrified, the default address is C0H.

## 3. Display control

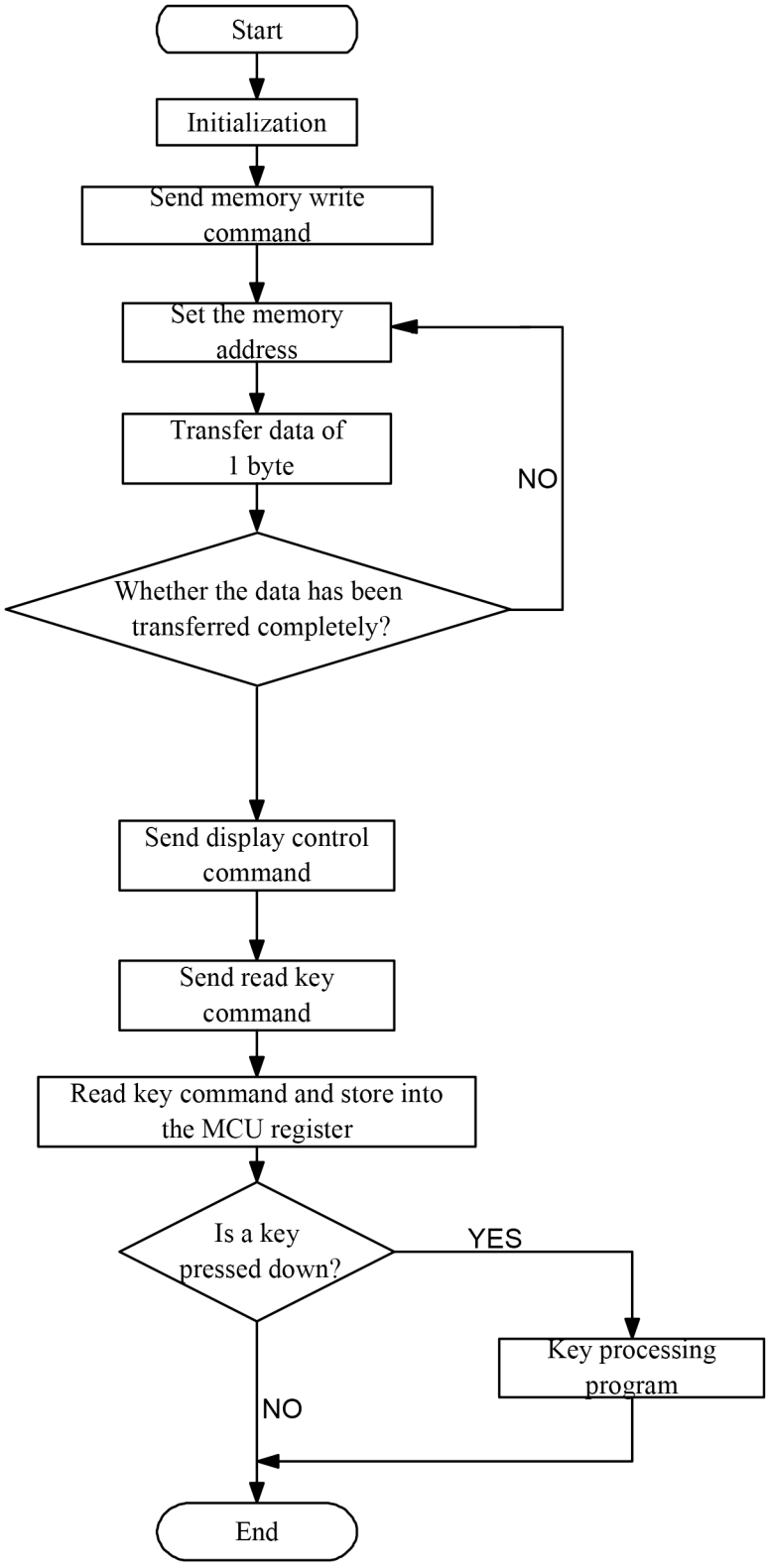
| MSB | | | | | | | LSB | | |
|---|---|---|---|---|---|---|---|---|---|
| **B7** | **B6** | **B5** | **B4** | **B3** | **B2** | **B1** | **B0** | **Function** | **Description** |
| 1 | 0 | Zero should be inserted for irrelevant items. | | | 0 | 0 | 0 | Setting of extinction number | 1/16<br>Pulse width is set as 1/16. |
| 1 | 0 | | | | 0 | 0 | 1 | | 2/16<br>Pulse width is set as 2/16 |
| 1 | 0 | | | | 0 | 1 | 0 | | 4/16<br>Pulse width is set as 4/16 |
| 1 | 0 | | | | 0 | 1 | 1 | | 10/16<br>Pulse width is set as 10/16 |
| 1 | 0 | | | | 1 | 0 | 0 | | 11/16<br>Pulse width is set as 11/16 |
| 1 | 0 | | | | 1 | 0 | 1 | | 12/16<br>Pulse width is set as 12/16 |
| 1 | 0 | | | | 1 | 1 | 0 | | 13/16<br>Pulse width is set as 13/16 |
| 1 | 0 | | | | 1 | 1 | 1 | | 14/16<br>Pulse width is set as 14/16 |
| 1 | 0 | | | 0 | | | | Display switch setting | Display OFF |
| 1 | 0 | | | 1 | | | | | Display ON |

## 8. Program flow chart

### 1. Flow chart of program using address auto increment 1 mode

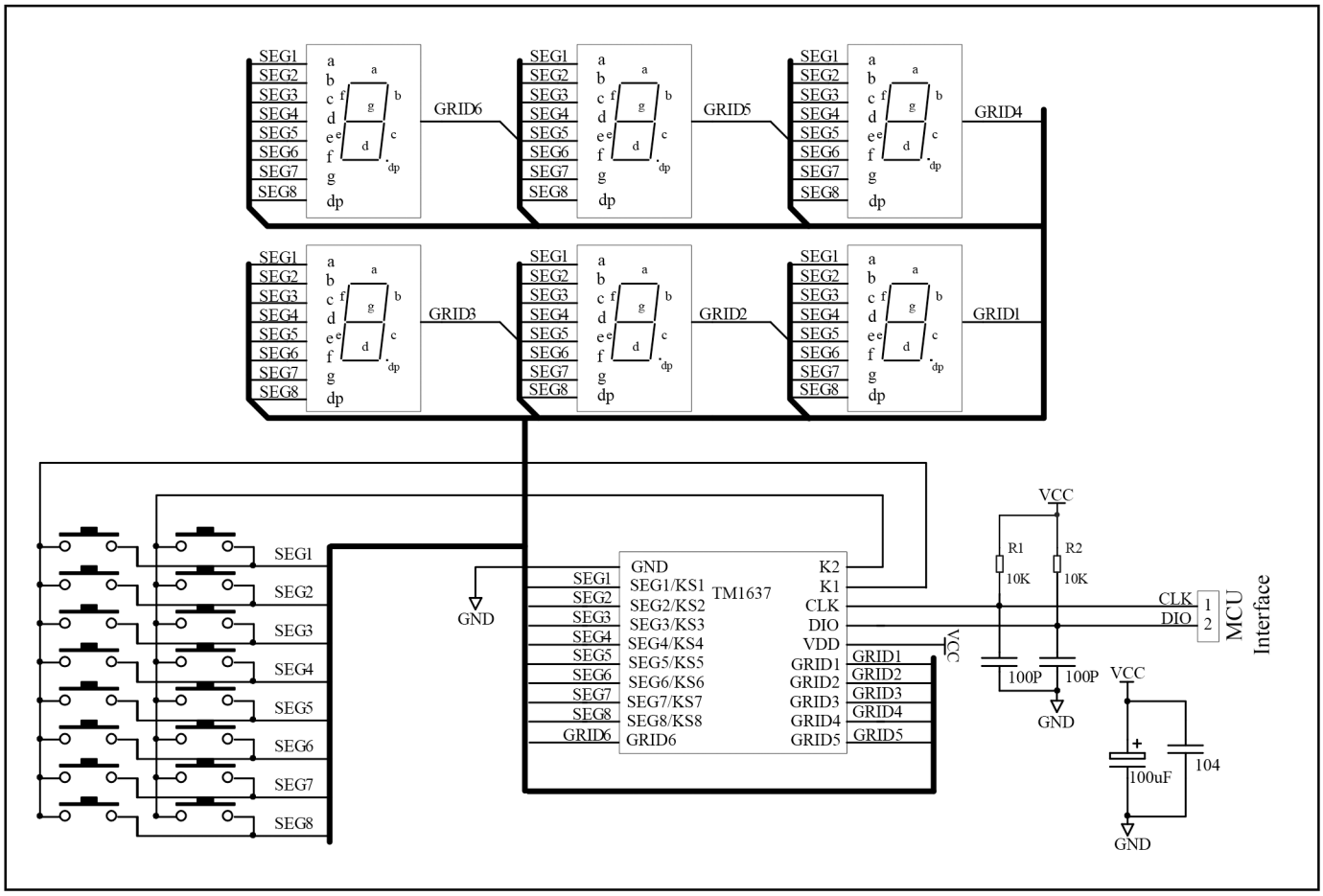


## 2. Flow chart of program design using fixed address



## 9. Hardware connection drawing

Nixie tube in circuit diagram is common anode one.




Note:

1. filtering capacitor between VDD and GND should be arranged on PCB plate as close to TM1637 chip as possible to strengthen filtering effect.
2. 100pF capacitor connected to the DIO, CLK communication port pull-up and pull-down can reduce interference to radio communications port.
3. Since blue-ray nixie tube break over step-down voltage is 3V, TM1637 power supply should be 5V.

# 10. Electrical parameter

## 1. Limit parameter (Ta = 25℃, Vss = 0 V)

| Parameters | Symbol | Range | Unit |
|---|---|---|---|
| Logic power supply voltage | VDD | -0.5 ～+7.0 | V |
| Logic input voltage | VI1 | -0.5 ～ VDD + 0.5 | V |
| LED and SEG drive sink current | IO1 | 50 | mA |
| LED and GRID drive source current | IO2 | 200 | mA |
| Power loss | PD | 400 | mW |
| Work temperature | Topt | -40 ～ +85 | ℃ |
| Storage temperature | Tstg | -65 ～+150 | ℃ |

## 2. Normal working range (Ta = -40～+85℃, Vss = 0 V)

| Parameters | Symbol | Minimum | Typical | Maximum | Unit | Test condition |
|---|---|---|---|---|---|---|
| Logic power supply voltage | VDD | | 5 | | V | - |
| High-level input voltage | VIH | 0.7 VDD | - | VDD | V | - |
| Low-level input voltage | VIL | 0 | - | 0.3 VDD | V | - |

## 3. Electrical character (Ta = -40 - +85 , VDD = 4.5 - 5.5 V, Vss = 0 V)

| Parameters | Symbol | Minimum | Typical | Maximum | Unit | Test condition |
|---|---|---|---|---|---|---|
| GRID drive source current | Ioh1 | 80 | 120 | 180 | mA | GRID1~GRID6, Vo = vdd-2V |
| | Ioh2 | 80 | 140 | 200 | mA | GRID1~GRID6, Vo = vdd-3V |
| SEG drive sink current | IOL1 | 20 | 30 | 50 | mA | SEG1~SEG8 Vo=0.3V |
| DOUT pin output low current | Idout | 4 | - | - | mA | Vo = 0.4V, dout |
| High-level output current tolerance | Itolsg | - | - | 5 | % | Vo = VDD – 3V, GRID1～GRID6 |
| Output pull down resistor | RL | | 10 | | KΩ | K1~K2 |

| | | | | | | |
|---|---|---|---|---|---|---|
| Input current | II | - | - | ±1 | μA | VI = VDD / VSS |
| High-level input voltage | VIH | 0.7 VDD | - | | V | CLK，DIN |
| Low-level input voltage | VIL | - | - | 0.3 VDD | V | CLK，DIN |
| Lagging voltage | VH | - | 0.35 | - | V | CLK，DIN |
| dynamic current loss | IDDdyn | - | - | 5 | mA | Non-loaded, display OFF |

## 4. Switching character (Ta = -40 - +85℃, VDD = 4.5 - 5.5 V, Vss = 0 V)

| Parameters | Symbol | Mini mum | Typical | Maxi mum | Unit | Test condition | |
|---|---|---|---|---|---|---|---|
| oscillation frequency | fosc | - | 450 | - | KHz | | |
| Transmission delay time | tPLZ | - | - | 300 | ns | CLK → DIO | |
| | tPZL | - | - | 100 | ns | CL = 15pF, RL = 10K Ω | |
| Rise time | TTZH 1 | - | - | 2 | μs | CL = 300p F | GRID1～GRID6 |
| | TTZH 2 | - | - | 0.5 | μs | | SEG1～SEG8 |
| Fall time | TTHZ | - | - | 120 | μs | CL = 300pF，Segn，Gridn | |
| Maximum clock frequency | Fmax | - | - | 500 | KHz | 占空比50% 50% duty ratio | |
| Input capacitance | CI | - | - | 15 | pF | - | |

## 5. Timing character (Ta = -40 - +85℃, VDD = 4.5 - 5.5 V, Vss = 0 V)

| Parameters | Symbol | Minimu m | Typical | Maximu m | Unit | Test condition |
|---|---|---|---|---|---|---|
| Clock pulse width | PWCLK | 400 | - | - | ns | - |
| Data setup time | tSETUP | 100 | - | - | ns | - |
| Data hold time | tHOLD | 100 | - | - | ns | - |
| Waiting time | tWAIT | 1 | - | - | μs | CLK↑→CLK↓ |