What limits the application of TEM in the semiconductor industry?

Hong Zhang *

PVD Technology, Applied Materials, 4250 Burton Drive, Santa Clara, CA 95054, USA

Abstract

Transmission electron microscopy (TEM) is expected to play an important role in the future development of the semiconductor industry because of its high resolution and analytical ability. However, long turnaround time and difficulties in making TEM specimens really affect the application of TEM for routine support of semiconductor manufacture. In this paper, the author presents some recent TEM results on submicron semiconductor devices with multilayer interconnection to show how to effectively use TEM to support process development and failure analysis. An advanced technique to prepare TEM specimen is also discussed. © 1998 Elsevier Science S.A. All rights reserved.

Keywords: Transmission electron microscopy (TEM); Semiconductor devices; Film

1. Introduction

Transmission electron microscopy (TEM) has experienced dramatic development in the last 30 years. The new generation field emission analytical TEM provides atomic scale resolution combined with nano-scale crystal structure (CBED), chemical (EDS) and electronic structure (EELS) information [1] and, thus, is ideal for the study of submicron semiconductor devices. Two types of techniques [2] are usually applied for examining semiconductor devices, namely, plan view TEM and cross-section TEM. Planar-oriented samples provide a relatively large view area of a thin film normal to its surface, which gives information about grain size, distribution of defect or precipitates. Cross-section TEM is an extremely useful technique, which has been applied to study film thickness, step coverage, implant damage, etch profile, via or contact filing, interface contamination, particle identification and failure analysis.

As the scale of semiconductor devices shrink to sub-half micron regime, it becomes more and more difficult to make the interconnection. Typically, multiple-layer metalization is required to improve contact resistance, adhesion and wetting property, and the performance of the devices is extremely sensitive to the quality of those layers. However, to characterize those materials at the bottom of a 0.25 μm contact or via structure to a few nanometers thick is beyond the ability of any other instrument. TEM could become a major failure analysis and process control tool for semiconductor industry in the future.

Although TEM has significant advantages, there are still some concerns about applying TEM for routine support of manufacturing and process development. These concerns are the following.

1.1. Small examining area

Traditionally, TEM was used to achieve high resolution at high magnification. The TEM specimen with a few micron electron transparent area is good enough for most purposes. Semiconductor devices may contain a few million transistors in a centimeter square area. It is not convincing and sometimes may be misleading to examine only a few features and claim that it represents the process condition of the entire device.

1.2. Very difficult to prepare TEM specimen

First of all, for most devices, various materials, such as Si, SiO₂, Al, Ti, TiN, TiSi₂, W, WSiₓ, TiW, etc., are deposited and patterned to form functional devices and interconnections. The thickness of the entire device may be over 10 μm. To make all of the 10-μm materials to be electron transparent is a great challenge; secondly, failure analysis often requires cross-section TEM to be performed precisely on a single small feature (usually less than 0.5 μm), which is extremely difficult.
1.3. Long turnaround time

TEM analysis consists of many procedures, from sample preparation, image taking to final analyzing, they all require special skills and are usually very time consuming. Long turnaround time is one of the major complaints about TEM service.

1.4. High cost to set up a TEM lab

A well-established TEM lab may easily cost US$2 million. It is difficult to justify this amount of money unless we can address all the difficulties and complaints mentioned before.

As one may realize, most of the problems with TEM application are related to sample preparation, which is often the most difficult part of TEM analysis. In general, we classify the usage of TEM for semiconductor device as process evaluation and failure analysis, each of which requires different sample preparation techniques. For process evaluation, a large number of features such as contacts and vias need to be surveyed to have a statistical conclusion about current processes. While for failure analysis, precision TEM technique is applied to reach a specific area, such as a single poly gate, contact or via, and find out the root cause of the failure. In this paper, I will discuss recent developments in TEM sample preparation and present some TEM results on advanced semiconductor devices.

2. TEM sample preparation

The objective of TEM sample preparation is to create an electron transparent region containing the feature interested without contamination and artifacts. There are many different methods to make TEM specimens [3], but only three types of techniques are most commonly used for preparing TEM specimen from semiconductor devices.

2.1. Dimpling and ion milling technique

Dimpling and ion milling [4] is a well-known technique and most people use it. The sample is glued together, mechanical thinning, disc cutting to 3 mm disc, and then dimpling to a few microns thick. Finally, ion milling is applied. This technique is easy to use and works well for blanket films, large feature and repeat patterns. However, it provides smaller thin area and is difficult to target special feature.

2.2. Focused ion beam technique

Focused ion beam technique [5] was designed to make TEM sample from a specific area. Focused high energy gallium ions are used to remove materials from both sides of the feature interested. This technique offers a reliable method to make high precision cross sections of specific areas. However, this method provides very limited view area and introduces some artifacts. It also requires very expensive equipment, which further limits the usage of this method.

2.3. Wedge technique

Originally developed at IBM [6], this technique provides the highest flexibility over the other techniques. It can be used to make plan view, regular cross section and precision cross section specimens. Using a fixture called tripod polisher, one can thin the sample down to less than 1 μm by pure mechanical polish. Since all TEM specimen used for this paper are made by the wedge technique, I will explain more details about this technique as follows.

A new fixture called T-tool (T-tool is available from T & T group at 1500 Wyatt Dr., Suite 12, Santa Clara, CA, 95054, USA, referring to the shape of the tool, is used for sample preparation. First of all, a piece of thin cover glass is glued on the surface to protect the feature interested. The sample is then mounted on the T-tool model A for first side polish, as shown in Fig. 1a. The T-tool can be placed on the stage of the optical microscope as shown in

Fig. 1. (a) A schematic drawing of using T-tool for first side polish of TEM specimen. (b) A schematic drawing of using an optical microscope to monitor the advancing cross-section line.
Fig. 1b, and thus the advancing cross-section line can be monitored closely. The cross-section line can be adjusted by turning the two adjusting screws until the cross-section line parallel to the desired final finish line. As the advancing cross-section line approaches the target, finer grits of diamond lapping films are applied. The sequence can be 15, 6, 3, 1, 0.5, 0.1 μm and final syton (0.05 mm silica suspension) on polish cloth. First side polish stops, when cross-section line reaches the target.

For second side polish, T-tool model B is applied. After flattening the tool, the polish specimen is mounted on the glass surface by super glue or crystal bond with the polish surface attached to the glass. The T-tool is then placed on the grinding wheel for the second side polish as shown in Fig. 2a. A wedge angle can be introduced by turning the two adjusting screws. As the thickness of the specimen is down to 10–20 μm, it becomes light transparent. The T-tool can then be placed on the stage of an optical microscope for examination, as shown in Fig. 2b. According to the color difference of the specimen under transmitted light, the user may make the final adjustment to the wedge angle. Since the T-tool is very light and handy, it makes the sample preparation relatively easy. The finished specimen is then removed in acetone and mounted on a Cu grid. Fig. 3 is an optical microscopic image showing a finished cross-section TEM specimen with five-layer interconnection. The specimen is very thin and fringes in the silicon can be seen clearly. Usually a few seconds to a few minutes of ion milling is necessary for further thinning or cleaning.

3. TEM for process evaluation

One of the main purposes of using TEM to evaluate semiconductor manufacture on process is to utilize the high image and spatial resolution of TEM to investigate detailed structures produced by each process step, espe-
Fig. 5. TEM image of five-layer metallization. A total of 35 W contacts and vias are examined on this single image.

Fig. 6. TEM image of a six-layer interconnected structures with W plugs.
cially the interface area. In order to perform various analyses, the specimen has to be uniformly thin without contamination and artifact. As an example, Fig. 4 gives a TEM image of tungsten via structure. The sample contains Al, SiO$_2$, Ti, TiN, W. The thickness and grain structures of each metal layer can be easily distinguished.

As mentioned before, very limited view area is one of the major concerns with using TEM. In order to make a reliable evaluation, it is necessary to examine a large number of features such as poly gates, contacts and vias, to have a statistical conclusion about the process. Usually, contact or via chains are chosen for this purpose. Fig. 5 is a TEM image of a five-layer metal structure. A total of 35 W contacts and vias are shown on this single image. The thin area measures 2 mm long (limited by the size of Cu grid) along the front edge of the specimen. Therefore, examining hundreds even thousands of features in TEM on one cross section becomes possible. We can zoom in and look closely at any one contact or vias which may have a problem. Clearly, improvement of TEM sample preparation technique has come to the point that the TEM should not be treated as a tool that can only focus on very small area.

The high quality of specimen also enables us to fully take advantage of the capacity of TEM. Electron energy loss spectrometry (EELS) is a very powerful technique.

Fig. 7. Element maps of the six-layer interconnected structure by using Gatan image filter.
used to obtain chemical and even electronic structure information from materials. Its high sensitivity to light elements makes it more desirable for semiconductor usage. However, EELS analysis is very sensitive to specimen thickness, and in fact, EELS can only perform on very thin area (usually < 500 Å). Using the wedge technique, we are able to prepare a multilayer metal structure for EELS analysis. Fig. 6 is an example showing a six-layer inter-
Fig. 10. (a) TEM image of a failed Kelvin contact, showing under etch is the cause of failure. (b) TEM image of a failed Kelvin contact, showing wet clean causing silicide loss is the reason of the failure.

The connected structure, while Fig. 7a–f gives element maps of the six-layer structure by using Gatan image filter.

Combined with carefully designed experiments, TEM can also play an important role in process development. Fig. 8a and b gives a series of snapshots of CVD Al process to show the formation mechanism of voids. As shown in Fig. 8a, after 10-s deposition CVD Al film conformally covers the contact hole, while after 20-s deposition big voids are found in the middle of the contacts, as seen in Fig. 8b. The results indicate that CVD Al follows the rule for most CVD processes. It forms conform film initially and, at certain point, it begins to bridge over the top of the contact forming long key hole. Since Al is a soft metal with lower melting point, the long key holes in contacts will start rounding to lower surface energy by reducing the total surface area, and thus create big voids in contacts.

No matter how great the TEM image looks, TEM work cannot be fully appreciated until it can match the speed of the semiconductor industry. Quick turnaround is an essential requirement for the application of TEM in this industry. As mentioned earlier, sample preparation is often the major part of TEM analysis process. By using our newest T-tool, a well-trained technician can make a high quality TEM specimen within 2 h, which is close to the turnaround time of a polished cross-section SEM.

4. Precision TEM for failure analysis

Precision TEM is one of the most challenging works in any TEM lab. Usually, the devices fail during e-test and failed locations can be identified by different techniques, such as liquid crystal, emission microscopy, and voltage contrast. Precision TEM is then applied to identify the root cause of the failure. To a well-trained electron microscopist, the ‘precision TEM’ has two meanings: to precisely catch the smallest feature on devices, which requires a great deal of skill, patience and dedication, and to precisely point out a single process step causing failure, which requires knowledge of both electron microscopy and manufacture processes.

One of the most common problems related to device manufacture is the variation of contact or via resistance. A chain structure is usually used to evaluate the resistance. Random cross-section TEM works well if the problem is globe. However, if the problem is caused by a few bad contacts or vias, the chance for a random cross section to catch the failed contact or via from hundreds even thousands of them is very small. Precision TEM can then be applied if the failed location can be identified. Another common method to test the resistance of contact or via is to use a specially-designed structure, a so-called Kelvin structure which allows a single contact or via to be tested. Precision TEM can be used to cut a single Kelvin structure with known resistivity. The real challenge of doing precision TEM by wedge technique is the first side polish. Fig. 9 shows an optical microscopic image showing the ending.

Fig. 11. SEM image of a defective W via, showing enormous growth of W. However, no conclusive answer about the root cause.
Fig. 12. Precision cross-section TEM image of defective W via, showing a thin columnar Al whisker at center of the W plug. The Al is squeezed out from metal line at the bottom of the via.

Obviously, for the contact in Fig. 10a under etch is the problem and for the contact in Fig. 10b silicide loss is the reason. As pointed by arrows in Fig. 10b, there are undercuts at the lower corners of the contact indicating that wet clean before contact fill is the root cause of silicide loss.

Particles are another important issue for semiconductor manufacture. The most common techniques used to identify particles are focused ion beam and cross-section SEM. Combined with EDS, these techniques can verify the location and average composition of most particles. However, it is usually difficult to find the root cause of the particle because of lack of detailed information. Fig. 11 is a cross-section SEM image of an abnormal growth W on top of a via. Although we know the extrusion is W, it is hard to understand what happens and why it happens. Fig. 12 gives a TEM image of the same kind of defect. The sample was made by wedge technique and the cross section cuts through the center of the defect. A thin columnar Al whisker was found at the center of the W plug. The Al whisker connects to the Al metal line through an opening of Ti/TiN layer at the bottom of the via, indicating that the Al whisker was squeezed out from the metal line at bottom. A close look at the interface between Al whisker and W shows there is no Ti/TiN layer in the interface, indicating that the Al whisker must be formed after Ti/TiN deposition. The key hole between the side wall of via and Al whisker suggests that the nucleation of W occurred simultaneously on both sides, indicating that the Al whisker must be there before W deposition is started. Therefore, the particle, which appears to be W, is actually caused by the Al whisker. The Al whisker was formed after Ti/TiN deposition and before W deposition, the process step most likely is preheating.

As the dimension of devices scale down to submicron regime, electromigration has shown to be one of the...
primary causes of chip-level failure on conducting lines. While a great deal of study has been done on the fundamental mechanism of atomic motion induced by electric current and on failure statistics, there has been relatively less amount of work linking those fundamental study to the actual device failure, in other words, lack of experimental evidence to show the development of microstructure during failure process. Precision cross-section TEM technique offers the possibility to characterize the real electromigration test structure of submicron devices. In many cases, a chain structure, usually 1 mm long with 10 to 20 vias along the chain, is applied to test electromigration property. The current passes through the via chain under certain condition until it fails. Since the failure could be anywhere along the chain, it is desirable to look at the entire chain structure to have a complete information about the failure process, which means that the cross-section TEM sample has to be made to cover the entire test structure and catch every segment of the 0.5 μm wide and 1 mm long via chain. Again using the wedge technique, this is achievable. Fig. 13a is a TEM image of five vias in an electromigration test structure before being stressed, while Fig. 13b is the same kind of structure after being stressed. Clearly, voids can be seen near via no. 1, 3 and 5 and at via no. 2, 4, Cu accumulation occurs. The results reveal not only vacancies but also Cu migration during electromigration test.

5. Summary

The application of TEM on semiconductor devices has not been and may never be as easy as that of SEM, but it is also not as difficult or unreachable as many people thought. Although very intensive training is necessary, it is achievable to everyone. In this paper, I present various examples, some of them belong to the most difficult samples, showing that there is no limit on the application of TEM in the semiconductor industry. In our practice, it is the people’s presumption about TEM that keeps them from using it or in many cases that people do not realize this is something today’s TEM can do. Therefore, if anything still limits the application of TEM in the semiconductor industry, it is our own imagination.

References