Patterned Channels for Organic Field Effect Transistors

Code: S181-S184

Substrate: SiO_2

Architecture device: Bottom Gate, Bottom Contact.

Transistor Channel Type: Linear, Constant Length (30 µm, 10um or 5um) or variable length (30, 40, 50, 60, 80 µm, 10, 15, 20, 25, 30 µm or 5, 7.5, 10, 15, 20 µm)

Materials: Cr and Au (Contacts pads), Cr and Au (Active area)

Silicon Oxide OFET Substrate - Specification and Technical Data

Silicon oxide substrates (SiO_2) are cut from a highly P-doped (Boron) silicon wafer coated with 100-nm-thick layer of SiO_2 on both side. Specifically designed for OFET testing and material screening, the doped silicon and the oxide layer provide the gate and the dielectric respectively for a bottom-gate bottom-contact architecture.

Table 1: Substrate specification

Size	20 mm × 15 mm
Substrate Thickness	725 ± 25 µm
Growth	CZ
Orientation	<100>
Type/Dopant	P/Boron
Resistivity	5×10^{-4} to $10^{-2}\Omega$/cm
Front Surface	Polished
Back surface	Etched
Oxide Thickness (SiO_2)	300nm
Capacitance	≈ 1.09×10^{-8} F/ cm^2

Contacts and Device Channels - Design and Fabrication Specification

Design details

The structure and key features of the linear, low-density, constant-length channel, pre-patterned OFET substrate are detailed in the schematic in Fig. 1. The channel bar tolerance is ±8 µm.

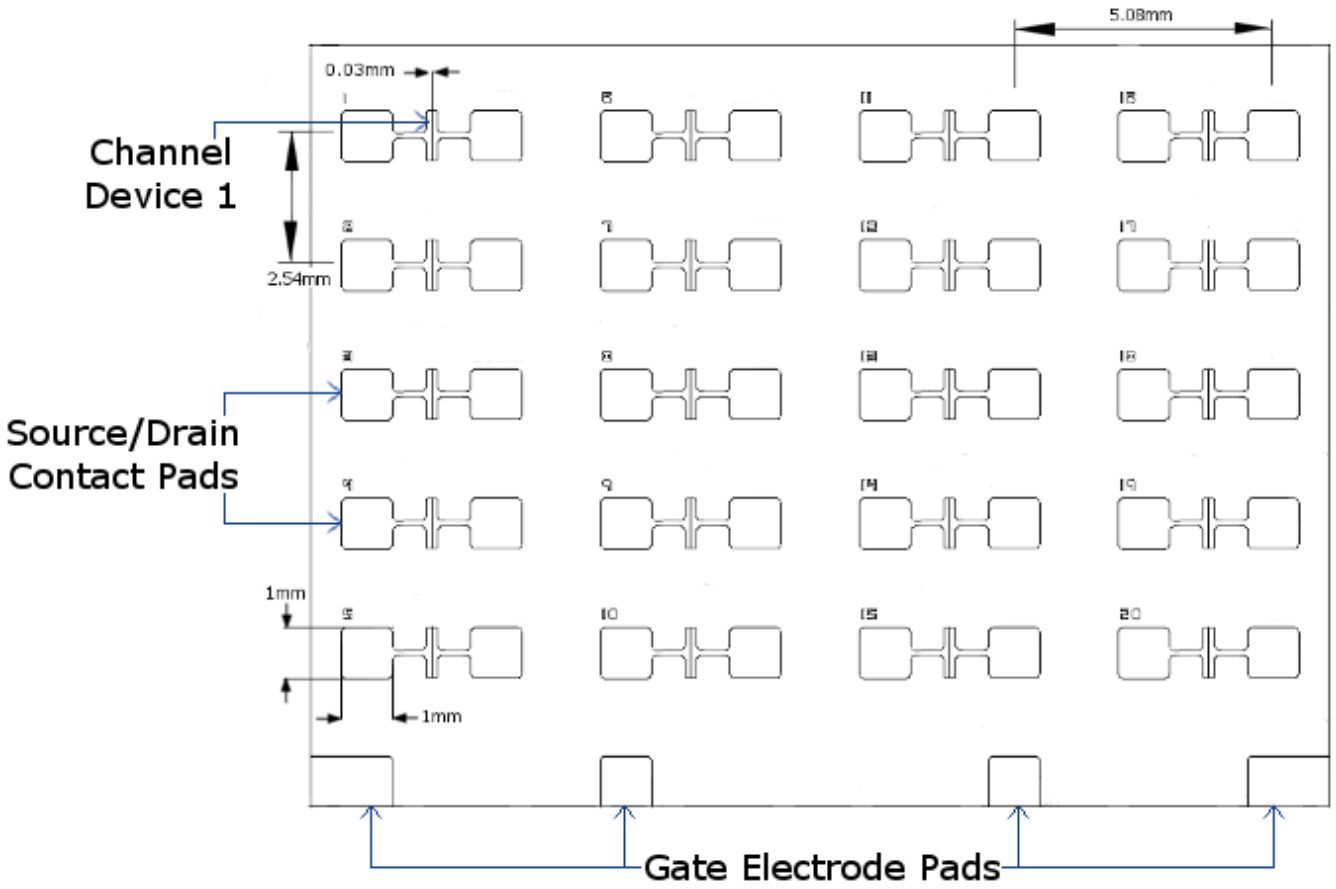

Figure 1. Schematic of linear, high-density, constant-channel-length, pre-patterned silicon substrate for OFET fabrication.

Handling

Refer to Fig. 2 for the location of the different *areas* on the pre-patterned substrate.

Substrate areas:

Gate(1); contact pad(2); central (3); active area/OFET channels (4), critical edge (5). The channels are numbered one to twenty starting from the top left corner and moving down each column.

The substrate must be handled with care on the gate, preferably using round end tweezers such as type 2A (C121). Use of pointed tip tweezers increases the risk of inadvertently damaging the patterned metallic features or cracking the silicon oxide dielectric.

Areas one and two are relatively robust and can be handled by tweezers and wiped clean with cotton buds. However, any mechanical contacts within the *active area* (area 3 to 5) may damage the channel and hence affect the device performance. Excessive tweezer pressure may also damage the drain/source pads and, especially the narrow “bridges” connecting the pads with the transistor channel.

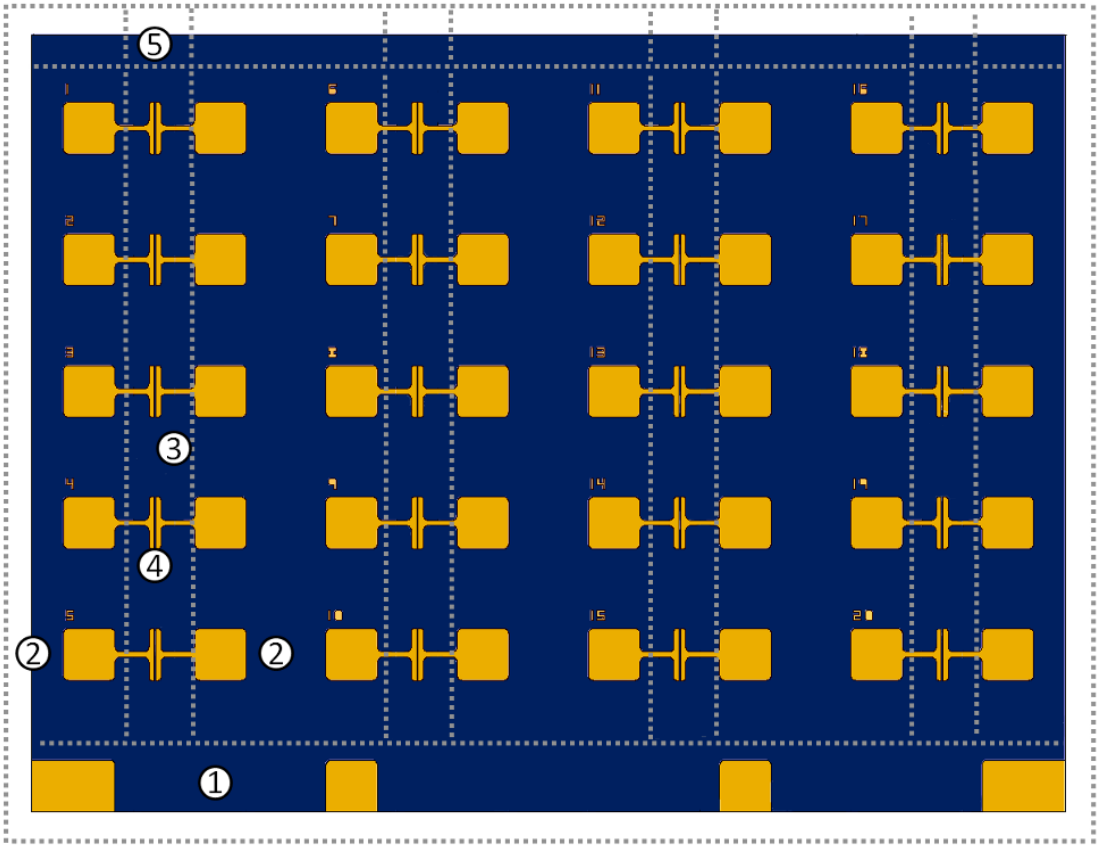

Figure 2. High-density, pre-patterned substrate: zone sub-division

OFET fabrication

The pre-patterned Ossila silicon oxide substrates are suitable for OFET fabrication by spin-coating, dip-coating or drop casting.

Before starting the fabrication routine, make sure that the surface is clean and free of dust. It is advisable to rinse the substrate in butanone (with optional five minutes sonication), and blow dry with a nitrogen gun.

Do not use a detergent, such as Hellmanex III, since this may etch the patterned features.

Removal of Excess Semiconductor

If the semiconductor is applied by spin or dip coating, the *gate* and *drain/source areas* must be wiped clean using a cotton swab wetted with the appropriated solvent (Chlorobenzene or Butanone, for example).

Make sure that the *central area* (*active area* and the gold electrical bridges, see Figure 2) is not wiped.

Note. The Chromium adhesion layer should guarantee sufficient adherence to allow for gentle cleaning of the gold bridge in the *central area*. However, we cannot guarantee against possible damage that may be caused by contact with the gold source-drain electrodes (area 3).

In order to limit gate leakage, it is advisable to clean the lateral edge of the substrate: keep the cotton bud in an upright position (perpendicular to the substrate) and slide it around the edge holding the substrate by the *gate area* using a pair of tweezers.

The *critical edge* must be carefully cleaned since it can be the source of non-negligible gate leakage. In order to clean this area effectively without damaging the devices, the following routine should be followed:

- Place the substrate on a surface and hold it firmly with tweezers,
- Position a cotton bud tip (wet with the appropriate solvent) on the surface, next to the *critical edge*.
- Incline the cotton bud at an angle of 80/85 degree toward the substrate surface and move it along the edge a few times.

Finally, in order to avoid cross-talk between devices, it is also advisable to wipe the areas between the channels using a high-precision cotton swab, see Fig 3.

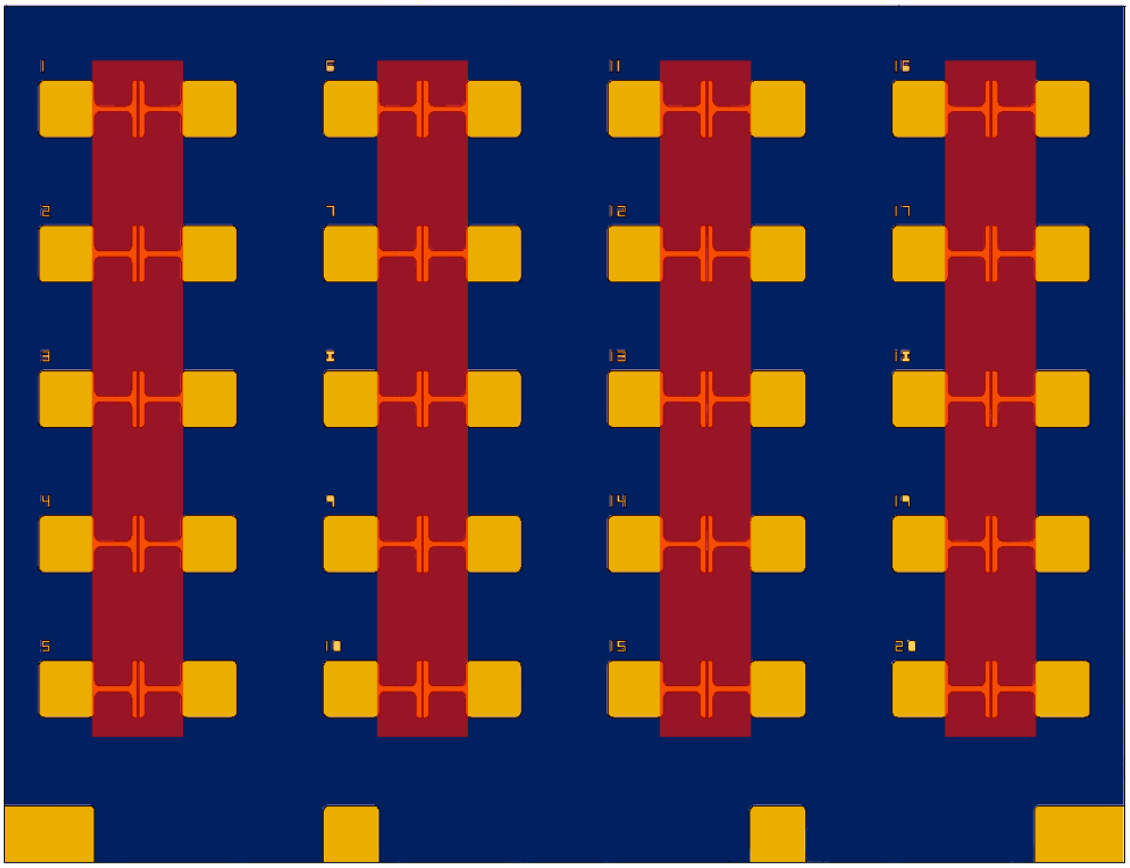

Figure 3. Standard Cleaning.

Fine cleaning

In order to achieve the best performance of the semiconductor materials, a thorough cleaning of the semiconductor between devices is recommended, see Fig 4. Cleaning between devices can be carried out through careful use of pointed (high-precision) cleanroom cotton swab.

Warning

Pointed cotton swabs can easily damage the active area. It is recommended to practise cleaning first.

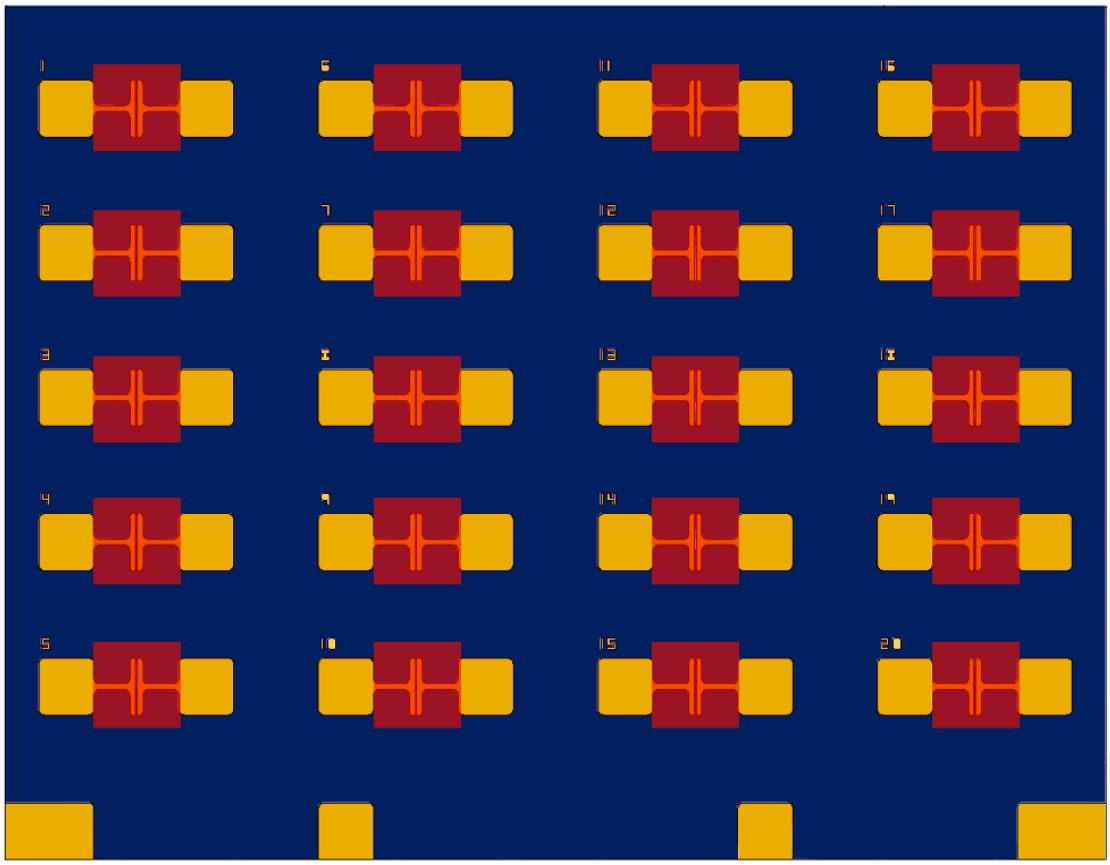

Figure 4. Substrate fine cleaning

Substrate Reusability

If carefully handled, and **depending on the fabrication/surface treatment**, the substrates are designed to be reused for (at least) three/four fabrication cycles.

In order to reuse the substrate, it is necessary to remove the previously administered semiconductor using an appropriate solvent.

The cleaning routine and the solvent used may depend on the specific fabrication protocols. For example, with P3HT in a chloroform/trichlorobenzene solution, the following cleaning routine may suffice to restore the substrate to its (almost) pristine condition:

- Rinse the substrate in chlorobenzene (if available, spin coat 1 ml or more of chlorobenzene on the substrate, dynamic delivery at 2000/3000 RPM).
- Use a solvent wetted cotton swab to wipe clean the edge and the back of the substrate
- Dip the substrate (face up) in chlorobenzene for 24 Hr (optional)
- Sonicate for five minutes with the substrate dipped in warm chlorobenzene
- Rinse copiously in clean chlorobenzene
- Rinse in Acetone (optional) and Iso-propyl alcohol followed by DI water (recommended)
- Blow dry with nitrogen

Surface treatment, such as OTS or dipolar SAM (PFBT, CBS etc), **are not removed** by this cleaning routine.

Do not use detergents as they can etch the aluminium from the surface.

Exposure of the substrate to pure chlorobenzene (or any chlorinate solvent) for more than 20/30 seconds may compromise the adhesion strength of the Cr/Au layer on the silicon surface. Do not subject the gold active area to any mechanical stress during the chlorinate-solvent cleaning routine, blow dry gently. Before spin coating, make sure that the chlorinated solvent is completely evaporated. Short exposure to pure chlorinated solvent (less than 20 seconds) should not affect the mechanical resilience of the Cr/Au layer. After a long exposure, see above, the Cr/Au layer regains its original adhesion property with the evaporation of the chlorinated solvent.

Example of OFET fabrication

Ossila PBTTT (M141), Poly(2,5-bis(3-hexadecylthiophen-2-yl)thieno[3,2-b]thiophene), is dissolved in dichlorobenzene (3 mg/ml) in an inert environment (glove box). The solution is placed on a hot plate at 80 ^{o}C with a magnetic stirrer bar for approximately three hours. After cooling down to 50 ^{o}C, the solution is filtered with a 0.45 µm PVDF filter.

The Ossila Pre-fabricated substrates are treated with PFBT to modify the gold work function and OTS to optimise the silicon surface property.

The semiconductor solution is delivered through spin coating at 2700 RPM for 180 second. The annealing (inside a glove box) is carried out by placing the substrate on a hot plate for one hour at 150 ^{0}C and then slowly cooling down at room temperature.

The characterisation of the 20 transistors is carried out using the Ossila High Density OFET Test Board; see Figs. 5, 6, 7 and 8 for a summary of the main results.

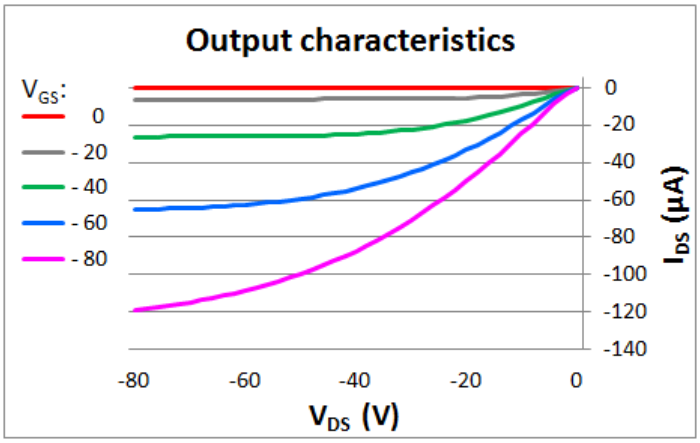

Figure 5: Typical output characteristic plot for the devices measured.

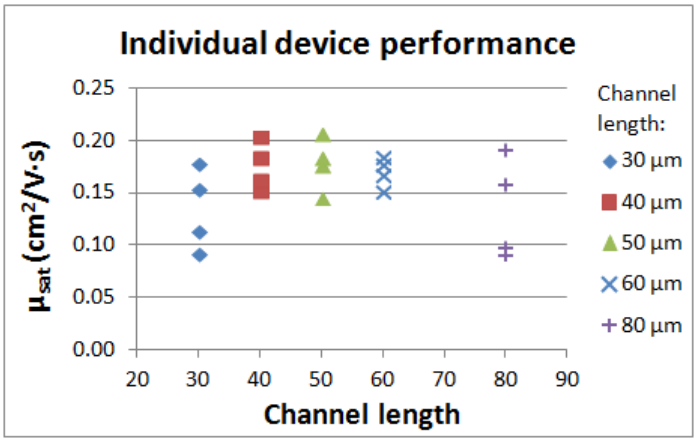

Figure 6: Saturation mobility of the 20 individual devices on the HD substrate.

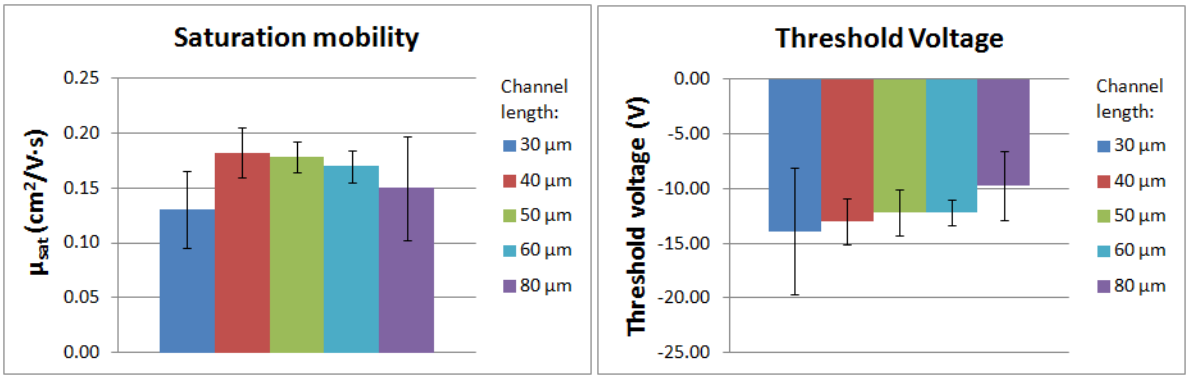

Figure 7: Data from all measured devices: the saturation mobility (left) and the threshold voltage (right). The error bars represent 2 × σ.

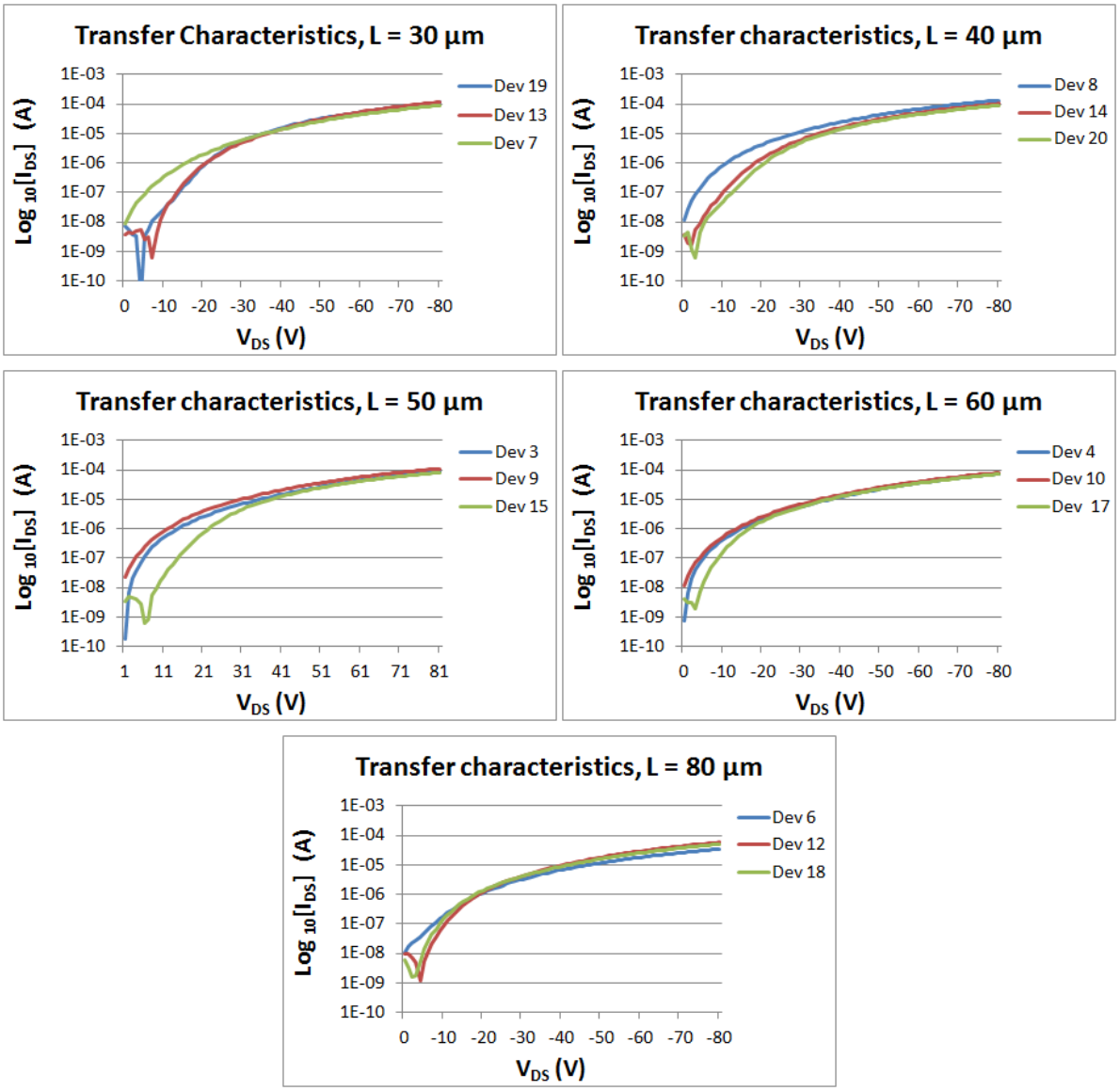

Figure 8: Transfer characteristics of the 75% highest performing devices for each channel length measured.