Mobility measurements for M104 (P3HT)

Contents

Overview

In this fabrication report, we detail an OFET measurement protocol on material M104 - a high regioregularity and molecular weight batch of poly(3-hexylthiophene-2,5-diyl), commonly known as P3HT.

Field effect mobilities in excess of **0.12 $cm^2/(V \cdot s)$** are recorded using M104 when the active layer is dispensed on OTS-treated silicon oxide dielectric by static spin coating from an optimized high/low boiling point solvent mix.

High hole mobility in conjunction with good solubility and partial air stability make regioregular P3HT a reference material of choice for both fundamental and applied research in organic electronic, physics and chemistry. As one of the most well-studied organic semiconductor, P3HT is often acknowledge to be one of the benchmark against which any new p-type or donor conjugate molecule should be compared and evaluated.

Mobility has previously been found to be positively correlated with increasing region-regularity, slow drying time (achieved using high boiling point solvent), lowering of the surface energy, and molecular weight in excess of 50kD. These conditions favour π-π stacking parallels to the OFET substrate, which in turn results in improved charge transport across the transistor channel [1-13].

Here, OFET substrate specifications were prepared using aluminium contact pads at the edge of the substrate and gold electrodes are selectively thermally evaporated on pre-diced silicon substrates to be used in bottom gate, bottom contact architecture, see Fig 1.

- Substrate size: 20 × 15 mm
- Gate conductivity: 1-30 Ω·cm (Boron doped)
- Silicon oxide thickness: 300 nm
- Device per substrates: five, common gate
- Channel length: 30 µm
- Channel width: 1000 µm

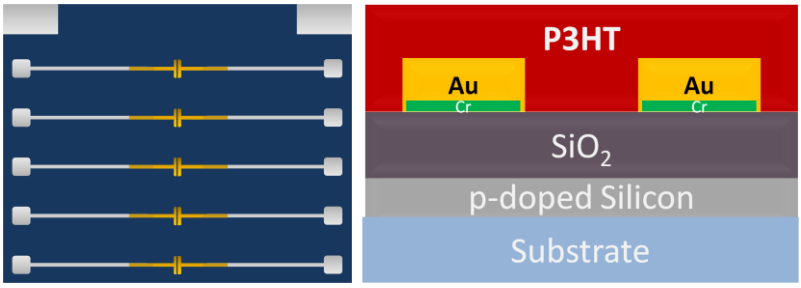

Figure 1. Left: constant-length, bottom contact, bottom gate OFET substrate. Here, the yellow features represent the Au electrodes, while the silver colour indicates the Al contact pads. Right: Schematic of the bottom gate/bottom contact OFET. Notice that the Au electrodes completely cover the Cr adhesion layer.

The substrates were also treated with Octadecyltrichlorosilane (OTS) and Pentafluorobenzene thiol (PFBT) prior to casting the organic semiconductor. The presence of OTS "neutralises" carrier traps (Si-OH groups), lowers the surface energy and makes the substrate hydrophobic. Meanwhile, under appropriate deposition conditions, PFBT forms a self-assembled monolayer covering the Au(111) surface. Due to its polar character, PFBT SAM is capable of decreasing the Au workfunction, and therefore favouring hole injection into the HOMO level.

Condensed Device Fabrication Routine

The active layer solution preparation, spin coating, substrate annealing and measurements are performed in a glove box under a nitrogen atmosphere (H_2O < 0.1 PPM; O_2 < 5/8 PPM).

Active Layer Preparation

High-Regioregular and high molecular weight RR-P3HT (M104) (RR = 96.3%, Mw =77,500, Mn = 38,700) is dissolved in a mix of high and low boiling point solvent in order to exploit the beneficial effect of long drying time and increase the wettability of low energy surface, respectively. In details,

1. 5 mg/ml of M104 dissolved in anhydrous Chloroform: Trichlorobenzene (99:1) mix;
2. Vial is placed on hot plate (70 ^{o}C) with a stirrer bar for 30 minutes;
3. Solution cooled down at room temperature and then filtered with a 0.45 µm PFTE filter;
4. Solution stored overnight on a hot plate at 30 ^{o}C to prevent excessive aggregation of the P3HT molecules.

Substrate Cleaning

1. Substrates loaded on to substrate rack (to keep them in upright position);
2. Sonicated in hot Hellmanex solution (1%) for five minutes;
3. Rinsed twice in hot water;
4. Sonicated in warm Isopropyl alcohol (70 ^{o}C) for five minutes;
5. Rinsed twice in cold DI water;
6. Substrates stored in DI water.

Thermal deposition of Electrodes and Contact Pads

1. Done on Edwards 306 Thermal coater in clean room condition;
2. Substrates are blown dry and loaded in a low density evaporation stack with a low density shadow mask to pattern the desired features;
3. Secondary mask is added to selectively evaporate the gate and drain/source pads;
4. Vacuum chamber pumped down to a vacuum pressure of 5×10^{-6} mBar;
5. Chromium adhesion layer: 5 nm, rate ~0.05 nm/s;
6. Aluminium: 80 nm, rate: ~0.4 nm/s;
7. Changed secondary mask to deposit electrodes (FET channels);
8. Vacuum: 2 to 3×10^{-6} mBar;
9. Chromium adhesion layer: 1 nm, rate ~0.05 nm/s;
10. Gold: 40 nm; rate ~0.05 nm/s.

PFBT treatment for Au electrodes (laminar flow)

1. Oxygen plasma treatment, 30 seconds at 100 W;
2. Substrates immerged in 2.5 mMol/l solution of PFBT in isopropyl alcohol at room temperature;
3. Substrates rinsed twice in pure isopropyl alcohol;
4. Substrates are blown with nitrogen gun.

OTS treatment for SiO_2 dielectric (lamina flow)

1. 200 µl solution of pure OTS in cyclohexane, anhydrous grade, prepared in glove box so to obtain a final concentration of 1 mMol/l, see point 6;
2. Trough filled with 60 ml of cyclohexane, HPLC grade, in laminar flow;
3. Previously prepared OTS solution quickly added to the cyclohexane and mixed with a pipette tip;
4. Substrate (pre-loaded on a substrate rack) immerged in the trough;
5. Trough topped up with extra 3 ml cyclohexane and closed with a glass lid. The final solution (63 ml) contain OTS at a concentration of 1 mMol/l;
6. Substrates kept for 18 minutes in the OTS solution;
7. Substrates removed from the OTS solution, quickly rinsed twice in clean Cyclohexane, and then are blown dry with nitrogen gun.

Contact Angle Assessment

The water-drop test on the treated silicon is a quick test to qualitatively assess the effect of the OTS on the silicon substrates, see Fig. 3. Note that quantitative assessment has previously shown this routine to produce contact angles of ~110° and this test is used as a quick reference to ensure fabrication has functioned correctly.

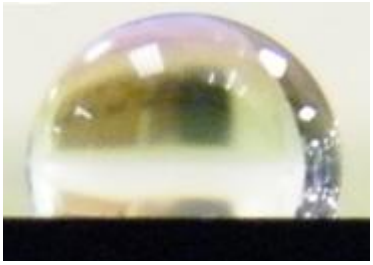

Figure 3. Drop of D.I. water on OTS treated surface: notice the contact angle between the substrate and the liquid: θ_{sl} >>90^{o}

P3HT (M104) spin coating (glove box)

1. 30 µl of Organic Semi-Conductor (OSC) solution delivered on the middle of the substrate and then spin coated at 1000 RPM for 10 s followed by 60 s at 2000 RPM;
2. Cotton swab soaked in chlorobenzene to thoroughly wipe clean the contact pads and the rest of the substrates with the exception of the area around the channel;
3. High precision cotton swab to clean between devices to avoid cross-talking and reduce leakage;
4. Substrates annealed at 90 ^{o}C for 30 minutes;
5. Cooled down for ten minutes;
6. Five devices per substrate automatically characterised using Ossila FACT1 in glove box, see Fig 4;
7. Second annealing at 120 ^{o}C for 20 minutes, slow cooling down at room temperature and measurement;
8. Annealing at 150 ^{o}C for 20 minutes, slow cooling down at room temperature and measurement.

A total of fifteen devices (three substrates) were prepared: Sub 14, 15 and 17. In the following, Dev 14.1 refers to device 1 (the closest to the gate pads) on substrates 16 and so forth.
The OFET characterisation are carried out using Ossila FACT1, see Fig 3.

Results

The yield of working OFETs was 85% and was solely determined by failure in channel wetting due to OTS treatment. For data analysis purpose, we included the best 12 OFETs (in term of mobility) with the below plots in figure 5 showing the typical output characteristics for a device and figure 6 showing the transfer characteristics for all devices under different annealing conditions.

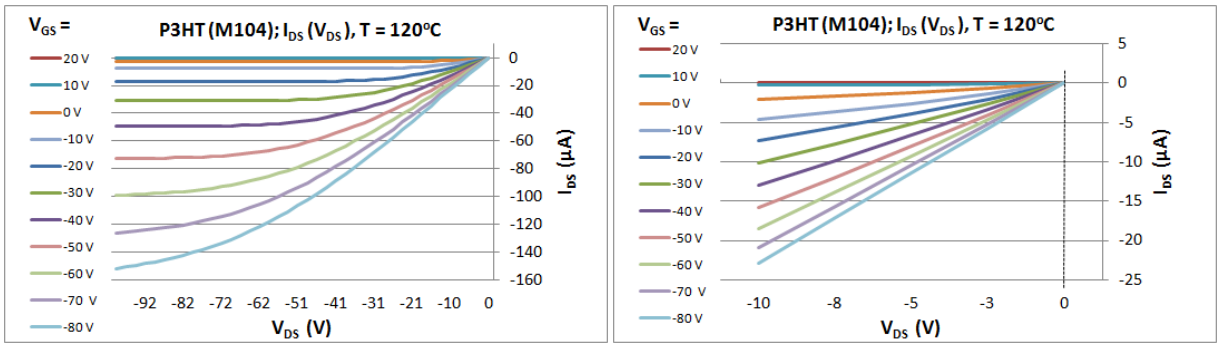

Figure 5. Left side: Output Characteristics (I-V) for and Dev14.2. Right side: details of the linear region for the same device.

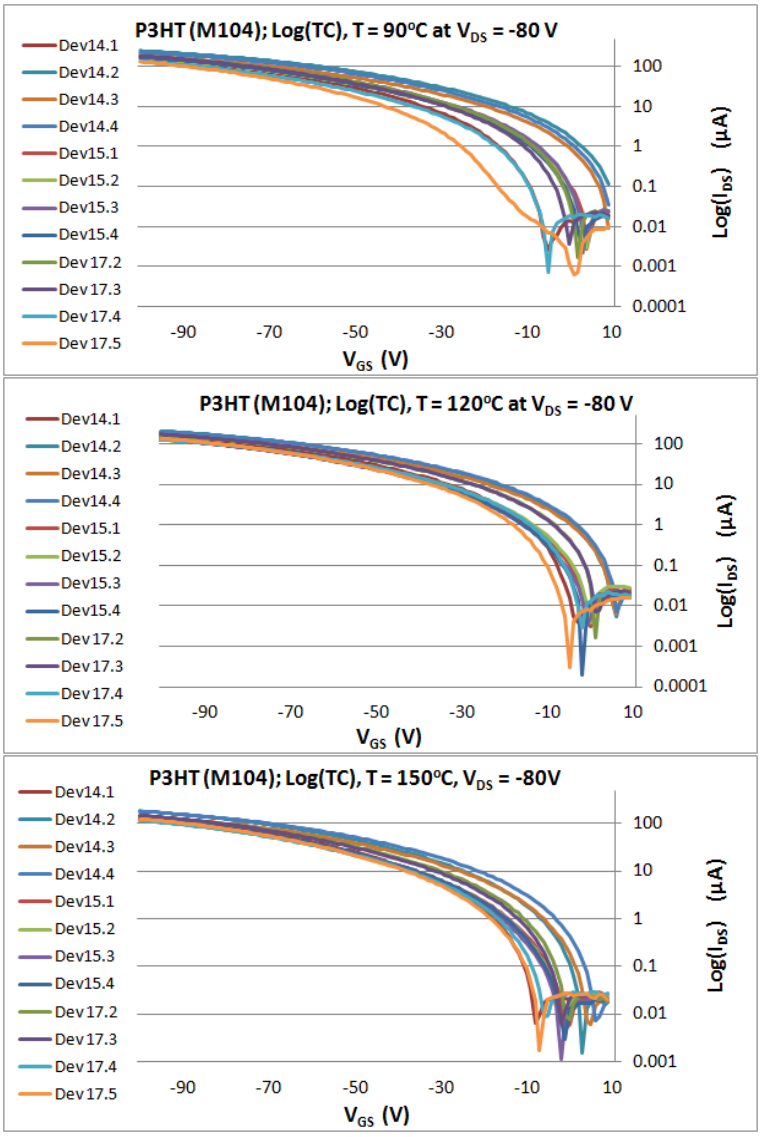

Figure 6. Absolute value of the saturation transfer characteristics in semi-log scale, Log(I_{GS}), at V_{DS} = -80 V versus V_{GS} at the three annealing temperatures 90°C, 120°C and 150°C

Mobility. The saturation (μ_{Sat}) and linear (μ_{Lin}) field effect mobility are plotted in Fig. 7, first row, for the three annealing temperatures. The saturation mobility is extracted from the output

characteristics of the transistors operating in saturation regime at V_{DS} -80 V, while the linear mobility is calculated with the transistor operating in linear regime at V_{DS} =-5 V, for more details on mobility calculations refers to App. A

After the first annealing at T = 90 °C, the OFETs afford saturation mobility ranging from a minimum of 0.12 $cm^2/(V{\cdot}s)$ to a maximum of 1.44 $cm^2/(V{\cdot}s)$ with an average mobility and standard deviation of 0.129 $cm^2/(V{\cdot}s)$ ± 0.01. Considering the modest channel width to length ratio (W=1×10^3 µm; L=30 µm; W/L ≈ 33), this is an excellent result for a bottom contact gold electrode.

Both μ_{Sat} and μ_{Lin} decrease with the successive annealing steps. This behaviour can be ascribed to 1) a deterioration of the transistor performance due to the application of three consecutive annealing/measurement cycles to the substrates (short lifetime is a well-known, often swept-under-the-carpet, open issue for OFET technology) and 2)the damage that temperature above 90 °C can inflict to the PFBT monolayer.

Threshold voltage (V_T), OFF current (I_{OFF}) and ON/OFF ratio are reported in the table below. For the definition of the OFET parameters used in this table, refers to App A.

Ann. Temp.	V_T (V)	I_{OFF} (µA)	V^{eff}_T (V)	I^{eff}_{OFF} (nA)	ratio LOG(ON/OFF)
90 °C	-9.0±7.9	-1.8±1.1	2.3±5.6	-19.5±32	3.3/5.3
120 °C	-10.5±5.4	-1.1±0.6	-0.1±3.8	-7.8±3.7	4.0/5.0
150 °C	-11.2±5.5	-0.9±0.4	-1.6±4.2	-7.4±5.6	3.9/5.0

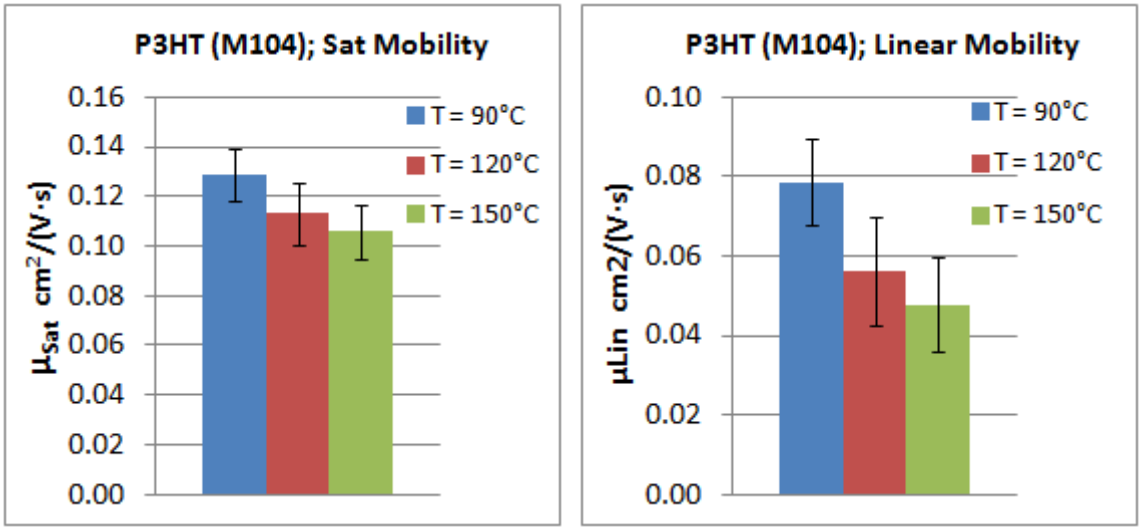

Figure 7 Saturation and linear mobility for P3HT (M104) transistors for the three annealing temperatures 90°C, 120°C and 150°C in the case of initial spin speed of 1000RPM. The width of the bars represents two standard deviations, i.e. 2×σ.

Leakage Current. The leakage current was well below the one-percent drain current threshold limit (i.e., $I_{leak} < 0.01\ I_{DS}$) required by the IEEE Std 1620-2008, "*IEEE Standard for Test Methods for the Characterization of Organic Transistors and Materials*".

Appendix A - Mobility Estimation

The field effect mobility, μ, for OFET is a function of the gate voltage and is calculated from the following equations -

$$\mu_{Lin} \approx \frac{1}{C_{ox}} \frac{1}{V_{DS}} \frac{L}{W} \frac{\partial I^{lin}{}_{DS}}{\partial V_{GS}} \quad ;$$

$$\mu(V_{GS}) = \frac{2L}{W} \frac{1}{C_{ox}} \frac{\partial \sqrt{I_{DS}^{sat}}}{\partial V_{GS}} \quad \text{Eq.1}$$

L and *W* are the length and width of the channel, while C_{ox} is the capacitance per unit area. $\frac{\partial I^{lin}{}_{DS}}{\partial V_{GS}}$ and $\frac{\partial \sqrt{I_{DS}^{sat}}}{\partial V_{GS}}$ are the derivative of the drain current (root square of I_{DS}) measured with the transistor operating in linear (saturation) mode.
Unfortunately, the simplest algorithms for numerical differentiation produce outcomes that can be affected by non-negligible numerical error and, most importantly, amplifies the noise embedded in the measurement data carried out in noisy environment such as glove boxes and clean rooms. With this in mind, we modified Eq. 1 as follow -

1. The measured data $I_{DS}(V_{GS})$ are partitioned in consecutive ten-points subsets;
2. For each subset, the linear fit and its slope $\alpha(V_{GS})$ are calculated;
3. For the saturation mobility, the linear fit is calculated with respect to the square of I_{DS};
4. The slope of the linear fit is then inserted in Eq. 1 instead of the derivative

$$\mu_{Lin}(V_{GS}) \approx \frac{1}{C_{ox}} \frac{1}{V_{DS}} \frac{L}{W} \alpha_{Lin}(V_{GS}) \quad ;$$

$$\mu_{Sat}(V_{GS}) = \frac{2L}{W} \frac{1}{C_{ox}} \alpha_{Sat}(V_{GS}) \quad \text{Eq.2}$$

5. Statistical parameters, such as the Root Mean Square Error and the coefficient of determination, R^2, are calculated in order to determine the "Goodness of fit", i.e. to estimate the agreement between experimental data and a linear current-voltage law.
6. The gate-voltage dependent mobility is then taken as the value given by Eq. 2 where α_{Lin} (α_{Sat}) calculated from the subset of the measured I_{DS} that best fits a liner relationship between the gate current (square of I_{DS}) and gate voltage, see point 5.

In general, the data subset for which the condition 6 above is satisfied gives also the maximum mobility with a remarkable "goodness of fit": Root Mean Square Error < 0.000001 and coefficient of determination, R^2, ≈ 1. Note that for a perfect linear relationship, Root Mean Square Error = 0 and R^2 = 1

The saturation mobility, $\mu_{Sat,}$ for the samples analysed for this work was found indeed to be strongly depended on the gate voltage, with the maximum mobility located at V_{GS} ranging from -50 to -59 V or -60 to -69 V.

Threshold Voltage, off current and ON/OFF ratio. The threshold voltage (V_T) is calculated from the *x*-intercept of the linear fit of the portion of the output characteristic used to extract the mobility ($I_{DS}(V_{GS})$, with V_{DS} = -80 V). The OFF current is therefore given by $I_{OFF}= I_{DS}(V_T)$, while the ON current is the maximum of I_{DS}. With these definitions, V_T and I_{OFF} tend to be overestimated, with the former to be intended not a proper threshold, but a good indicator of the gate voltage at which I_{DS} becomes substantial.

We therefore also report the standard IEEE definition of the "effective" OFF current as the minimum of I_{DS} (I^{eff}_{OFF}) and relative threshold voltage V^{eff}_T, the latter defined through the relation $I^{eff}_{OFF} = I_{DS}(V^{eff}_T)$.

References

[1] Zhenan Bao and Jason Locklin (Editor), *Organic Field-Effect Transistors*, CRC Press.

[2] *Two-dimensional charge transport in self-organized, high-mobility conjugated polymers*; H. Sirringhaus et al., Nature, V401, P685-688 (1999)

[3] *Controlling the field-effect mobility of regioregular polythiophene by changing the molecular weight*, R.J.Kline et al., *Adv. Mater*, V15*, P*1519, (2003)

[4] *Soluble and processable regioregular poly(3-hexylthiophene) for thin film field-effect transistor applications with high mobility*, Z. Bao et al., Appl. Phys. Lett., V69*, P*4108–4110, (1996)

[5] *Enhancement of field-effect mobility due to surface-mediated molecular ordering in regioregular polythiophene thin film transistors*, D.H. Kim et al., *Adv. Func. Mater.*, V15*, P*77–82, (2005)

[6] *Effect of molecular weight and annealing of poly (3-hexylthiophene)s on the performance of organic field-effect transistors*, A. Zen et al., Adv. Func. Mater, V14, P757–764, (2004)

[7] *Nanostructure dependence of field-effect mobility in regioregular poly(3-hexylthiophene) thin film field effect transistors*, R. Zhang,. J. Am. Chem. Soc., V28, *P*3480–3481, (2006)

[8] *High mobility conjugated polymer field-effect transistors,* H. Sirringhaus et al., Advances in Solid State Physics, V39, P101–110, (1999)

[9] *Relationship between the microscopic morphology and the charge transport properties in poly(3-hexylthiophene) field-effect transistors,* M. Surin et al,. J. Appl. Phys., V100**,** 033712 (2006)

[10] *Dependence of field-effect mobility and contact resistance on nanostructure in regioregular poly(3-hexylthiophene) thin film transistors,* K.A. Singh et al*,.* Appl. Phys*.* Lett. V92, 263303 (2008)

[11] *Controlled One-Dimensional Nanostructures in Poly(3-hexylthiophene) Thin Film for High-Performance Organic Field-Effect Transistors,* D.H. Kim et al., J. Phys. Chem. B*,* V110(32) PP15763–15768 (2006)

[12] *Enhanced Mobility of Poly(3-hexylthiophene) Transistors by Spin-Coating from High-Boiling-Point Solvents;* J-F. Chang et al*.,* Chem. Mater., V16 (23), P4772–4776 (2004)

[13] *General observation of n-type field-effect behaviour in organic semiconductors,* L-L. Chua*,* Nature, V434, P194-199 (2005)

[14] Taylor J.R. *Introduction to error analysis, 2ed,* University Science Books,U.S.