# VS23S010D   Datasheet

# VS23S010D-L - 1 Megabit SPI SRAM
## with Serial and Parallel Interfaces
## and Integrated Video Display Controller

## Features

- Flexible 1.5V - 3.6V operating voltage
- 131,072 x 8-bit SRAM organization
- Serial Peripheral Interface (SPI) mode 0 compatible
    - Byte, Page and Sequential modes
    - Supports Single, Dual and Quad I/O read and write
    - Fast operation: the whole memory can be filled in 262158 or read in 262159 cycles (Quad-I/O SPI, Quad address mode)
    - XHOLD and XWP pins
- 8-bit Parallel Interface (Simplified 8080 and NAND FLASH Type Interface)
    - Sequential read and write in 4 byte blocks
    - Fast operation, the whole memory can be filled or read in 131077 cycles
- Integrated Video Display Controller with Video DAC
    - Supports NTSC and PAL video formats
    - Fully configurable by user
    - 9-bit Video DAC and 8x Video PLL
- High operating frequencies
    - Up to 38 MHz for SPI
    - Up to 40 MHz for 8-bit parallel interface
    - Over 35 MHz for Video Display Controller
    - (TBD) MHz for SRAM writes when Video Display Controller enabled
- Active Low-power
    - Read current 340 $\mu$A at 1 MHz (Single I/O, SO=0, $T_A$=+85$^\circ$C, VDD=3.3V)
- Industrial temperature range
    - -40$^\circ$C to + 85$^\circ$C
- Pb-Free and RoHS compliant

## Description

The VLSI Solution VS23S010D-L is an easy-to-use and versatile serial SRAM device. The memory is accessed via an SPI compatible serial bus. The device also contains Video Display Controller, which can be configured to continuously output analog composite video from the memory array data to implement a video frame buffer.

Alternatively, a 8-bit parallel interface can be used to access the SRAM instead of the SPI.

To sum up, there are four separate operating modes in VS23S010D-L:

- SPI Single, Dual, or Quad operation and 4 General Purpose I/O pins
- SPI Single, Dual, or Quad operation and simultaneous Video Display Controller
- 8-bit Parallel Interface operation
- 8-bit Parallel Interface operation and simultaneous Video Display Controller

## Applications

- Micro-controller RAM extension
- VoIP and internet data stream buffer
- Audio data buffer
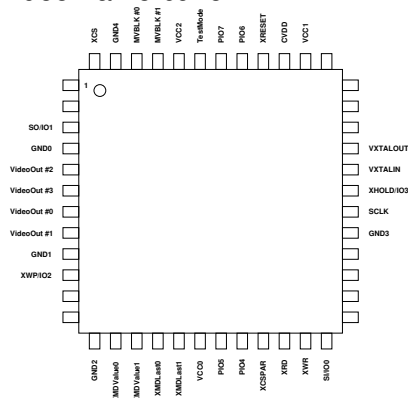- Video frame buffer



Figure 1: LQFP48 pin out (not to scale)

## Operating Modes

VS23S010D-L operates in one of four modes: SPI, SPI and Video Display Controller, 8-bit parallel mode or 8-bit parallel mode and Video Display Controller.
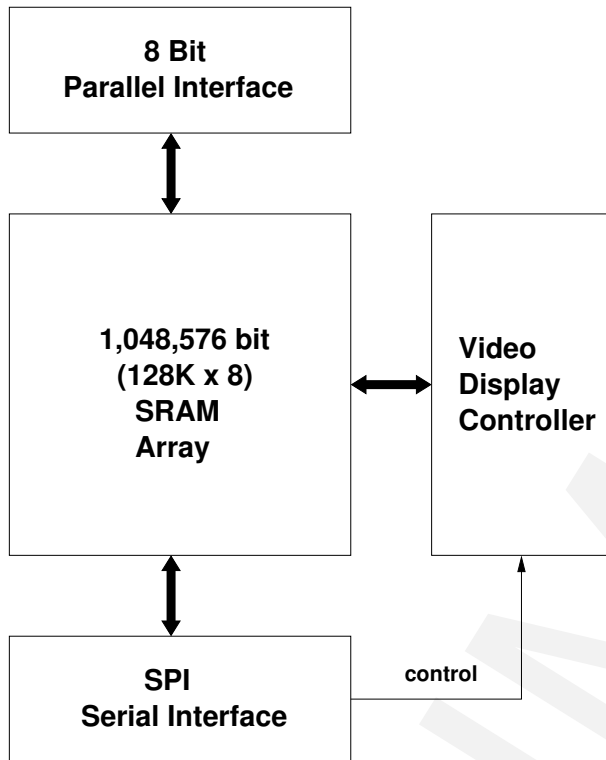


Figure 2: SPI or 8-bit parallel interface and Video Display Controller can be enabled at the same time.

In SPI mode SRAM and control registers can be accessed. Dual-I/O and Quad-I/O modes are used only for SRAM read and write.

When Video Display Controller is enabled SPI can be used simultaneously. There is an additional limit to maximum SPI access rate in this mode.

When 8-bit parallel interface is used to access SRAM, SPI must be inactive. Video Display Controller can be operational simultaneously. However, Video Display Controller can be controlled only by SPI. There is a limit to maximum access rate for 8-bit parallel interface when Video Display Controller is en-
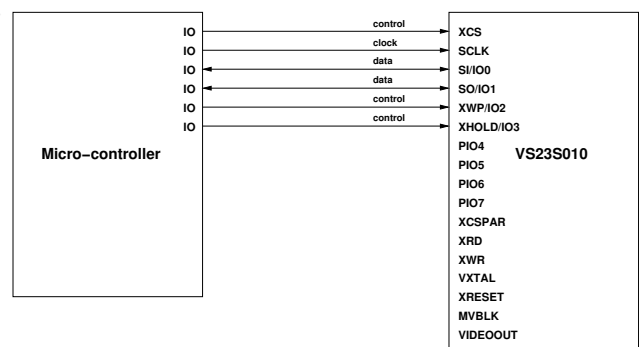
abled.

Following are connection examples for different operating modes. Some I/Os of VS23S010D-L are unconnected, because they have internal pull-up or pull-down resistors. Note also, that power and ground connections are not shown in the following examples.
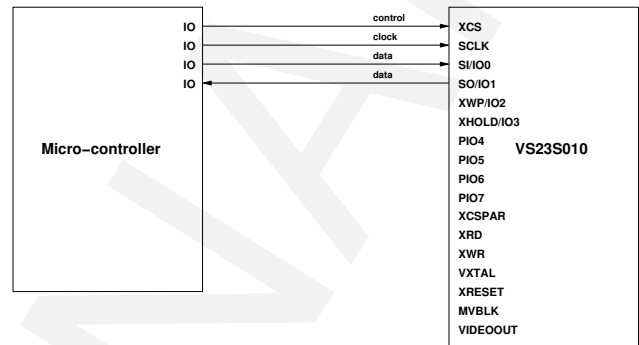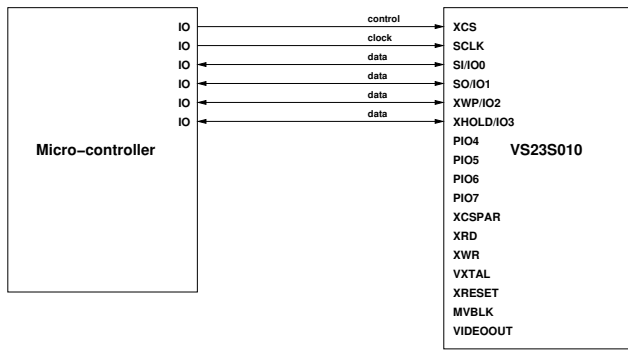


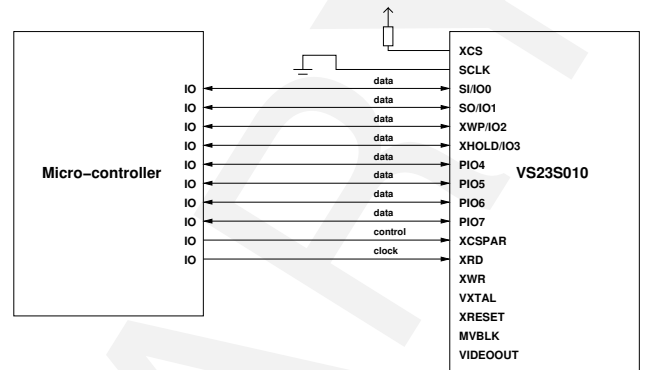SPI connection, minimum configuration
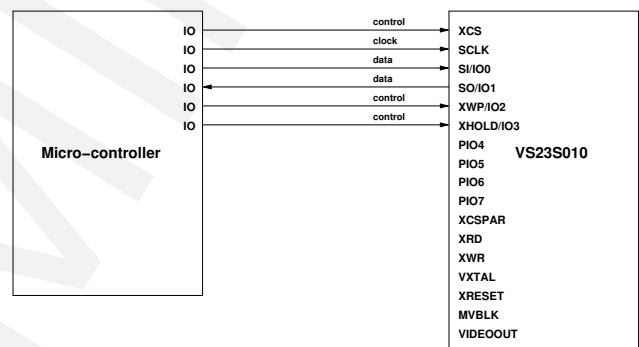


SPI connection, basic configuration



SPI Dual–I/O connection

SPI Quad–I/O connection



8–bit parallel interface (minimum configuration, one clock is enough)
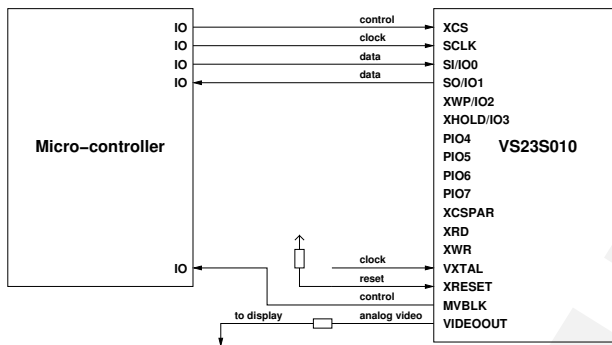


SPI connection (minimum configuration), video generator enabled
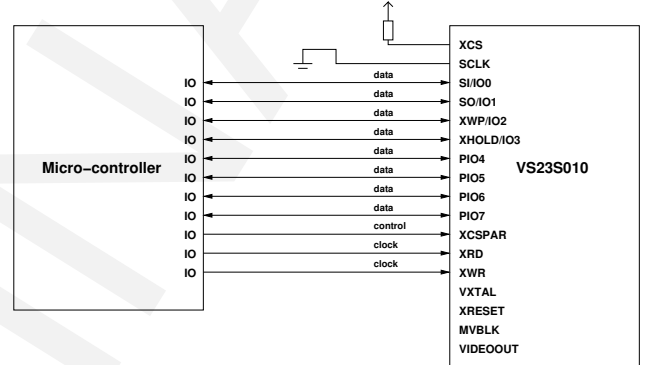


8–bit parallel interface
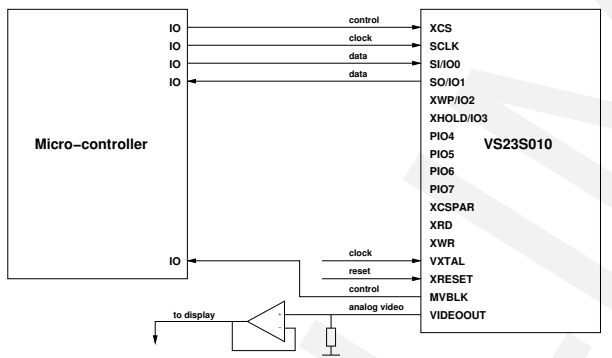


SPI connection (minimum configuration), video generator enabled, video buffer



8–bit parallel interface, video generator enabled, video buffer
(SPI for video generator control when 8–bit interface is not active)



SPI Quad–I/O connection, video generator enabled, video buffer

# Contents

## List of Figures

# 1 Disclaimer

This is a *preliminary* data sheet. All properties and figures are subject to change.

# 2 Definitions

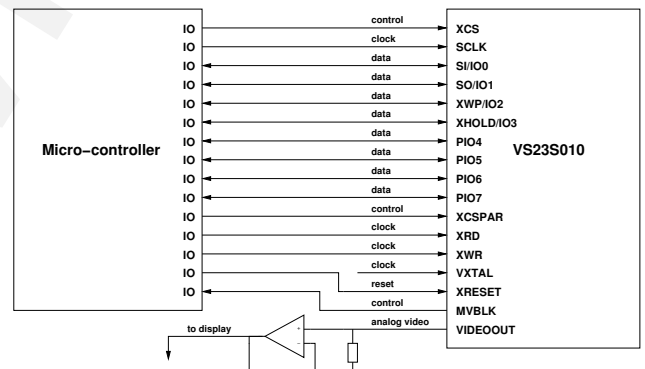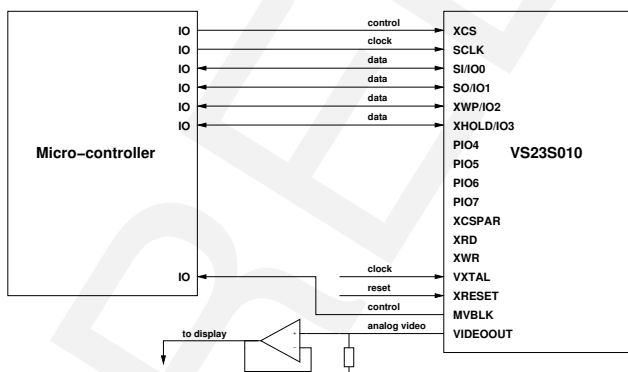**B** Byte, 8 bits

**b** Bit

**CSClk** Clock, which frequency is Color Subcarrier Frequency of a video format.

**GPIO** General Purpose I/O

**LSB** Least Significant Bit

**MSB** Most Significant Bit

**NTSC** National Television System Committee video format, color subcarrier frequency is 3.579545 MHz.

**PAL** Phase Alternating Line video format, color subcarrier frequency is 4.43361875 MHz.

**POR** Power On Reset

**SPI** Serial Peripheral Interface

**SRAM** Static Random Access Memory

**TBD** To Be Defined

**U, V** Chrominance components (color information)of video signal

**VClk** Video Display Controller clock of the VS23S010D-L. It can come directly from VXTAL oscillator or can be generated on-chip by 8x PLL from VXTAL pins. **VClk frequency has to be 8 times the color subcarrier frequency of the selected analog video format.**

$$F_{VClk} = 8 \times F_{CSClk}$$

If on-chip PLL is used, the VXTAL clock frequency is 3.579545 MHz for NTSC and 4.43361875 MHz for PAL video. If Video Display Controller clock is directly from the VXTAL pins without using the on-chip PLL, then VXTAL clock frequency is 28.63636 MHz for PAL and 35.46895 for NTSC video.

**Y** Luna component (the brightness) of video signal

# 3   Electrical Characteristics & Specifications

## 3.1   Absolute Maximum Ratings

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| Positive Supply | VDD | -0.3 | 3.6 | V |
| Core Supply | CVDD | -0.3 | 1.98 | V |
| Current at any non-power pin[1] | | | ±50 | mA |
| Voltage at any digital input | | -0.3 | VDD+0.3[2] | V |
| Operating temperature | | -40 | +85 | °C |
| Storage temperature | | -65 | +150 | °C |
| ESD protection on any pin[3] | | 2.0 | | kV |

[1] Higher current can cause latch-up.

[2] Must not exceed 3.6 V

[3] Human Body Model (HBM) MIL-STD-883E Method 3015.7

## 3.2   DC Characteristics

$T_A$ = -40 ... +85 °C

| Parameter | Min | Max | Unit | Test Conditions |
|---|---|---|---|---|
| Positive supply voltage | 1.5 | 3.6 | V | |
| High-level input voltage | $0.7 \times$VDD | VDD+0.3[1] | V | |
| Low-level input voltage | -0.2 | $0.3 \times$VDD | V | |
| Low-level input voltage | -0.2 | $0.25 \times$VDD | V | Any Schmitt-trigger pin |
| High-level output voltage | $0.7 \times$VDD | | V | $I_O$ = -1.0 mA |
| Low-level output voltage | | $0.3 \times$VDD | V | $I_O$ = 1.0 mA |
| I/O leakage current [2] | -2.00 | 2.00 | $\mu$A | Pin as input or High-Z |
| Pull-up current | -7.50 | -1.00 | $\mu$A | Any pull-up pin |
| Pull-down current | 0.50 | 5.00 | $\mu$A | Any pull-down pin |
| I/O capacitance [3] | | 6 | pF | VDD=0V, f=0.5 MHz, $T_A$=+25 °C |
| RAM data retention voltage [3,4] | | 0.9 | V | |
| Start-up time after power-up [5] | | 100 [3] | $\mu$s | |
| DAC output load | 75 | | $\Omega$ | |
| DAC output level (code 000h) | -10 | 10 | mV | VDD $\geq$ 3.0 V, 150 $\Omega$ load |
| (code 1FEh) | 2.000 | 2.200 | V | |

[1] Must not exceed 3.6V

[2] Excluding the pins with pull-up or pull-down resistors

[3] This parameter is periodically sampled and is not 100% tested.

[4] This is the limit to which VDD can be lowered without losing RAM data.

[5] Refer to Chapter 10 for additional information.

## 3.3  AC Characteristics

### 3.3.1  General

VDD = 3.3 V, $T_A$ = -40 ... +85 °C

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| Data clock high time | Tclkh | $0.5 * T_{MAX}$ [1] | | ns |
| Data clock low time | Tclkl | $0.5 * T_{MAX}$ [1] | | ns |
| Data clock rise time [2,3] | Tclkr | | 2 | $\mu$s |
| Data clock fall time [2,3] | Tclkf | | 2 | $\mu$s |
| Data in setup time | Tds | 2 | | ns |
| Data in hold time | Tdh | 6 | | ns |
| Output disable time [2] | Tdis | | 15 | ns |
| Output valid time | Tv | | 30 | ns |
| Output hold time | Toh | 6 | | ns |

[1] $T_{MAX}$ is the minimum clock cycle time in each mode.

[2] This parameter is periodically sampled and is not 100% tested.

[3] Refer to Chapter 10 for additional information.

### 3.3.2  SPI Mode

VDD = 3.3 V, $T_A$ = -40 ... +85 °C

| Parameter | Symbol | Min | Max | Unit | Test Conditions |
|---|---|---|---|---|---|
| SPI clock frequency [1] | $F_{SCLK}$ | | 32 | MHz | VDD = 1.5 V |
| | | | 38 | MHz | VDD $\geq$ 1.8 V |
| XCS high time | Txcshi | 31 | | ns | VDD = 1.5 V |
| | | 26 | | ns | VDD $\geq$ 1.8 V |
| XCS setup time | Txcss | 4 | | ns | |
| XCS hold time | Txcsh | 0 | | ns | |
| XHOLD setup time | Txhs | 2 | | ns | |
| XHOLD hold time | Txhh | 1 | | ns | |
| XHOLD low to output High-Z [2] | Txhlz | 4 | | ns | |
| XHOLD high to output valid [2] | Txhhz | | 16 | ns | |
| XWP setup time | Txws | 1 | | ns | |
| XWP hold time | Txwh | 1 | | ns | |

[1] When used with an external micro-controller the maximum SPI frequency is based on the total of VS23S010D-L and micro-controller I/O-delays and routing delays of the card.
[2] This parameter is periodically sampled and is not 100% tested.
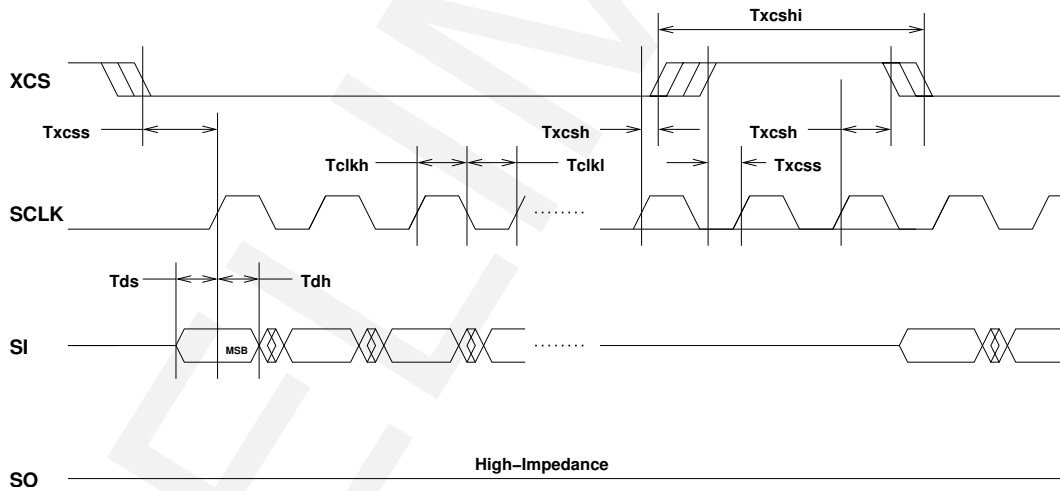


Figure 3: SPI Input Timing
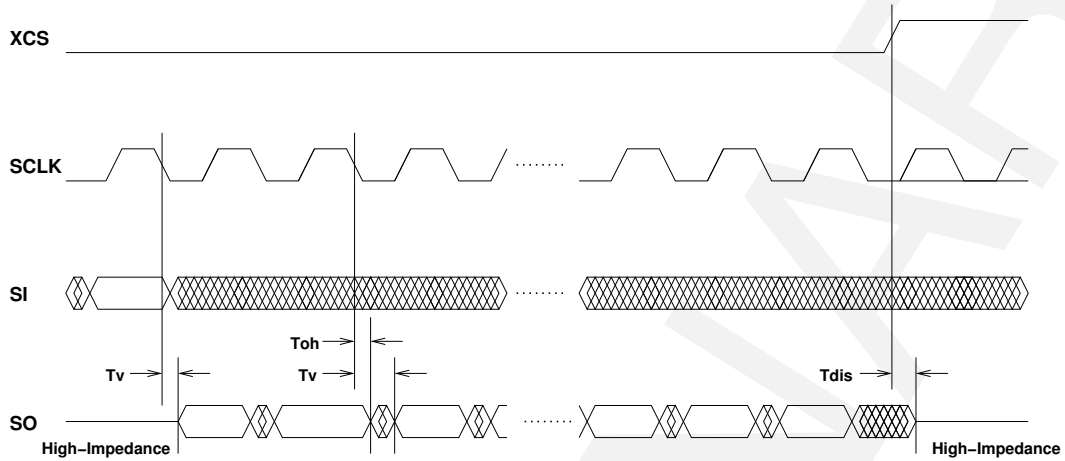
Figure 4: SPI Output Timing
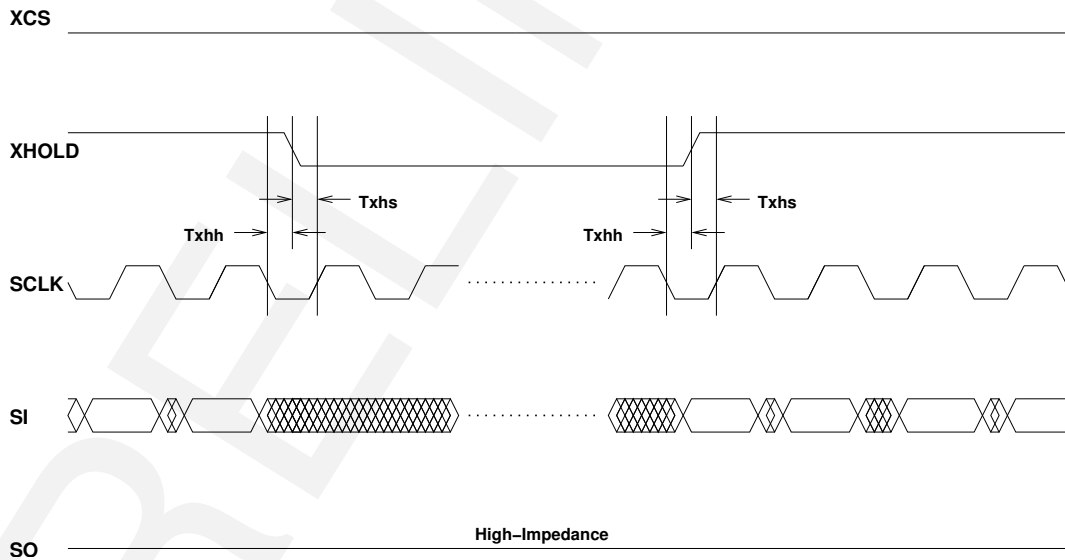


Figure 5: XHOLD Timing, SPI and Dual-I/O Input Modes. Notice that internal address counter does not increment, when XHOLD is low.
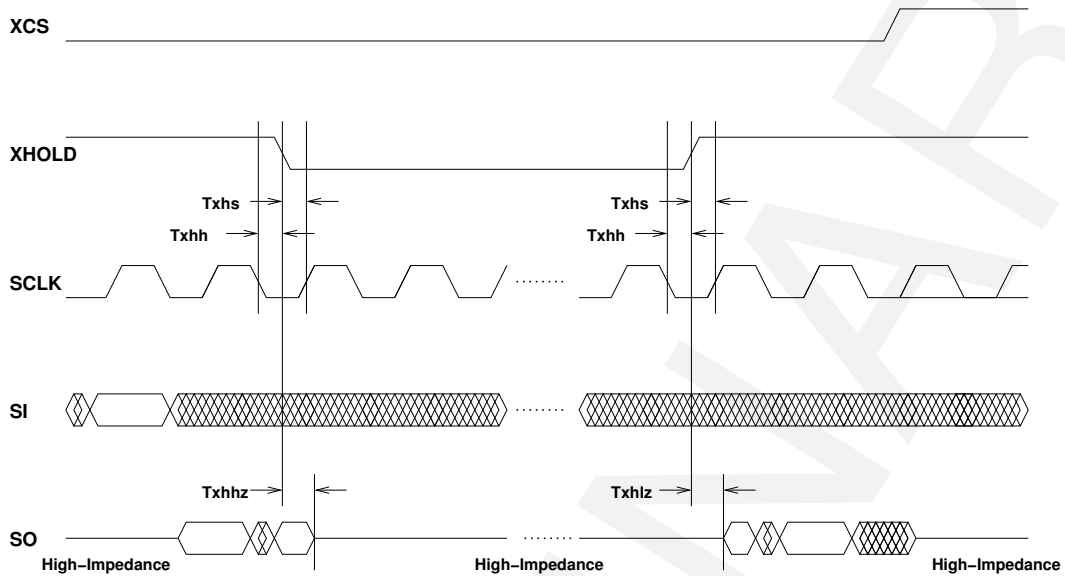
Figure 6: XHOLD Timing, SPI and Dual-I/O Output Modes. Notice that internal address counter does not increment, when XHOLD is low.
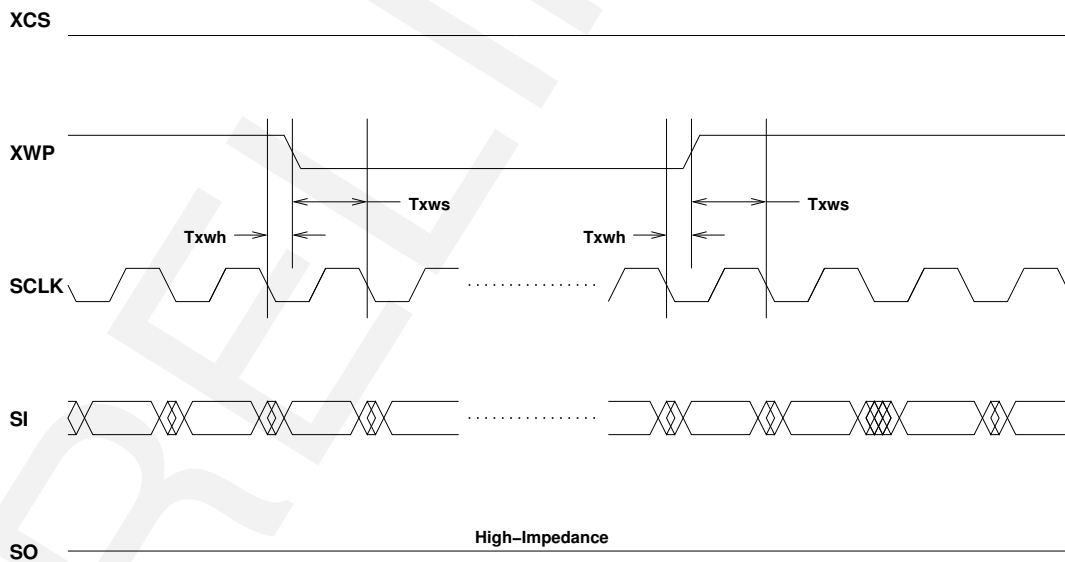


Figure 7: XWP Timing, SPI and Dual-I/O Modes. Notice that internal address counter increments, when XWP is low.

### 3.3.3   Video Display Controller Mode

VDD $\geq$ 3.0 V, $T_A$ = -40 ... +85 $^\circ$C

| Parameter | Symbol | Min | Typ [3] | Max | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| VXTAL frequency when PLL used | $F_{VXTALP}$ | 2.6 [1] | | 4.5 | MHz | |
| VXTAL frequency when PLL not used | $F_{VXTALXP}$ | - | | 35.5 | MHz | |
| XRESET active time [1,2] | Txresl | $T_{VXTAL}$ +20 | | | ns | |
| XRESET inactive to ready [1] | Txresv | | | $4 * T_{VClk}$ +10 | ns | |
| **High current mode, 75 $\Omega$ load** | | | | | | |
| Output level: | | | | | | |
| code 000h (Sync level) code 0FFh | Levprhc | -18 555 | -2 667 | 18 690 | mV mV | Protoline |
| code 066h (Black level) code 165h (White level) | Levpihc | 217 795 | 264 937 | 285 1073 | mV mV | Picture line |
| code 1FEh | Levdmhc | 1.200 | 1.356 | 1.400 | V | Direct mode |
| Output rise time | Tdacorfhc | | | | ns | |
| Output settling time | Tdacoshc | | | | ns | |
| Differential nonlinearity error | DNLdachc | | +1.4/-1.4 +1.2/-1.0 | +2.3/-2.3 +2.3/-2.3 | LSB LSB | Protoline Picture line |
| Integral nonlinearity error | INLdachc | | +1.4/-1.7 +1.6/-1.3 | +2.3/-3.3 +2.7/-2.7 | LSB LSB | Protoline Picture line |
| **Low current mode, 75 $\Omega$ load** | | | | | | |
| Output level: | | | | | | |
| code 000h (Sync level) code 0FFh | Levprlc | -3 45 | -1.7 53 | 3 57 | mV mV | Protoline |
| code 066h (Black level) code 165h (White level) | Levpilc | 17 64 | 20 76 | 24 80 | mV mV | Picture line |
| Output rise time | Tdacorflc | | | | ns | |
| Output settling time | Tdacoslc | | | | ns | |

[1] This parameter is periodically sampled and is not 100% tested.

[2] Note that XRESET affects only to Video Display Controller logic.  Video Display Controller control registers are not reset by XRESET.

[3] Typical values are given at +25 $^\circ$C.
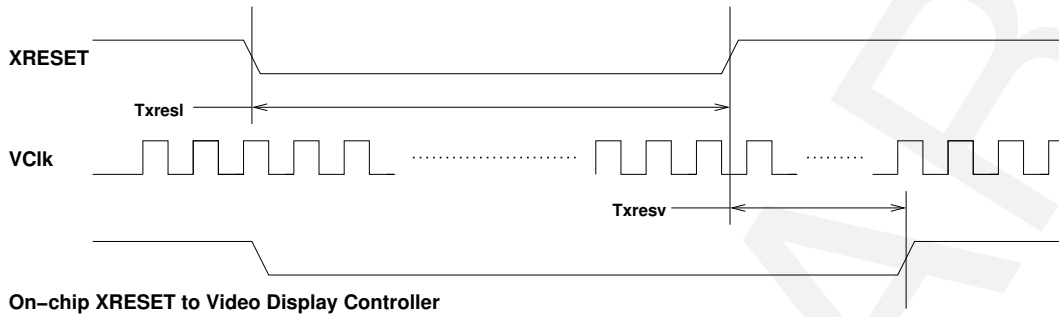
Figure 8: XRESET Timing
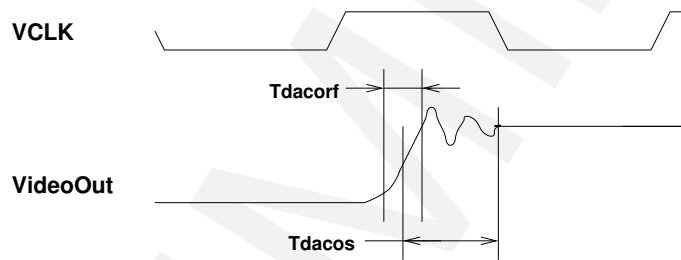


Figure 9: VideoOut Timing
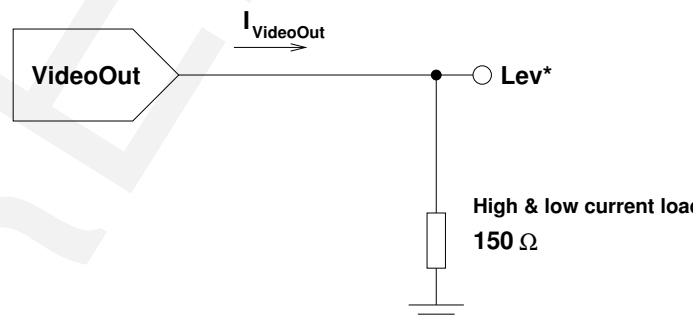


Figure 10: VideoOut Level Measurement

### 3.3.4   8-bit Parallel Interface Mode

VDD = 3.3 V, T$_A$ = -40 ... +85 °C

| Parameter | Symbol | Min | Max | Unit | Test Conditions |
|---|---|---|---|---|---|
| Clock frequency [1] | F$_{XRD\_XWR}$ | | 32 | MHz | VDD = 1.5 V |
| | | | 34 | MHz | VDD = 1.8 V |
| | | | 40 | MHz | VDD = 3.0 V |
| XCSPAR high time | Txcphi | 31 | | ns | VDD = 1.5 V |
| | | 29 | | ns | VDD = 1.8 V |
| | | 25 | | ns | VDD = 3.0 V |
| XCSPAR setup time | Txcps | 1 | | ns | |
| XCSPAR hold time | Txcph | 0 | | ns | |

[1] When used with an external micro-controller the maximum 8-bit Parallel Interface frequency is based on the total of VS23S010D-L and micro-controller I/O-delays and routing delays of the card.
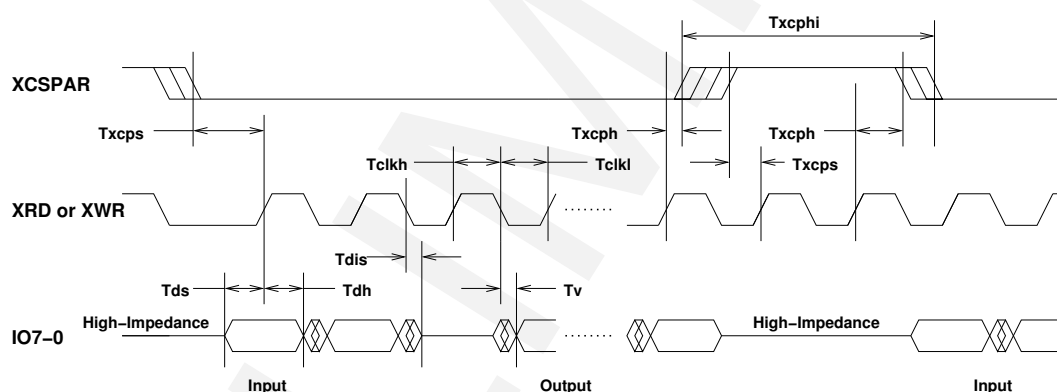


Figure 11: 8-bit Parallel Interface Timing

**AC Test Conditions**

| AC Waveform: | |
|---|---|
| Input pulse level | $0.1 \times$VDD to $0.9 \times$VDD |
| Input rise/fall time | (TBD) ns |
| Operating temperature | -40 °C to +85 °C |
| C$_L$ = (TBD) pF | |
| **Timing Measurement Reference Level:** | |
| Input | $0.5 \times$VDD |
| Output | $0.5 \times$VDD |

## 3.4  Current Consumption

$T_A$ = +25 °C, XCS=VDD, SI=SO=SCLK=GND, other inputs connected to VDD or GND by on-chip pull-up or pull-down resistors of the pins.

| Parameter | Min | Typ | Max | Unit | Test Conditions |
|---|---|---|---|---|---|
| Stand-by current [1] | | 40-65 | (TBD) | $\mu$A | |
| | | | 300 [2] | $\mu$A | $T_A$ = +85 °C |
| | | | 1000 [2] | $\mu$A | $T_A$ = +125 °C |

[1] Additional information is in Chapter 10

[2] This parameter is periodically sampled and is not 100% tested.

### 3.4.1  SPI Mode

VDD = 3.3 V, $T_A$ = +85 °C, these parameters are periodically sampled and are not 100% tested.

| Parameter | Min | Typ | Max | Unit | Test Conditions |
|---|---|---|---|---|---|
| VDD current, SPI single output read | | | 340 | $\mu$A | $F_{SCLK}$ = 1 MHz, SO = 0 |
| | | | 740 | $\mu$A | $F_{SCLK}$ = 10 MHz, SO = 0 |
| | | | 1.3 | mA | $F_{SCLK}$ = 24 MHz, SO = 0 |
| VDD current, SPI single port write | | 0.1-1.3 | | mA | $F_{SCLK}$ = 1 MHz, $T_A$ = +25 °C |
| & read, two patterns[1] | | 1.0-2.7 | | mA | $F_{SCLK}$ = 10 MHz, $T_A$ = +25 °C |

[1] Current is very much data-dependent.

### 3.4.2  Video Display Controller Mode

VDD = 3.3 V, $T_A$ = +25 °C, these parameters are periodically sampled and are not 100% tested.

| Parameter | Min | Typ | Max | Unit | Test Conditions |
|---|---|---|---|---|---|
| VDD current, Video Display Controller on | | 3.8 - 18.4 | | mA | 150 $\Omega$ load |

### 3.4.3   8-bit Parallel Interface Mode

VDD = 3.3 V, T$_A$ = +85 °C, these parameters are periodically sampled and are not 100% tested.

| Parameter | Min | Typ | Max | Unit | Test Conditions |
|---|---|---|---|---|---|
| VDD current, parallel read | | | 350 | $\mu$A | F$_{XRD\_XWR}$ = 1 MHz, data out = 00h |
| | | | 750 | $\mu$A | F$_{XRD\_XWR}$ = 10 MHz, data out = 00h |
| | | | 1.4 | mA | F$_{XRD\_XWR}$ = 24 MHz, data out = 00h |
| VDD current, parallel read & write, increasing data[1] | | 0.8 | | mA | F$_{XRD\_XWR}$ = 1 MHz, T$_A$ = +25 °C |
| | | 2.2 | | mA | F$_{XRD\_XWR}$ = 10MHz, T$_A$ = +25 °C |
| | | 3.0 | | mA | F$_{XRD\_XWR}$ = 15MHz, T$_A$ = +25 °C |

[1] Current is very much data-dependent.

# 4   Packages and Pin Descriptions

## 4.1   Narrow SOIC8

Narrow SOIC8 is a lead (Pb) free and also RoHS compliant package. RoHS is a short name of *Directive 2002/95/EC on the restriction of the use of certain hazardous substances in electrical and electronic equipment*.

Narrow SOIC8 package dimensions can be found at *http://www.vlsi.fi/fileadmin/quality/soic8.pdf*.

The VS23S010D-S has the following pin out:

| Pin Name | SOIC8 Pin | Pin Type | Function | Initial State |
|---|---|---|---|---|
| XCS | 1 | DIS | Active low chip select for SPI | I |
| SO/IO1 | 2 | DIO | SO for SPI / IO1 for Dual-I/O and Quad-I/O SPI | I |
| XWP/IO2 | 3 | DIOSPU | Active low write protect for SPI and Dual-I/O SPI / IO2 for Quad-I/O SPI | IH |
| GND | 4 | GND | Ground | |
| SI/IO0 | 5 | DIO | SI for SPI / IO0 for Dual-I/O and Quad-I/O SPI | I |
| SCLK | 6 | DIS | SCLK for SPI | I |
| XHOLD/IO3 | 7 | DIOSPU | Active low Hold for SPI and Dual-I/O SPI / IO3 for Quad-I/O SPI | IH |
| VCC | 8 | PWR | Power supply | |
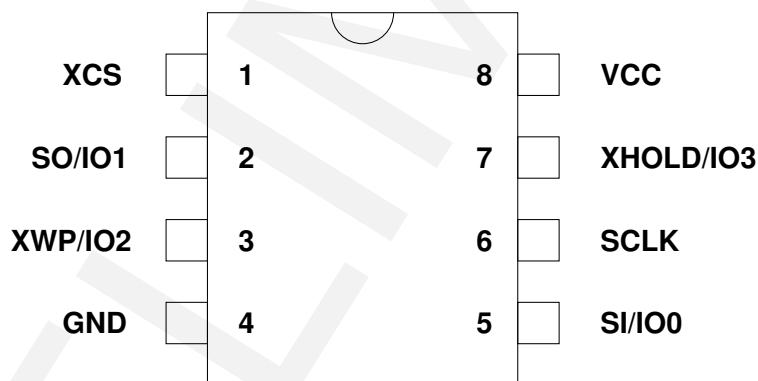


Figure 12: SOIC8 narrow package, compatible with standard pin out (not to scale).

Pin types:

| Type | Description |
|---|---|
| DIS | Digital input, Schmitt-trigger |
| DIO | Digital input/output |
| DIOSPU | Digital input/output with Pull-Up resistor, Schmitt-trigger |
| GND | Ground pin |
| PWR | Power supply pin |

Initial States of pins after power-up:

---

| Initial State | Description |
|---|---|
| I | Input, floating (3-state) |
| IH | Input, on-chip Pull-Up resistor |

## 4.2  LQFP48

LQFP48 is a lead (Pb) free and also RoHS compliant package.  RoHS is a short name of *Directive 2002/95/EC on the restriction of the use of certain hazardous substances in electrical and electronic equipment*.

LQFP48 package dimensions can be found at *http://www.vlsi.fi/fileadmin/quality/lqfp48.pdf*.

The VS23S010D-L has the following pin out:

| Pin Name | LQFP48 Pin | Pin Type | Function | Initial State |
|---|---|---|---|---|
| | 1-2 | R | | |
| SO/IO1 | 3 | DIO | SO for SPI / IO1 for Dual-I/O and Quad-I/O SPI and 8-bit parallel interface | I |
| GND0 | 4 | GND | Ground | |
| | 5-6 | R | | |
| VideoOut #0 | 7 | AO | Current-mode analog composite video output | I |
| | 8 | R | | |
| GND1 | 9 | GND | Ground | |
| XWP/IO2 | 10 | DIOSPU | Active low write protect for SPI and Dual-I/O SPI / IO2 for Quad-I/O SPI and 8-bit parallel interface | IH |
| | 11-12 | R | | |
| GND2 | 13 | GND | Ground | |
| XMDValue0 | 14 | DIPU | Multi-IC IC Id bit 0, active low | IH |
| XMDValue1 | 15 | DIPU | Multi-IC IC Id bit 1, active low | IH |
| XMDLast0 | 16 | DIPU | Multi-IC Last IC bit 0, active low | IH |
| XMDLast1 | 17 | DIPU | Multi-IC Last IC bit 1, active low | IH |
| VCC0 | 18 | PWR | Power supply | |
| PIO5 | 19 | DIOPD | IO5 for 8-bit parallel interface / GPIO1 / VGP1 for Video Display Controller | IL |
| PIO4 | 20 | DIOPD | IO4 for 8-bit parallel interface / GPIO0 VGP0 for Video Display Controller | IL |
| XCSPAR | 21 | DISPU | Active low chip select of 8-bit parallel interface | IH |
| XRD | 22 | DISPU | Clock of 8-bit parallel interface | IH |
| XWR | 23 | DISPU | Clock of 8-bit parallel interface | IH |
| SI/IO0 | 24 | DIO | SI for SPI / IO0 for Dual-I/O and Quad-I/O SPI and 8-bit parallel interface | I |
| | 25-28 | R | | |
| GND3 | 29 | GND | Ground | |
| SCLK | 30 | DIS | SCLK for SPI | I |
| XHOLD/IO3 | 31 | DIOSPU | Active low Hold for SPI and Dual-I/O SPI / IO3 for Quad-I/O SPI and 8-bit parallel interface | IH |
| VXTALIN | 32 | DIC | Clock for Video Display Controller | I |
| VXTALOUT | 33 | DOC | Clock for Video Display Controller | I |
| | 34-36 | R | | |
| | 37 | R | | |
| VCC1 | 38 | PWR | Power supply | |
| CVDD | 39 | CREG | Regulated digital core voltage, **do not connect** | |
| XRESET | 40 | DISPD | Active low reset for Video Display Controller | IL |
| PIO6 | 41 | DIOPD | IO6 for 8-bit parallel interface / GPIO2 / VGP2 for Video Display Controller | IL |
| PIO7 | 42 | DIOPD | IO7 for 8-bit parallel interface / GPIO3 / VGP3 for Video Display Controller | IL |
| TestMode | 43 | DISPD | Active high testmode select | IL |
| VCC2 | 44 | PWR | Power supply | |
| | 45 | R | | |
| MVBLK #0 | 46 | DO | Video Display Controller block move active | OL |
| GND4 | 47 | GND | Ground | |
| XCS | 48 | DIS | Active low chip select for SPI | I |

Pin types:

| Type | Description |
|------|-------------|
| AO | Current-mode analog output, external series resistor needed for voltage |
| CREG | Core regulated operating voltage pin |
| DIO | Digital input/output |
| DIOPD | Digital input/output with Pull-Down resistor |
| DIOSPU | Digital input/output with Pull-Up resistor, Schmitt-trigger |
| DIPU | Digital input with Pull-Up resistor |
| DIS | Digital input, Schmitt-trigger |
| DISPD | Digital input with Pull-Down resistor, Schmitt-trigger |
| DISPU | Digital input with Pull-Up resistor, Schmitt-trigger |
| DIC | Digital input, clock oscillator |
| DOC | Digital output, clock oscillator |
| DO | Digital output |
| GND | Ground pin |
| PWR | Power supply pin |
| R | Reserved for future use |

Initial States of pins after power-up:

| Initial State | Description |
|---------------|-------------|
| I | Input, floating (3-state) |
| IL | Input, on-chip Pull-Down resistor |
| IH | Input, on-chip Pull-Up resistor |
| OL | Output, driven low |
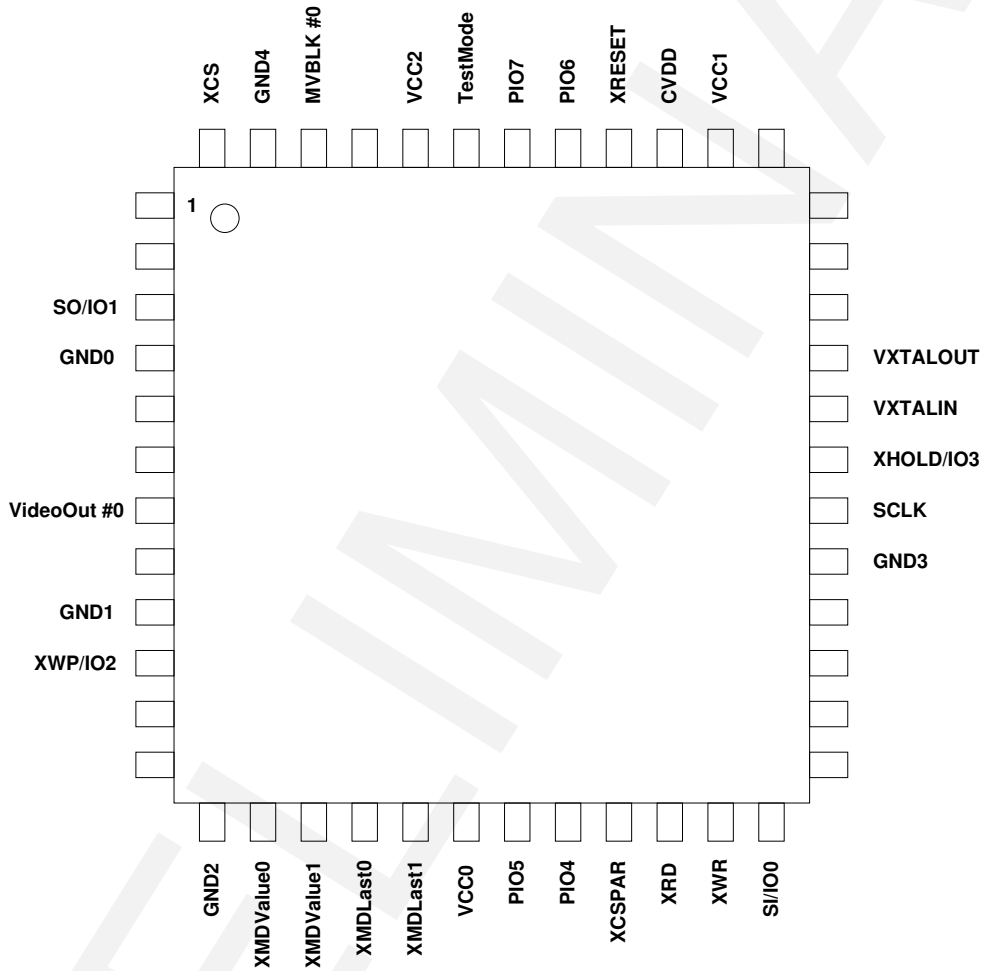
Figure 13: LQFP48 pin out (not to scale)

# 5   Connection Guidelines

To minimize power supply noise connect suitable by-pass capacitors between VCC supply pins and GND. Place by-pass capacitors as near as possible to VS23S010D-L for best effect.

VXTALIN and VXTALOUT are crystal oscillator pins for Video Display Controller.

Make sure that there is the lowest possible capacitive coupling between different clocks and chip selects  (SCLK, XRD, XWR, VXTALIN, VXTALOUT, XCS and XCSPAR)  and particularly to data signals on the circuit board. This is for minimizing interference between these signals.

VideoOut can be connected to a display via two 22 Ω series resistors and a transient suppressor providing some extra protection or by using an op-amp buffer.
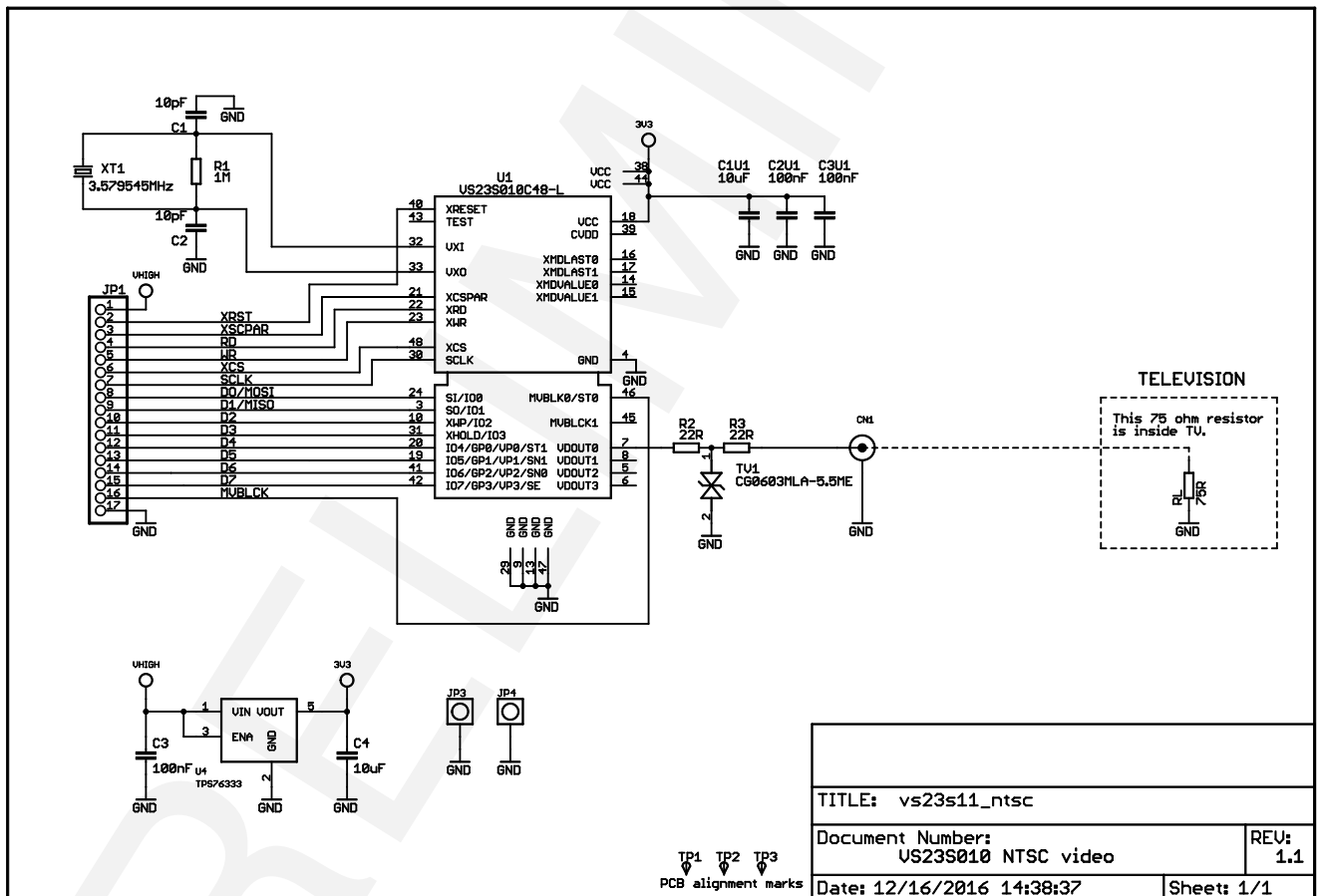
# 6 Device Operation

The device consists of following main blocks: SPI , Video Display Controller, 8-bit Parallel Interface and SRAM. SPI and Video Display Controller can be enabled simultaneously and also 8-bit Parallel Interface and Video Display Controller can be enabled at the same time. However, SPI and 8-bit Parallel Interface have to be used separately because they share I/O. The SRAM can be written and read by all other blocks of VS23S010D-L.
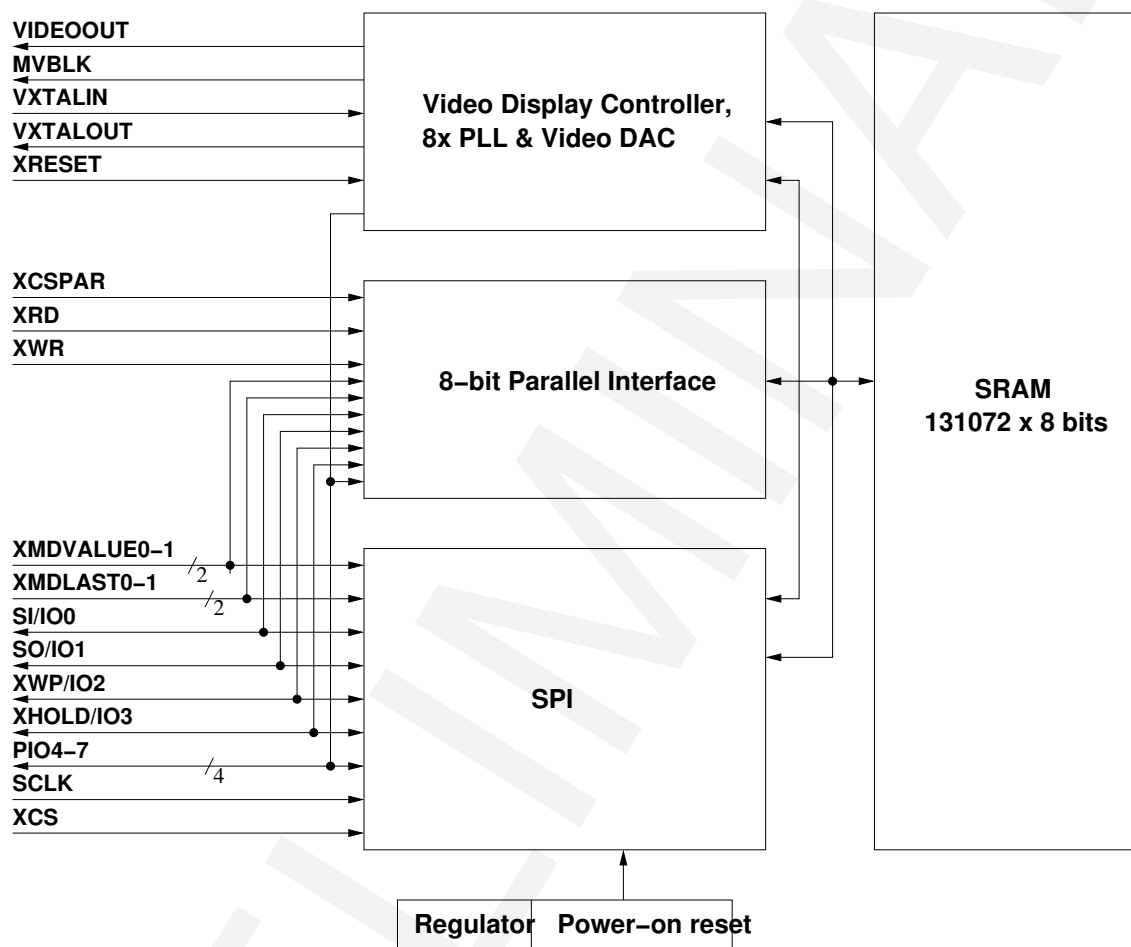


Figure 14: Device Organization

## 6.1 SPI

The VS23S010D-L is controlled by a set instructions that are sent from a host controller, commonly referred as SPI Master. The SPI Master communicates with the VS23S010D-L via the SPI bus which is comprised of four signal groups: Chip Select (XCS), Serial Clock (SCLK), Serial Input (SI, also SO in Dual-I/O mode and XWP and XHOLD in Quad-I/O mode) and Serial Output (SO, also SI in Dual-I/O mode and XWP and XHOLD in Quad-I/O mode).

The VS23S010D-L supports SPI protocol operation mode 0, which is very commonly used. Data is always latched in on the rising edge of the SCLK and always output on the falling edge

of the SCLK. SPI mode 0 is used in Single, Dual-I/O and Quad-I/O modes.
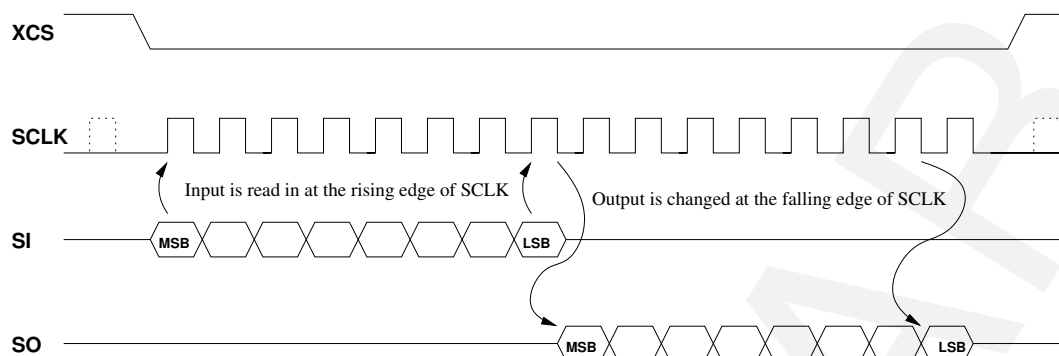


Figure 15: SPI Mode 0

SPI block does not have a separate Reset pin. There is an on-chip power-up delay logic, which is used to reset the selected SPI registers. SPI block logic is clocked by the SCLK pin. Following is a table describing the registers of the VS23S010D-L.

| Register | Symbol | R/W | Default Value | Initialization |
|----------|--------|-----|---------------|----------------|
| **General** | | | | |
| Status | STATUS | RW | 00h | Power-Up |
| Manufacturer and Device ID | ID | R | 2Bh | Power-Up |
| GPIO Control | GPIOCTRL | RW | 00h | Power-Up |
| GPIO State | GPIOSTATE | R | 0Ch | Pull-down and pull-up resistors |
| Multi-IC Access Control | MDACC | RW | 00h | Power-Up |
| **Video Display Controller** | | | | |
| Line Start | PGLPXST | W | 000h | Power-Up |
| Line End | PGLPXEND | W | 000h | Power-Up |
| Line Length | PGLPXLEN | W | 000h | Power-Up |
| Index Start | PGIDXST | W | 0000h | Power-Up |
| Control1 | PGCTRL1 | W | 0000h | Power-Up |
| Control2 | PGCTRL2 | W | 0000h | Power-Up |
| V Table | PGVTBL | W | 0000h | Power-Up |
| U Table | PGUTBL | W | 0000h | Power-Up |
| Program | PGPRGM | W | 0000 0000h | Power-Up |
| Line Value | PGCURRL | R | 0000h | Power-Up |
| Block Move Control1 | PGBMCTRL1 | W | 0 0000 0000h | Power-Up |
| Block Move Control2 | PGBMCTRL2 | W | 0000 0000h | Power-Up |

### 6.1.1   Byte, Page and Sequential Operation Modes

Bits 7 to 6 of the Status register select these three SPI Operation Modes. These modes affect SPI Single, Dual and Quad I/O SRAM operations.

**Byte Operation**   This mode is selected when Mode bits are "00". Read and write operations are limited to one byte in this mode i.e. address does not increment after each written or read byte. After command and 24-bit address byte data is read from or written to given SRAM address every time after subsequent 8 (Single), 4 (Dual-I/O) or 2 (Quad-I/O) SCLK cycles.
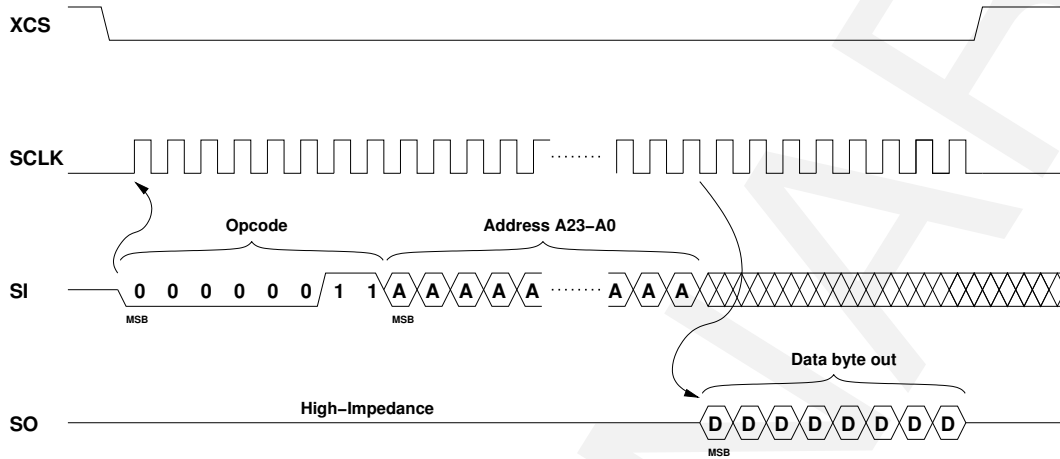


Figure 16: SPI Byte read
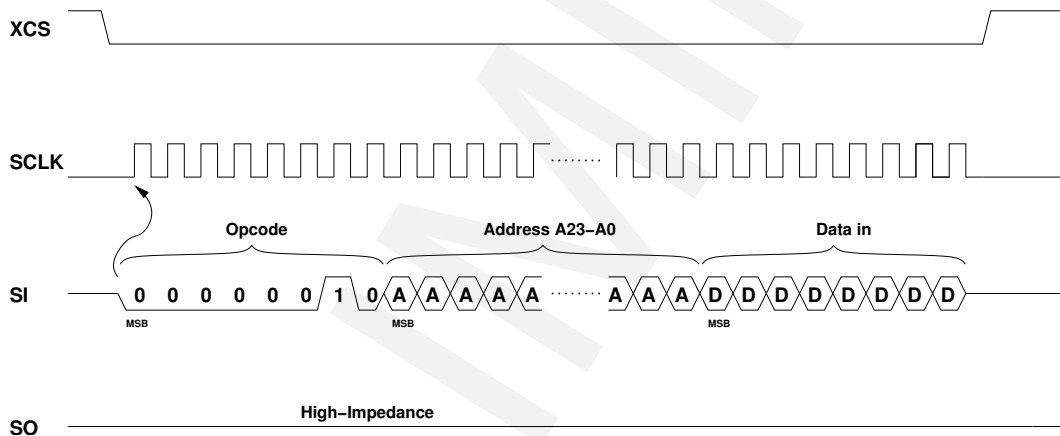


Figure 17: SPI Byte write

**Page Operation**   This mode is selected when Mode bits are "10". VS23S010D-L has 4096 pages of 32 bytes. In page mode reads and writes are limited to the page selected by the given address. After each written or read byte the SRAM address is increased automatically. When the last address of page is reached the accessing will continue from the first address of the page.

**Sequential Operation**   This mode is selected when Mode bits are "01". In this mode the entire SRAM array can be accessed in one operation. The address counter is increased automatically and when the last address 1FFFFh of the SRAM is reached the address counter returns to value 00000h.

If several VS23S010D-Ls are connected to SPI or 8-bit parallel bus in Multi-IC configuration, in the case of address wrapping around the addressing continues from the address 00000h of the
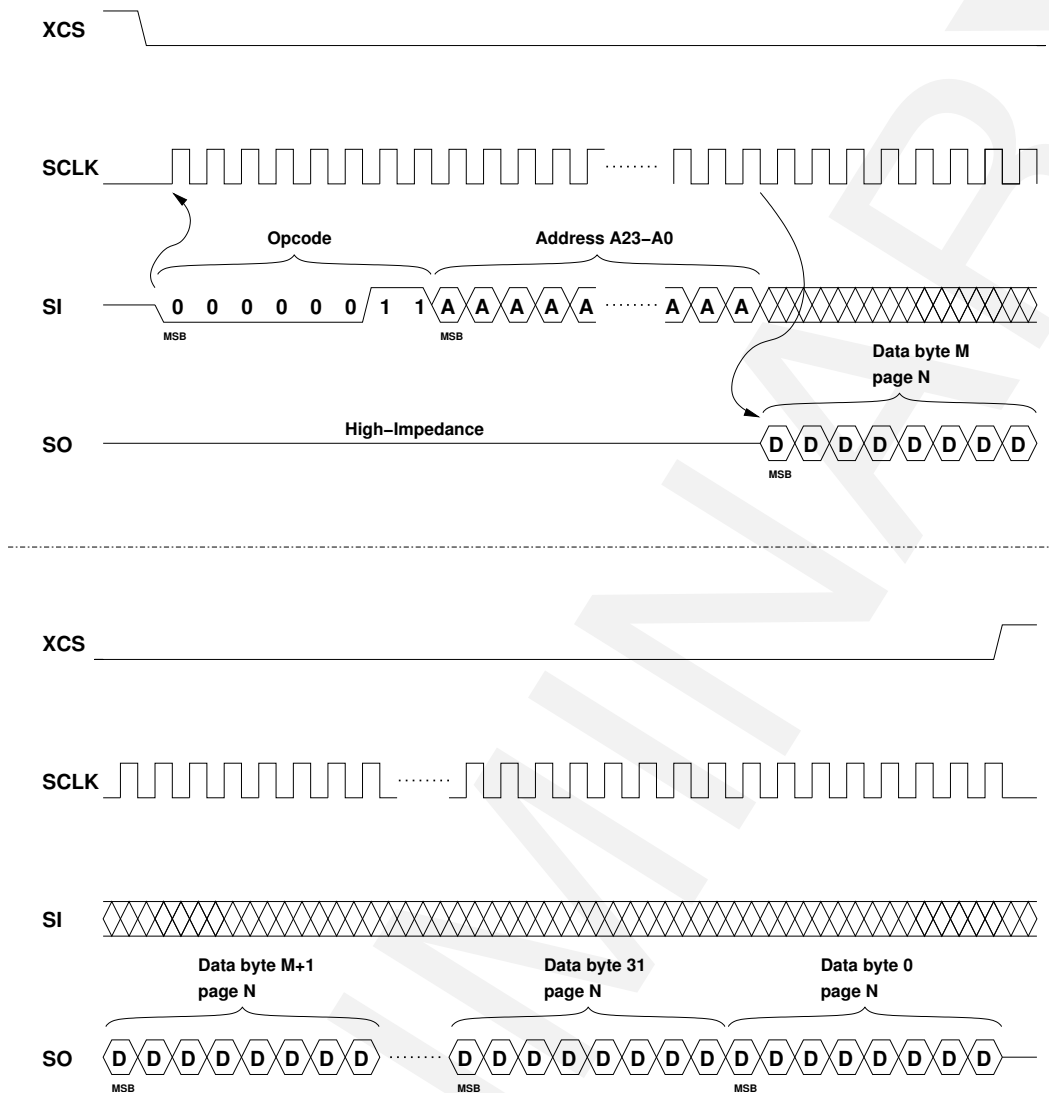
Figure 18: SPI Page read

next VS23S010D-L in system.

### 6.1.2   Dual-I/O and Quad-I/O Operation

In Dual-I/O SPI mode two data bits are read or written during one SCLK cycle. SI/IO0 pin is the lower bit and SO/IO1 pin is the higher bit in Dual-I/O mode. Both pins are inputs during the write and outputs during the read.

In Quad-I/O SPI mode four data bits are read or written during one SCLK cycle. SI/IO0 pin is the lowest bit, SO/IO1 pin is the second bit, XWP/IO2 is the third bit and finally XHOLD/IO3 is the fourth bit in Quad-I/O mode. The pins are inputs during the write and outputs during the read.

In these modes the SPI command is still given in one-bit SPI mode. The address can be given
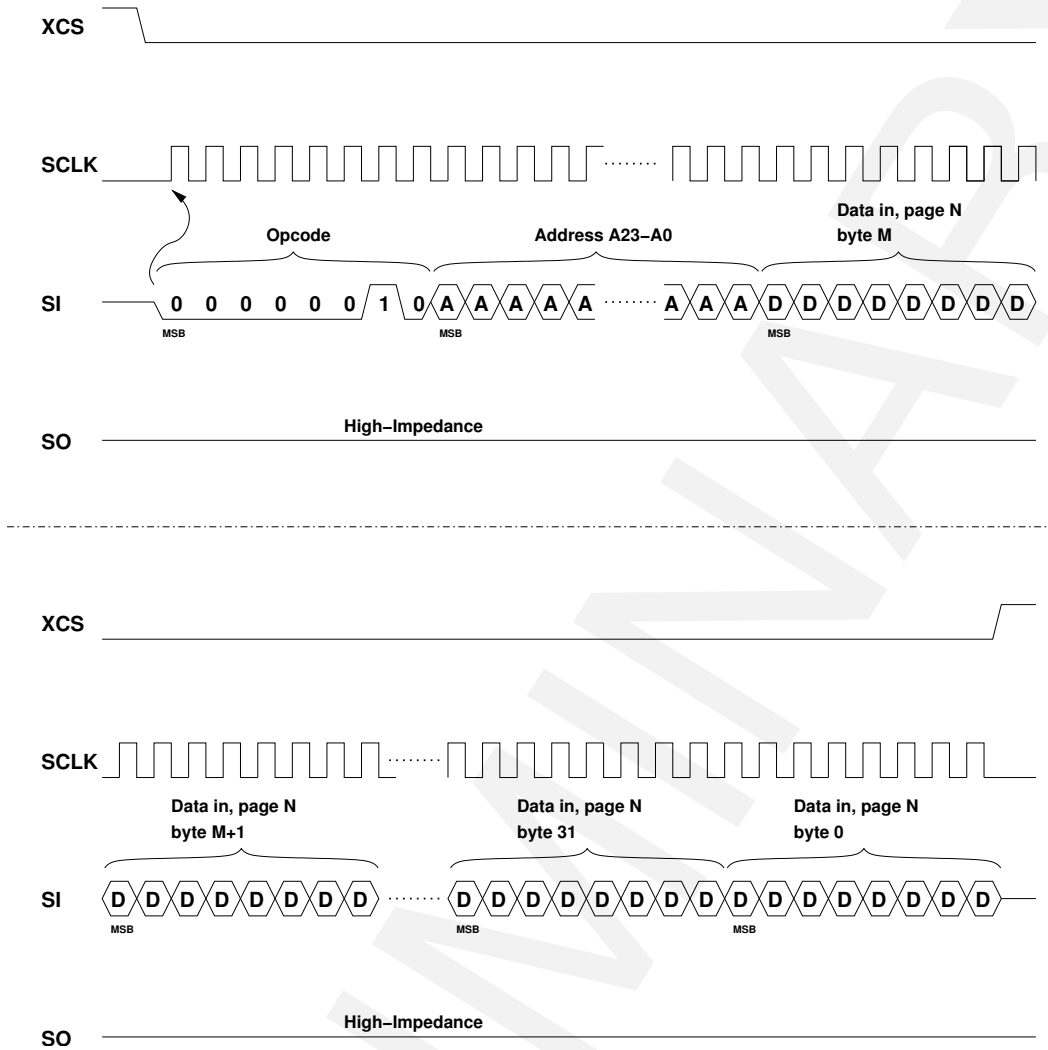
Figure 19: SPI Page write

either in one-bit SPI mode or multi-bit SPI mode depending on the given command.
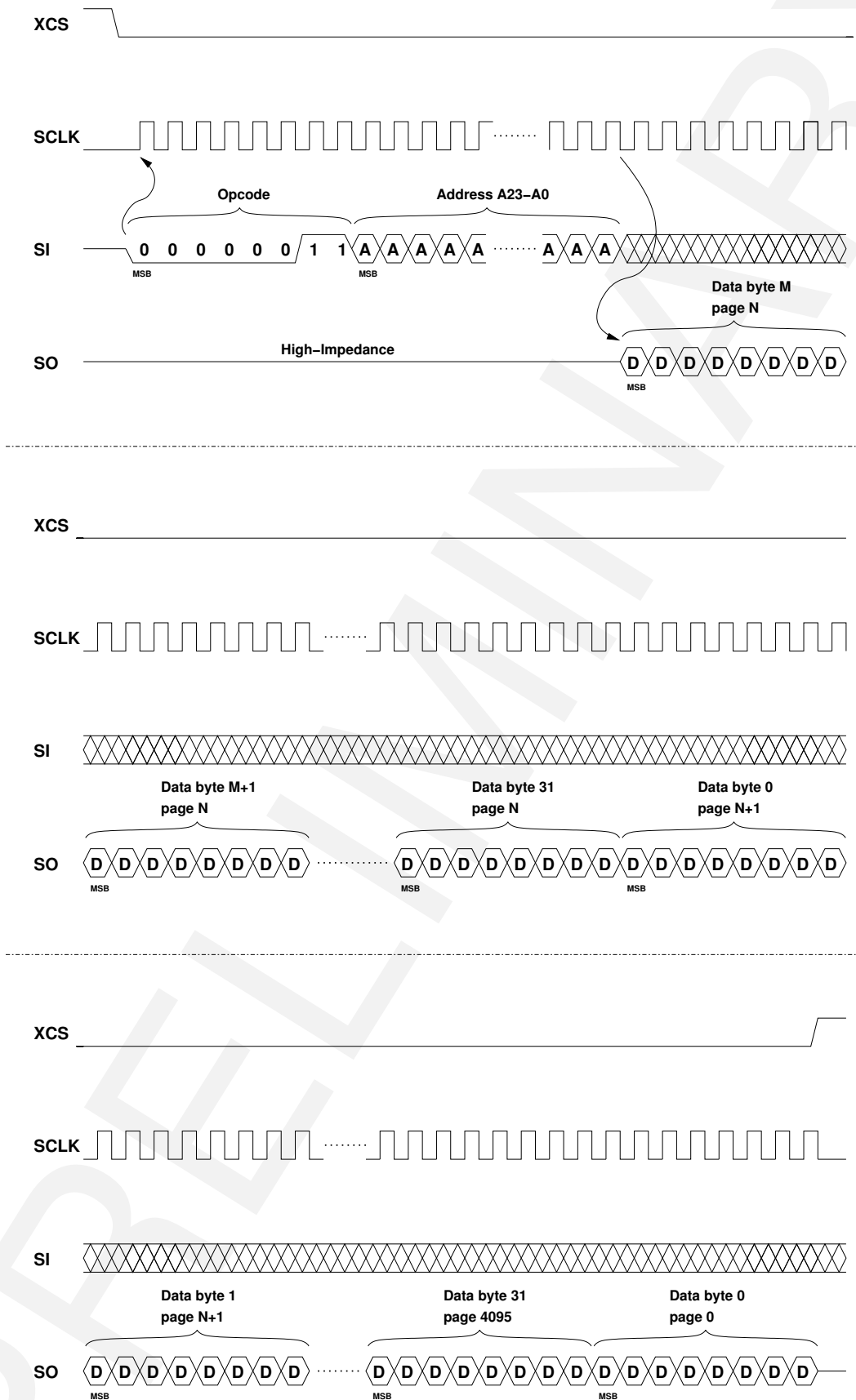
Figure 20: SPI sequential read
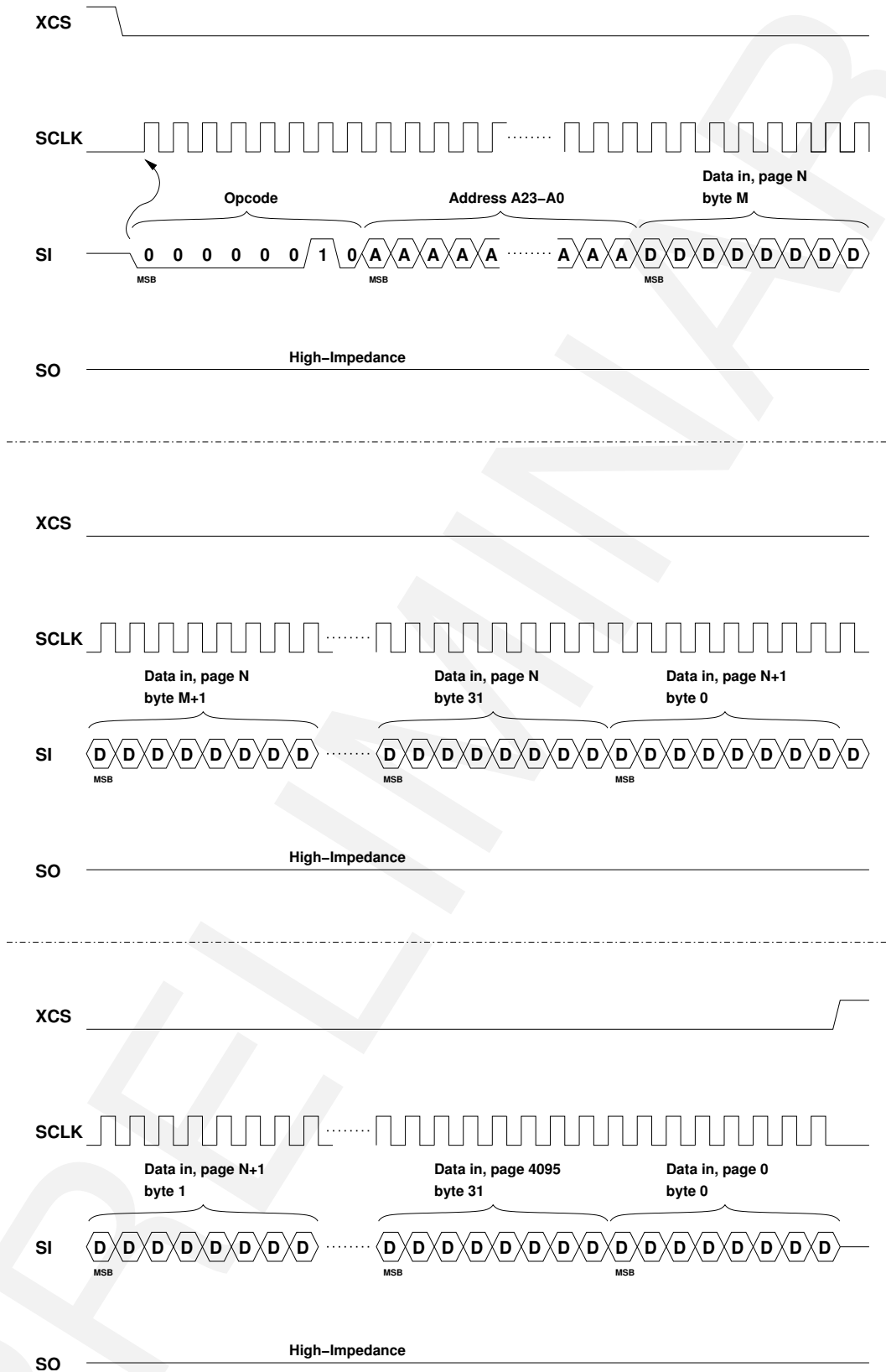
Figure 21: SPI sequential write

### 6.1.3   Write Protect in Single- and Dual-I/O Modes

In single and dual-I/O modes it is possible to suspend writing of some bits during the write operation. This is done by setting XWP pin to low state when SCLK pin is low. When the XWP pin is low SPI data is not taken into VS23S010D-L even though SCLK is toggled. The address counter is incremented during this time when SCLK is toggled like normally in write operation. When the XWP pin is set to high during SCLK low state the write operation continues to an updated SRAM address.In Figure 7 is shown XWP timing.

### 6.1.4   Hold in Single- and Dual-I/O Modes

Hold functionality can be disabled by writing the StSPIH bit of Status register high.  After VS23S010D-L power-up the StSPIH bit is low and Hold function is enabled.

XHOLD pin can be used in single and dual-I/O memory operations. Setting XHOLD low in these modes suspends the operation in progress (SPI read or write). The state of the XHOLD pin can be changed when SCLK is in low state. When XHOLD is low during SPI memory operation the SRAM address counter does not increment even though SCLK is toggled.  In read operation the SO output goes to high-impedance state when XHOLD is low.  This allows SPI bus to be used by some other device during the VS23S010D-L memory operation.  When the XHOLD pin is set to high again the VS23S010D-L memory operation continues. In Figures 5 and 6 are shown hold functionality.

### 6.1.5   Multi-IC Operation

VS23S010D-L has support for multi-die or multi-IC use of SPI and 8-bit parallel interface.  In this mode SRAMs are connected in series after each other to form one large SRAM entity. The Video Display Controller block can only access the its SRAM.

With Multi-IC controls it is possible to connect up to four VS23S010D-Ls acting as one larger VS23S010D-L. XMDLAST0 and XMDLAST1 are active low signals, which are used for informing the number of VS23S010D-L connected to single SPI and/or 8-bit parallel interface bus. XMDVALUE0 and XMDVALUE1 are also active low signals that define the position of each VS23S010D-L in the system.

When one VS23S010D-L is used, the SRAM address is formed using address bits A16-A0. In Multi-IC system additional address bits A18-A17 are used to define, which VS23S010D-L IC is accessed.  Value "00" of A18-A17 selects VS23S010D-L #0 as SRAM access target, "01" selects VS23S010D-L #1, "10" selects VS23S010D-L #2 and finally "11" selects VS23S010D-L #3. The following table summarizes how address bits affect the starting address of SRAM operation in different VS23S010D-L Multi-IC configurations.

| SRAM Operation Start Point | | | | | |
|---|---|---|---|---|---|
| A23-A19 | A18-A17 | A16-A0 | XMDVALUE1-0 | XMDLAST1-0 | # of VS23S010D-Ls |
| Don't care | Don't care | VS23S010D-L #0 | "11" | "11" | 1 |
| | "00" or "10" | VS23S010D-L #0 | "11" | "11" | 2 |
| | "01" or "11" | VS23S010D-L #1 | "10" | | |
| | "00" or "11" | VS23S010D-L #0 | "11" | "01" | 3 |
| | "01" | VS23S010D-L #1 | "10" | | |
| | "10" | VS23S010D-L #2 | "01" | | |
| | "00" | VS23S010D-L #0 | "11" | "00" | 4 |
| | "01" | VS23S010D-L #1 | "10" | | |
| | "10" | VS23S010D-L #2 | "01" | | |
| | "11" | VS23S010D-L #3 | "00" | | |
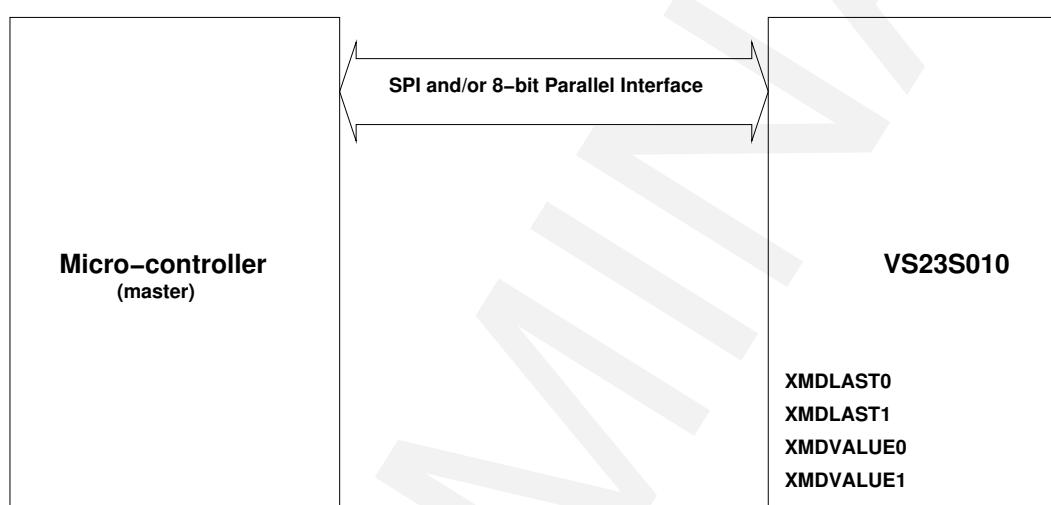


Single VS23S010, XMD* pins have internal pull–up resistors

Figure 22: One VS23S010 operation

It is possible to limit SPI register access to selected VS23S010D-Ls in Multi-IC mode by setting bits in Multi-IC Access Control register. This allows user to write a control command to a selected VS23S010D-L or read a register value from a selected VS23S010D-L. SRAM reads and writes are not affected by this control, because SRAM is handled as one large SRAM entity in Multi-IC mode. Also Multi-IC Access Control writes affect all VS23S010D-Ls in the Multi-IC system.
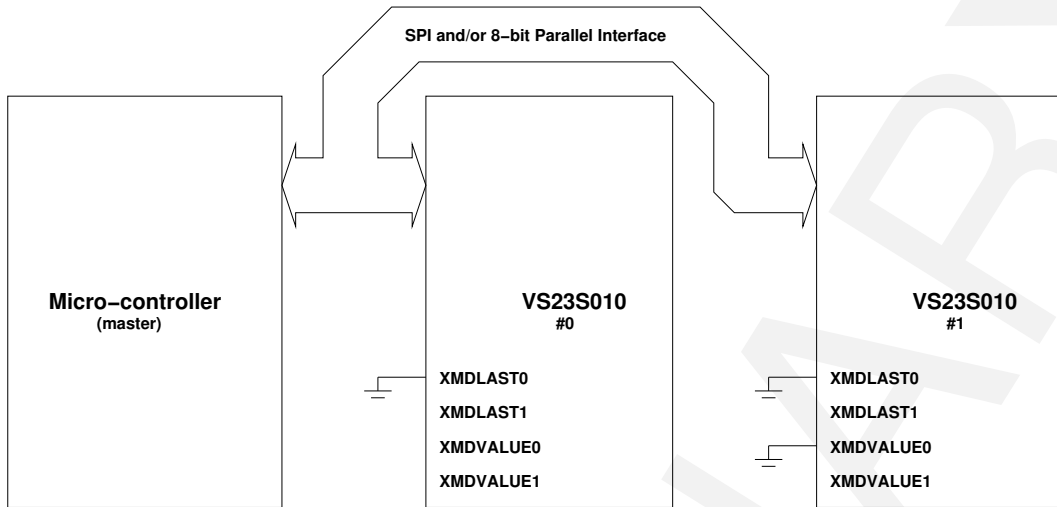
Two VS23S010s, XMD* pins have internal pull–up resistors

Figure 23: Two VS23S010s operation
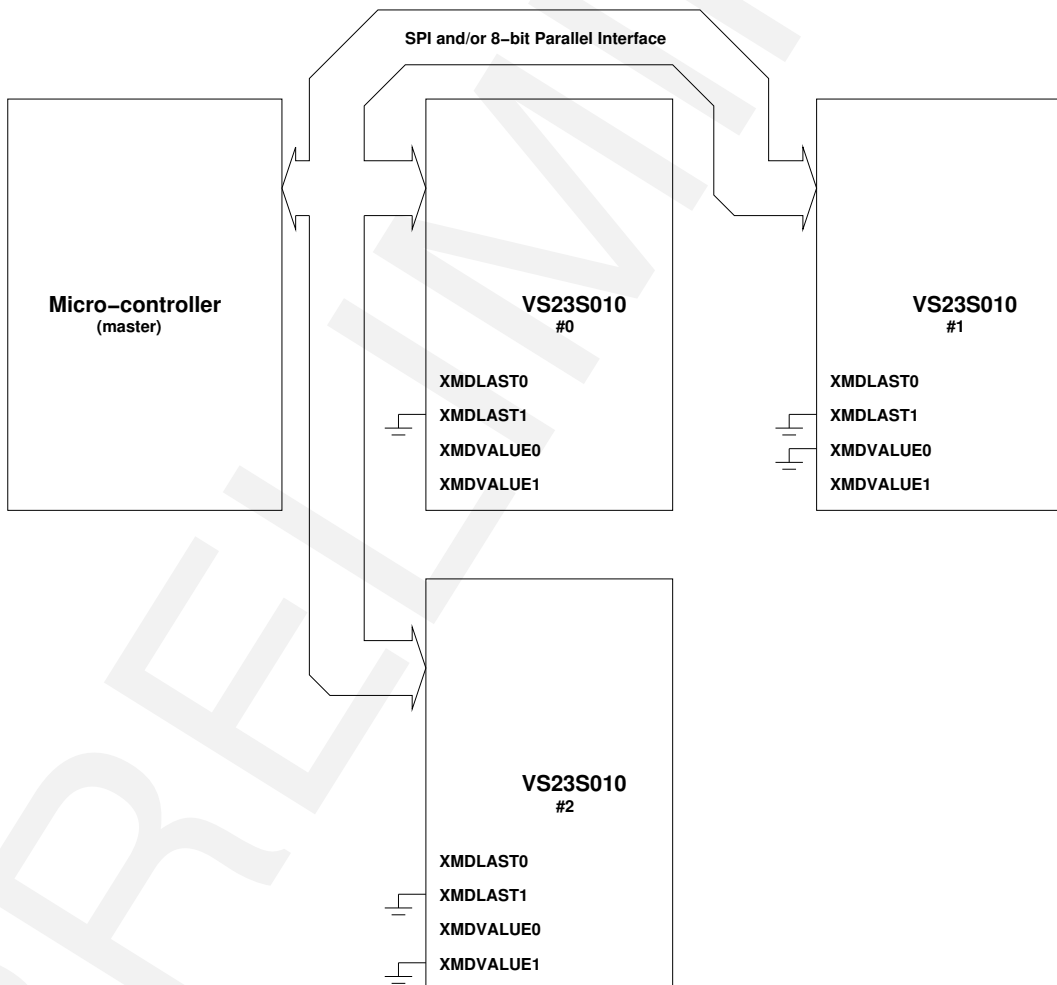


Three VS23S010s, XMD* pins have internal pull–up resistors

Figure 24: Three VS23S010s operation
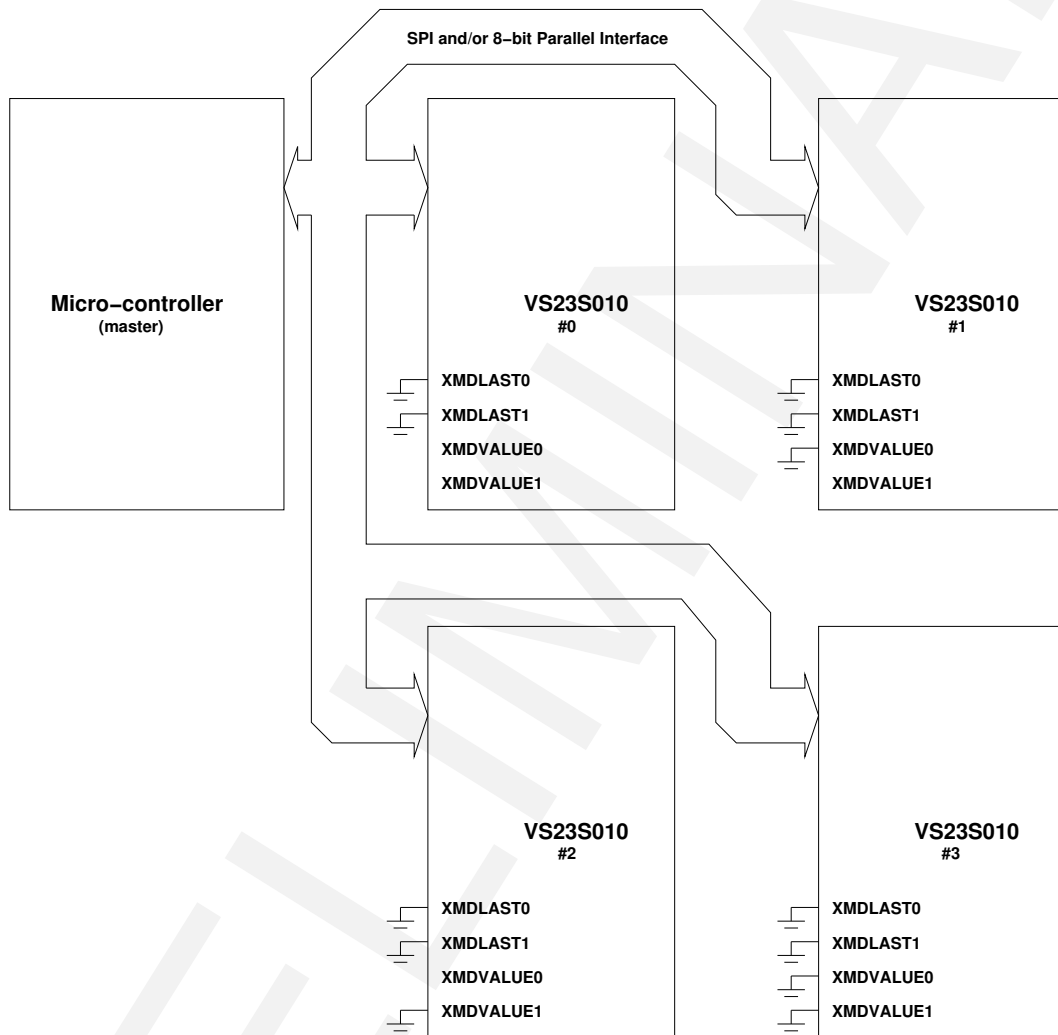
Four VS23S010s, XMD* pins have internal pull–up resistors

Figure 25: Four VS23S010s operation
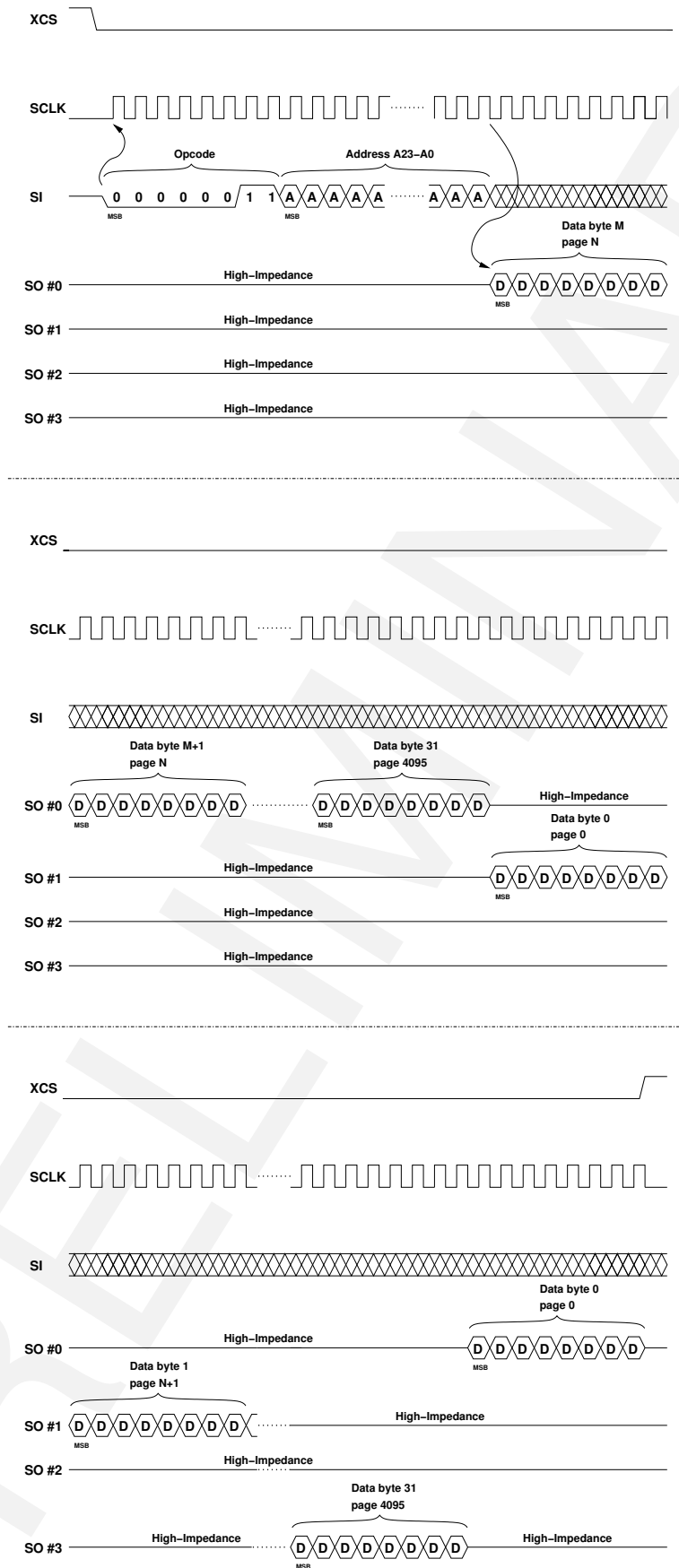
Figure 26: SPI read in Multi-IC system consisting of four VS23S010D-Ls

## 6.2   Video Display Controller

The use of Video Display Controller is described in VS23S010D Guide.

## 6.3 8-Bit Parallel Interface

In parallel mode it is possible to write and read SRAM in the blocks of four bytes. 8-bit parallel interface is an alternative interface to SRAM and during its operation SPI has to be inactive. Clock for the parallel interface is generated on-chip by logical and of XRD and XWR pins. XRD and XWR have equal functionality in generating the parallel interface clock and either XRD or XWR can be used to generate clock for read or write. Data pins in this mode are from LSB: SI/IO0, SO/IO1, XWP/IO2, XHOLD/IO3, PIO4, PIO5, PIO6 and PIO7. They are inputs in instruction, address and write phase and outputs in SRAM data read phase.

Parallel interface timing is similar to SPI: Data is always latched in on the rising edge of the clock and always output on the falling edge of the clock. When pins are switched from input to output, there is a delay of one clock cycle before the outputs are driven by VS23S010D-L.

Additional information considering the usage of interface is given in Chapter 9.
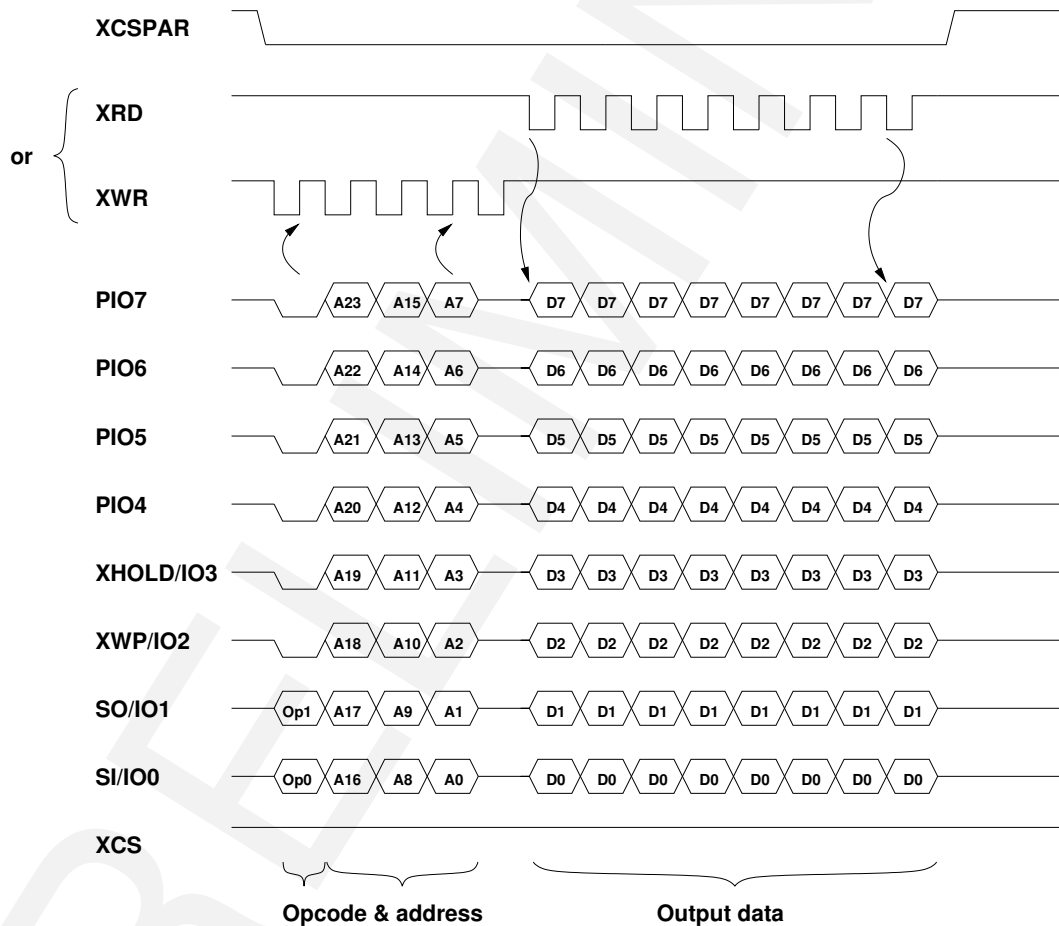


Figure 27: Example of 8-Bit Parallel Interface Signals, more detailed timing shown in Chapter 9.

# 7   SPI Commands and Addressing

A valid SPI instruction or operation is started by first asserting the XCS pin. After that, the host controller clocks out a valid 8-bit opcode on the SPI bus. Following the opcode instruction dependent information (address or data bytes) is sent by the host controller. Address and data are sent MSB first. Operation is ended by deasserting the XCS pin.

**Opcodes which are not supported by the VS23S010D-L are not allowed .** Also if XCS is deasserted when the whole byte is not clocked out the operation of the byte in question will be aborted.

Addressing the SRAM of the VS23S010D-L requires three bytes to be sent, address bits A23-A0. Since the maximum address of one VS23S010D-L is 1FFFFh the address bits A16 to A0 will be used by one device.   Additional address bits A18 and A17 are used in Multi-IC configuration to select one of possibly four devices. Address bits A23 to A19 are ignored by the VS23S010D-L.

| Command | Opcode | | Address Bytes | Data Bytes |
|---------|--------|--|---------------|------------|
| **SRAM Read Commands** | | | | |
| Read | 03h | 0000 0011 | 3 | 1+ |
| Dual-Output Read | 3Bh | 0011 1011 | 3 | 1+ |
| Dual-Output Read, Dual Address | BBh | 1011 1011 | 3 | 1+ |
| Quad-Output Read | 6Bh | 0110 1011 | 3 | 1+ |
| Quad-Output Read, Quad Address | EBh | 1110 1011 | 3 | 1+ |
| **SRAM Write Commands** | | | | |
| Write | 02h | 0000 0010 | 3 | 1+ |
| Dual-Input Write | A2h | 1010 0010 | 3 | 1+ |
| Dual-Input Write, Dual Address | 22h | 0010 0010 | 3 | 1+ |
| Quad-Input Write | 32h | 0011 0010 | 3 | 1+ |
| Quad-Input Write, Quad Address | B2h | 1011 0010 | 3 | 1+ |
| **Miscellaneous Commands** | | | | |
| Read Status Register | 05h | 0000 0101 | 0 | 1+ |
| Write Status Register | 01h | 0000 0001 | 0 | 1+ |
| Read Manufacturer and Device ID | 9Fh | 1001 1111 | 0 | 1+ |
| Read GPIO Control Register | 84h | 1000 0100 | 0 | 1+ |
| Write GPIO Control Register | 82h | 1000 0010 | 0 | 1+ |
| Read GPIO State Register | 86h | 1000 0110 | 0 | 1+ |
| Read Multi-IC Access Control | B7h | 1011 0111 | 0 | 1+ |
| Write Multi-IC Access Control | B8h | 1011 1000 | 0 | 1+ |
| **Video Display Controller Commands** | | | | |
| Write Picture Start value | 28h | 0010 1000 | 0 | 2 |
| Write Picture End value | 29h | 0010 1001 | 0 | 2 |
| Write Line Length | 2Ah | 0010 1010 | 0 | 2 |
| Write Video Display Controller Control1 | 2Bh | 0010 1011 | 0 | 2 |
| Write Picture Index Start address | 2Ch | 0010 1100 | 0 | 2 |
| Write Video Display Controller Control2 | 2Dh | 0010 1101 | 0 | 2 |
| Write V Table | 2Eh | 0010 1110 | 0 | 2 |
| Write U Table | 2Fh | 0010 1111 | 0 | 2 |
| Write Program | 30h | 0011 0000 | 0 | 4 |
| Read Current Line value & PLL lock | 53h | 0101 0011 | 0 | 2 |
| Write Block Move Control1 | 34h | 0011 0100 | 0 | 5 |
| Write Block Move Control2 | 35h | 0011 0101 | 0 | 4 |
| Start Block Move | 36h | 0011 0110 | 0 | 0+ |

## 7.1   SPI Read Commands (03h)

The Read command can be used to sequentially read a continuous stream data from the device by providing clock signal once the initial starting address has been specified. The device has on internal address counter that increments or not on every cycle depending on SPI operating mode.

To perform a read operation, XCS must first be asserted and read opcode must be clocked into

device. After the opcode three address bytes are clocked into the device to specify the starting address location of the first byte to read within SRAM.

After address bytes additional SCLK clock cycles will result in data being output on the SO pin. Data is output MSB first. In sequential mode when the last byte (1FFFFh) of the SRAM has been read, the reading will continue from the beginning of the array (00000h). However, if there are several VS23S010D-Ls in Multi-IC configuration and sequential mode is selected, the reading will continue from the beginning of the array (00000h) of the next VS23S010D-L device. Also, if last VS23S010D-L accesses its last byte (1FFFFh) in Multi-IC mode, the reading will continue from the beginning of the array (00000h) of the first VS23S010D-L device.

Deasserting the XCS pin will terminate the read operation and SO pin goes to high-impedance state.



Figure 28: SPI Read

### 7.1.1   Dual-Output Read (3Bh and BBh)

Dual-Output Read is similar to Read command except that two bits of data are clocked out of the device on every clock cycle.

To perform a Dual-Output Read XCS pin is first asserted. After that opcode 3Bh and three address bytes are sent by the host controller.

After the three address bytes are clocked in, the device will output data on SI/IO0 and SO/IO1 pins. The data is clocked out MSB first and MSB is on pin SO/IO1. During the first clock cycle bit6 will be on SI/IO0 pin, on the next cycle bit5 is on SO/IO1 and bit4 on SI/IO0 and so on. In sequential mode the SRAM addressing will roll over similarly to normal SPI read operation.

Deasserting the XCS pin will terminate the read operation and SI/IO0 and SO/IO1 pins go to high-impedance state.

Dual-Output, Dual Address Read is similar to Dual-Output Read command except that two bits of address are clocked in the device on every clock cycle.
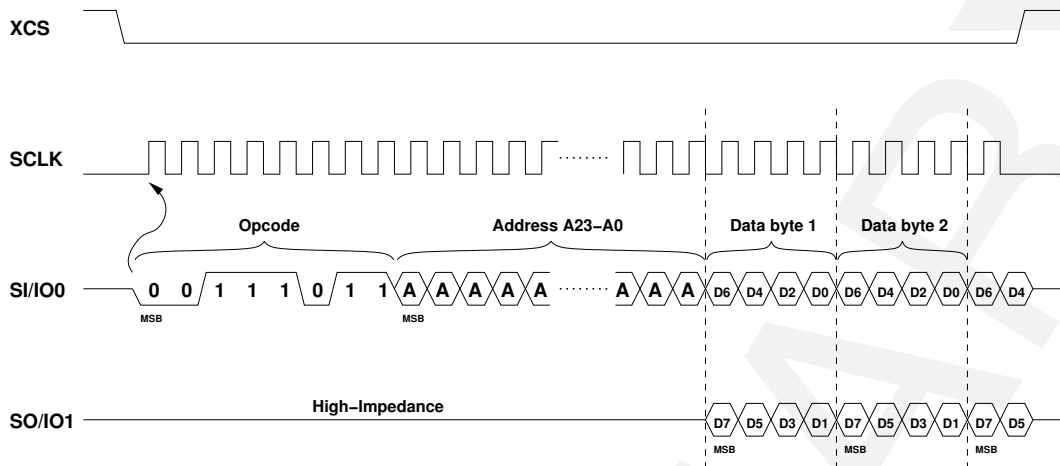
Figure 29: SPI Dual-Output Read

To perform a Dual-Output, Dual Address Read XCS pin is first asserted. After that opcode BBh is sent in one bit mode and three address bytes are sent in dual I/O mode by the host controller to SI/IO0 and SO/IO1 pins.

After the three address bytes are clocked in, there is a dummy byte cycle. After that the device will output data on SI/IO0 and SO/IO1 pins. The rest of the operation is similar to Dual-Output Read.
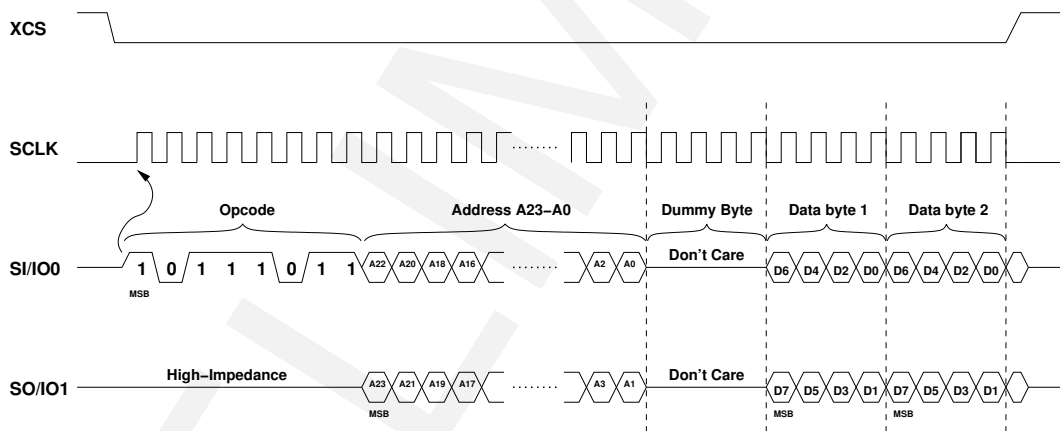


Figure 30: SPI Dual-Output Read, Dual Address

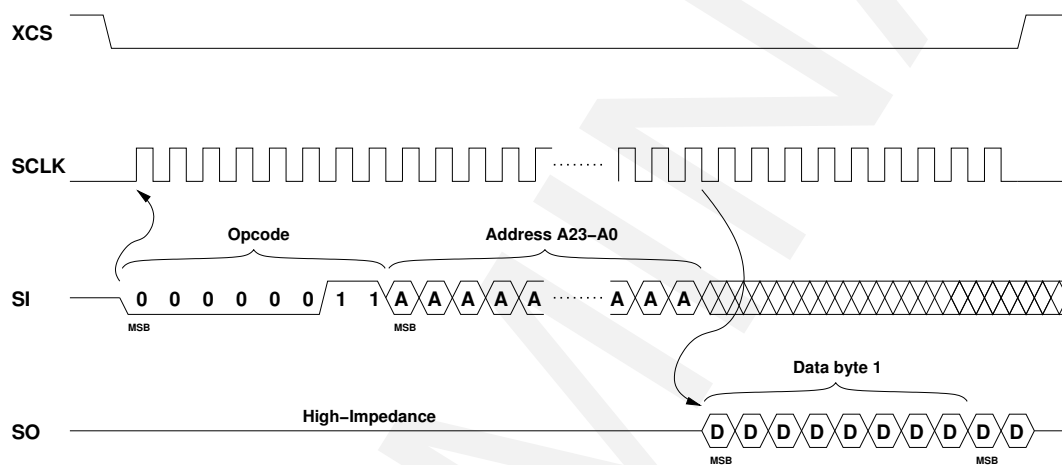### 7.1.2   Quad-Output Read (6Bh and EBh)

Quad-Output Read is similar to Read command except that four bits of data are clocked out of the device on every clock cycle.

To perform a Quad-Output Read XCS pin is first asserted. After that opcode 6Bh and three address bytes are sent by the host controller.

After the three address bytes are clocked in, the device will output data on SI/IO0, SO/IO1,

XWP/IO2 and XHOLD/IO3 pins. The data is clocked out MSB first and MSB is on pin XHOLD/IO3. During the first clock cycle bit6 will be on XWP/IO2 pin, bit5 on pin SO/IO1 and bit4 on SI/IO0, on the next cycle bit3 is on XHOLD/IO3 and bit2 on XWP/IO2 and so on. In sequential mode the SRAM addressing will roll over similarly to normal SPI read operation.

Deasserting the XCS pin will terminate the read operation and SI/IO0, SO/IO1, XWP/IO2 and XHOLD/IO3 pins go to high-impedance state.



Figure 31: SPI Quad-Output Read

Quad-Output, Quad Address Read is similar to Quad-Output Read command except that four bits of address are clocked in the device on every clock cycle.

To perform a Quad-Output, Quad Address Read XCS pin is first asserted. After that opcode EBh is sent in one bit mode and three address bytes are sent in quad I/O mode by the host controller to SI/IO0, SO/IO1, XWP/IO2 and XHOLD/IO3 pins.

After the three address bytes are clocked in, there is a dummy byte cycle. After that the device will output data on SI/IO0, SO/IO1, XWP/IO2 and XHOLD/IO3 pins. The rest of the operation is similar to Quad-Output Read.

## 7.2  SPI Write Commands (02h)

Prior to writing the device must be selected by bringing XCS pin low. Once the device is selected the Write command can be started by issuing a Write instruction (opcode 02h) followed by a 23-bit address. If the device works in sequential mode (set by Status Register write) then after the initial data byte additional bytes can be clocked into device. The internal address

Figure 32: SPI Quad-Output Read, Quad Address

pointer is automatically incremented when needed depending on operating mode. In sequential mode when the internal address pointer reaches its maximum value (1FFFFh) it rolls over to 00000h. If VS23S010D-L is part of the Multi-IC setup, then in sequential mode the writing will continue from the beginning (00000h) of the next VS23S010D-L SRAM. Also in sequential mode after the last byte (1FFFFh) of the last VS23S010D-L is written, the writing continues from the beginning (00000h) of the first VS23S010D-L SRAM. This allows the operation to continue indefinitely, however, previous data will be overwritten.
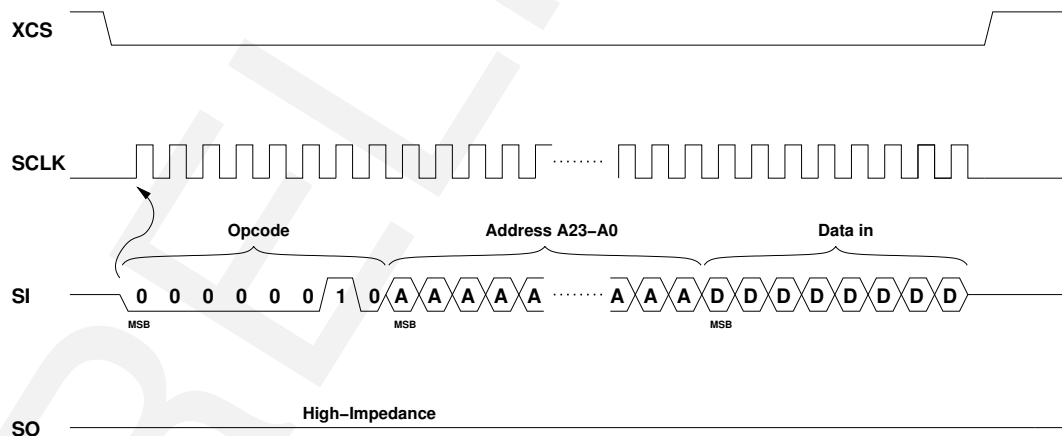


Figure 33: SPI Write

### 7.2.1   Dual-Input Write (A2h and 22h)

Dual-Input Write command is similar to Write command except that two bits of data are clocked in the device on every clock cycle and opcode is A2h.
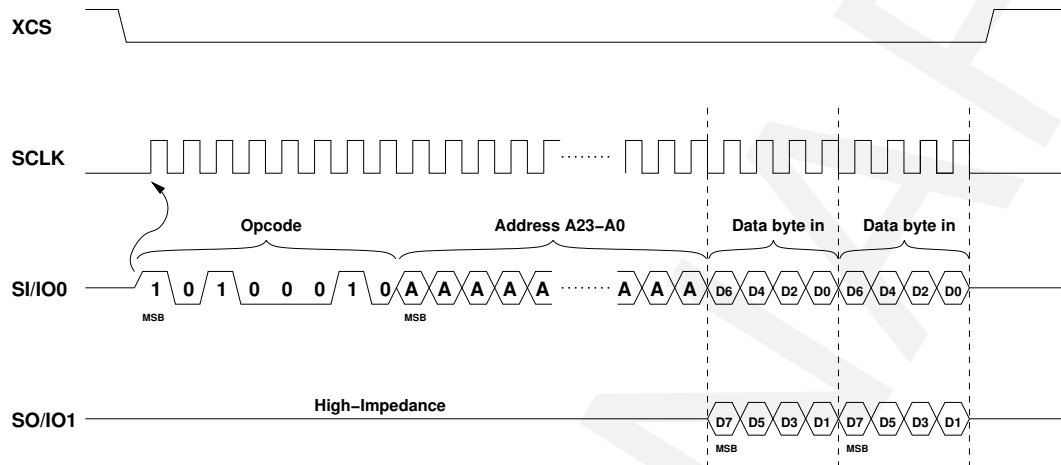


Figure 34: SPI Dual-Input Write

Dual-Input, Dual Address Write command is similar to Dual-Input Write command except that two bits of address are clocked in the device on every clock cycle and opcode is 22h.
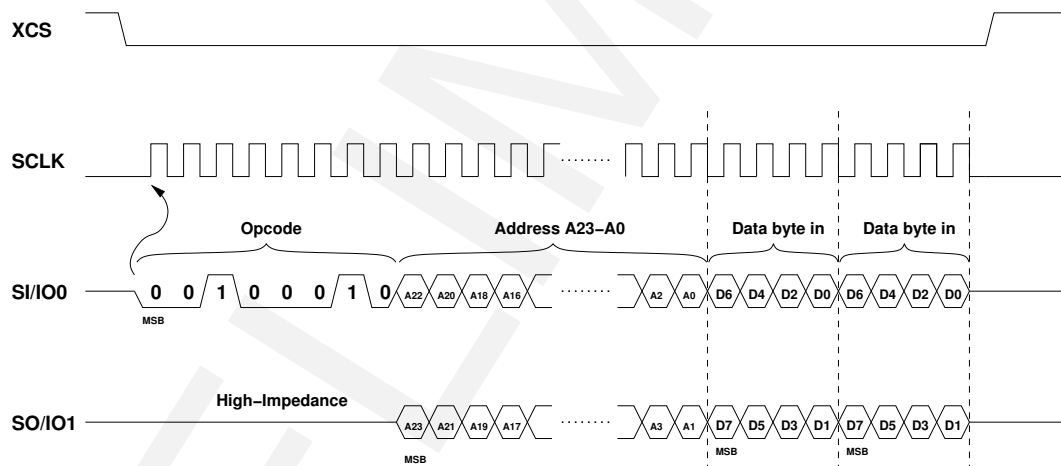


Figure 35: SPI Dual-Input, Dual Address Write

### 7.2.2   Quad-Input Write (32h and B2h)

Quad-Input Write command is similar to Write command except that four bits of data are clocked in the device on every clock cycle and opcode is 32h.

Quad-Input, Quad Address Write command is similar to Quad-Input Write command except that four bits of address are clocked in the device on every clock cycle and opcode is B2h.
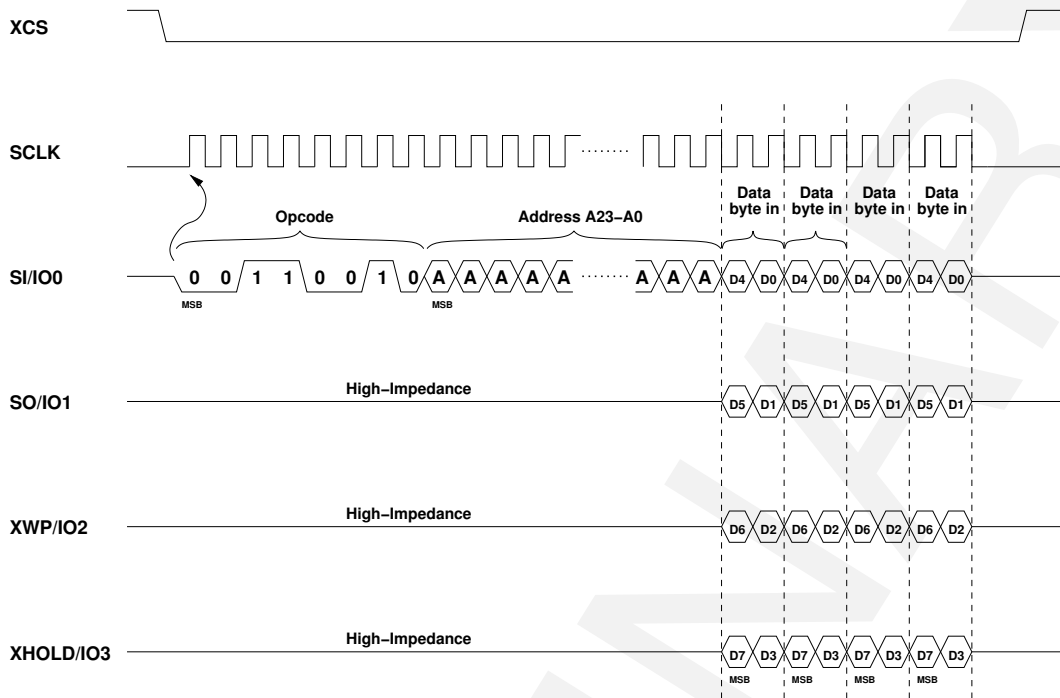
Figure 36: SPI Quad-Input Write
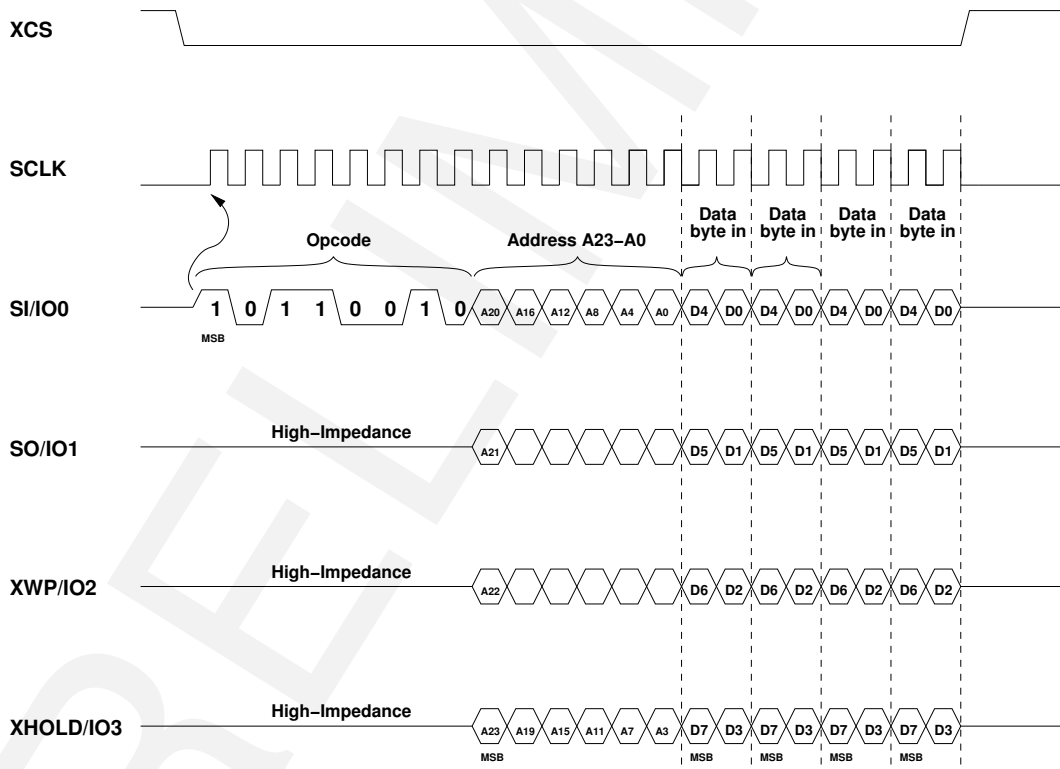


Figure 37: SPI Quad-Input, Quad Address Write

## 7.3   SPI Miscellaneous Commands

### 7.3.1   Read Status Register (05h)

The Read Status command is started by asserting XCS pin. After that the host controller sends the opcode, 05h. The device responds by clocking out a byte wide value of Status register. When XCS pin is deasserted, the clocking out of the register is ended and SO pin goes to high-impedance state.

| Output Bits | Name | | Type | | Description |
|---|---|---|---|---|---|
| 7-6 | StSPIMn | SPI Mode | RW | 0 0 | Byte Mode (Default) |
| | | | | 0 1 | Sequential Mode |
| | | | | 1 0 | Page Mode |
| | | | | 1 1 | Reserved |
| 5 | Reserved | Reserved | RW | 0 | Default |
| 4 | StFastWV | SPI Fast Write in Video Mode | RW | 0 | Normal write (Default) |
| | | | RW | 1 | Fast write |
| 3-1 | StUsern | User Bits | RW | | User Bits |
| 0 | StSPIH | SPI Hold Function | RW | 0 | Hold (Default) |
| | | | | 1 | No Hold |

**StSPIMn**   These bits indicate the operating mode of the SPI of the VS23S010D-L. StSPIMn bits affect the operation in all SPI SRAM read and write modes.

**Reserved**   This bit is reserved. It has to be low always for correct functionality of the VS23S010D-L.

**StFastWV**   StFastWV bit enables fast write mode when video generation is enabled. In fast write mode it is possible to write up to six times the amount of data compared to normal mode.

There are two limitations. The modulo-4 of the start address has to be zero. Otherwise the SRAM data below start address to address, which is equally divisible by four is set to 00h.

Also the modulo-4 of last address has to equal three in fast write mode. If modulo-4 of the last address is something else, then the last 1 to 3 bytes are not written to SRAM. Fast write mode is only for SPI write operations when Video Display Controller is enabled.

**StUsern**   StUsern bits are user assignable and have no effect to operation on VS23S010D-L. Default value is low.

**StSPIH**   StSPIH enables Hold functionality in Single and Dual mode SPI operations. Default value is "0" which means that Hold functionality is enabled.
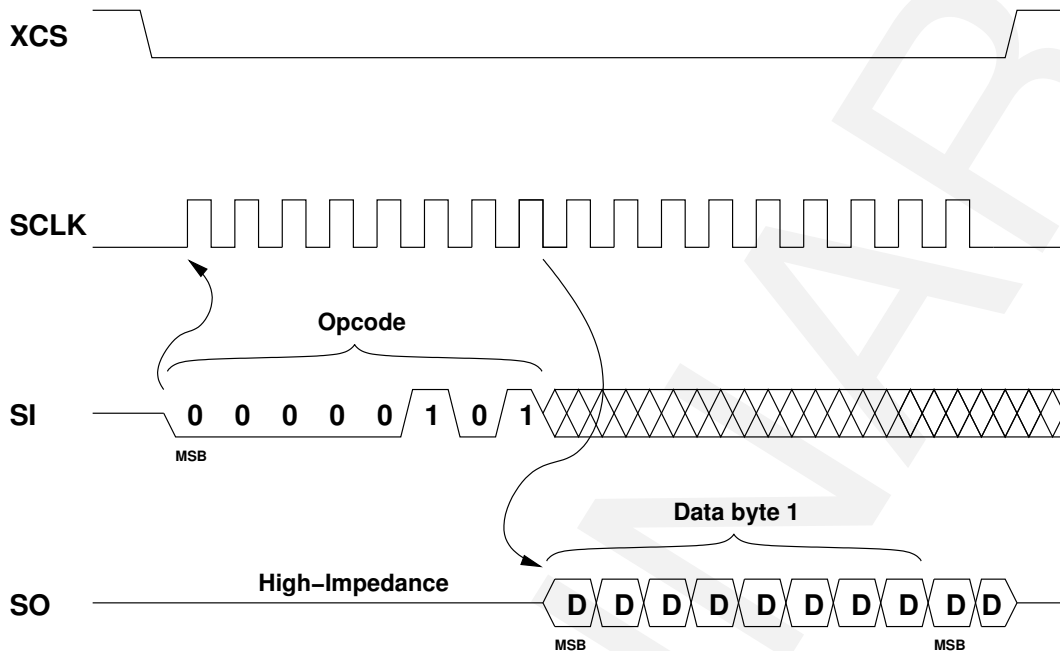


Figure 38: SPI Read Status Register

### 7.3.2   Write Status Register (01h)

To write the GPIO Control register XCS pin must be first asserted and opcode 01h clocked into the device. After that byte-wide value is clocked in the device via SI pin. The value is input MSB (bit 7) first. The state of the Status Register bits is changed according to the received byte after the SCLK goes low. Note, that bit 5 has to be low always.

| Write Status Register Format | | | | | | | |
|---|---|---|---|---|---|---|---|
| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| StSPIM1 | StSPIM0 | Reserved, "0" | StFastWV | StUser2 | StUser1 | StUser0 | StSPIH |

### 7.3.3   Read Manufacturer and Device ID (9Fh)

The Read Manufacturer and Device ID command is started by asserting XCS pin. After that the host controller sends the opcode, 9Fh. The device responds by clocking out a byte wide constant, value 2Bh. The two lowest bits of the second byte inform the amount of VS23S010D-Ls and also the amount of SRAM in the current configuration. When XCS pin is deasserted, the clocking out of the data is ended and SO pin goes to high-impedance state.

Note, Manufacturer and Device ID is read-only register.
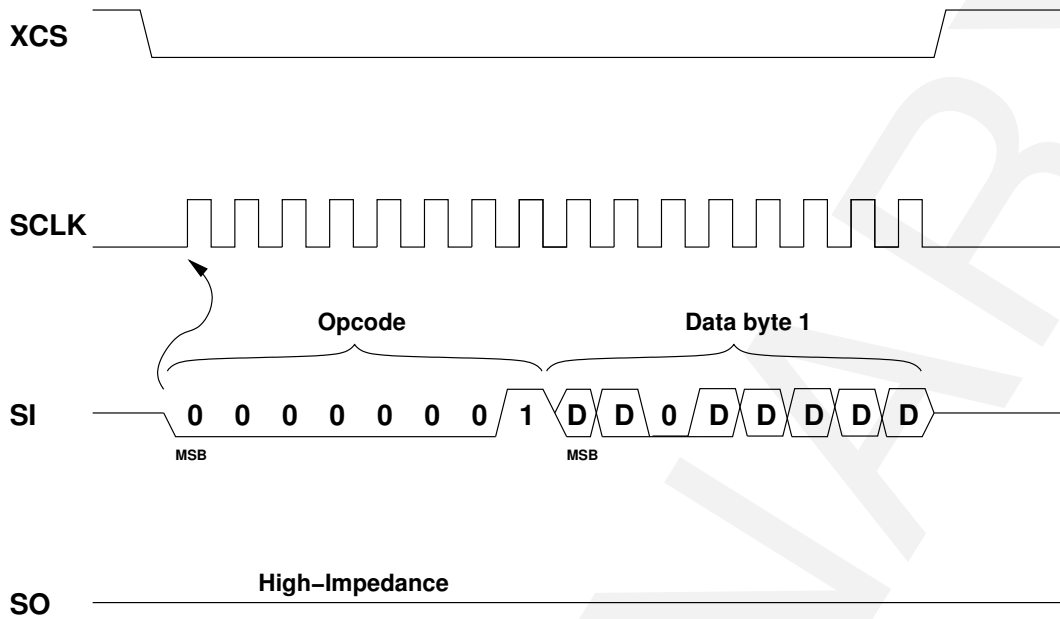
Figure 39: SPI Write Status Register

| Bits | | Name | Type | | Description |
|------|------|------------------------------|------|-----|-----------------------------------|
| 15-8 | ID | Manufacturer and Device ID | R | 2Bh | ID (default) |
| 7-2 | | Don't care | R | 0 | default |
| 1-0 | Conf | Device configuration | R | 00 | One VS23S010D-L, 1 Mbit SRAM |
| | | | | 01 | Two VS23S010D-Ls, 2 Mbit SRAM |
| | | | | 10 | Three VS23S010D-Ls, 3 Mbit SRAM |
| | | | | 11 | Four VS23S010D-Ls, 4 Mbit SRAM |
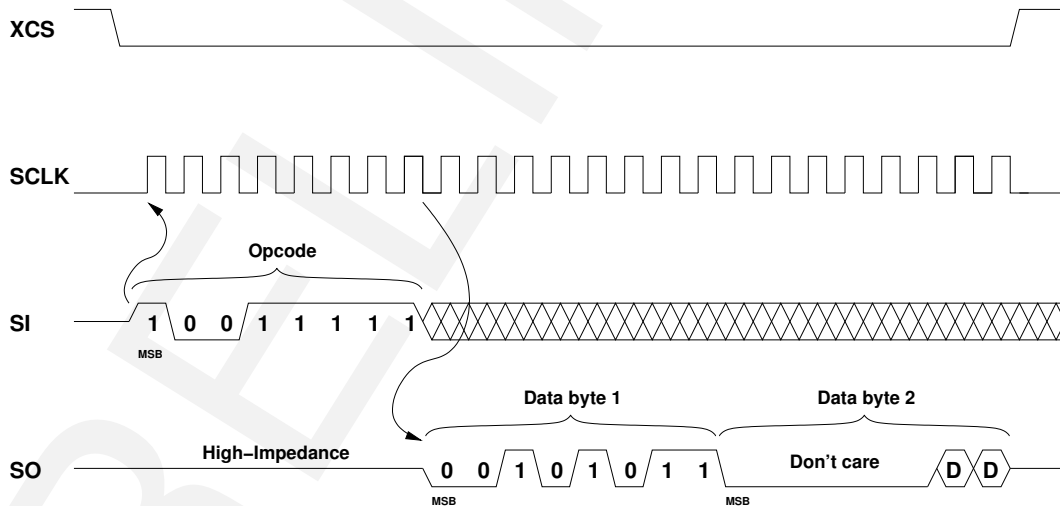


Figure 40: SPI Read Manufacturer and Device ID

### 7.3.4   Read GPIO Control Register (84h)

The Read GPIO Control Register command is started by asserting XCS pin. After that the host controller sends the opcode, 84h. The device responds by clocking out a byte wide value. When XCS pin is deasserted, the clocking out of the register value is ended and SO pin goes to high-impedance state.



Figure 41: SPI Read GPIO Control

| Bits | | Name | Type | | Description |
|------|------|------|------|---|-------------|
| 7-4 | PIOnD | PIO7-4 Direction | RW | 0 | Input (default) |
| | | | | 1 | Output |
| 3-0 | PIOnO | PIO7-4 Output State | RW | 0 | Low (default) |
| | | | | 1 | High |

**PIOnD**   PIOnD bits set the direction of PIO7-4 pins, when 8-bit parallel interface is not used. Default value "0" sets a PIO as input. Bit 7 sets PIO7 direction, bit 6 PIO6 direction and so on.

High value "1" sets the PIO as output with a value set in PIOnO bits.

**PIOnO**   PIOnO bits set the PIO7-4 output state. Default is "0", which sets the state low. Bit 3 sets PIO7 output state, bit 3 PIO6 output state etc.

High value "1" sets the corresponding PIO state to high.

Note, that 8-bit parallel interface overrides GPIO functionality of PIO7-4.

### 7.3.5   Write GPIO Control Register (82h)

To write the GPIO Control register XCS pin must be first asserted and opcode 82h clocked into the device. After that byte-wide value is clocked in the device via SI pin. The value is input MSB (bit 7) first. The state of the PIO7-4 pins is changed according to the received byte after the SCLK goes low.

| Write GPIO Control Register Format | | | | | | | |
|---|---|---|---|---|---|---|---|
| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| PIO7D | PIO6D | PIO5D | PIO4D | PIO7O | PIO6O | PIO5O | PIO4O |
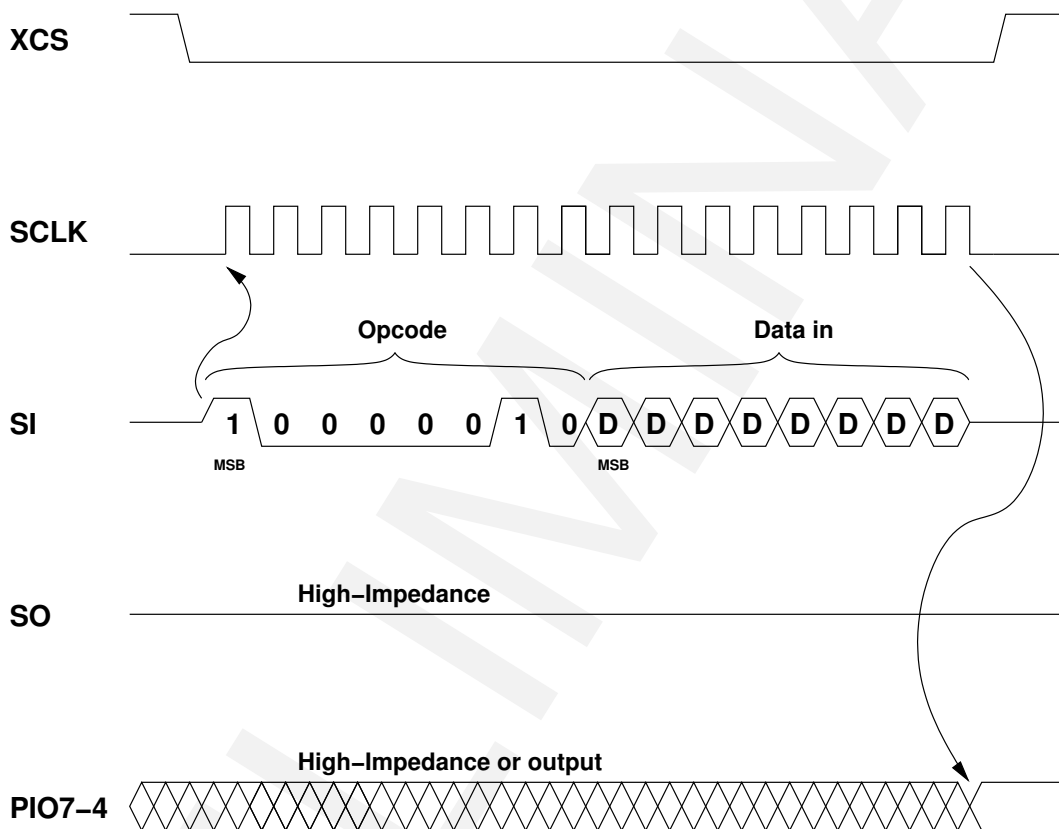


Figure 42: SPI Write GPIO Control

### 7.3.6   Read GPIO State Register (86h)

The Read GPIO State Register command is started by asserting XCS pin. After that the host controller sends the opcode, 86h. The device responds by clocking out a byte wide value. When XCS pin is deasserted, the clocking out of the register value is ended and SO pin goes to high-impedance state.
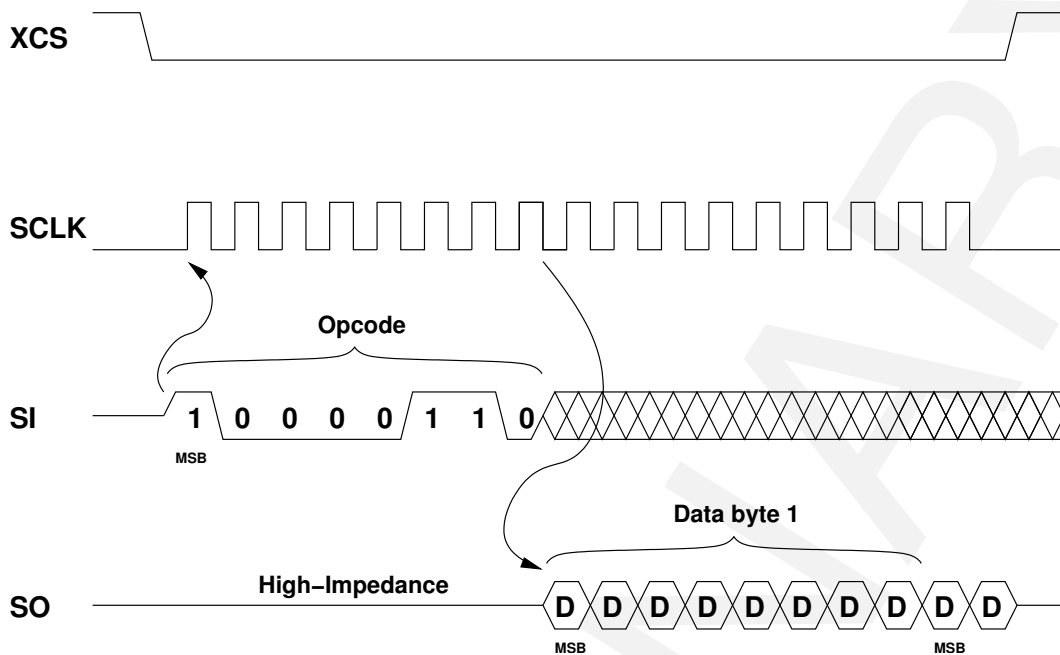
Figure 43: SPI Read GPIO State

| Output Bit | GPIO State Description |
|------------|------------------------|
| 7 | PIO7 logic state |
| 6 | PIO6 logic state |
| 5 | PIO5 logic state |
| 4 | PIO4 logic state |
| 3 | XHOLD logic state |
| 2 | XWP logic state |
| 1 | PLL lock |
| 0 | Video Generator block move active |

### 7.3.7  Read Multi-IC Control Register (B7h)

The read Multi-IC Control Register command is started by asserting XCS pin. After that the host controller sends the opcode, B7h. The device responds by clocking out a byte wide value. When XCS pin is deasserted, the clocking out of the register value is ended and SO pin goes to high-impedance state.
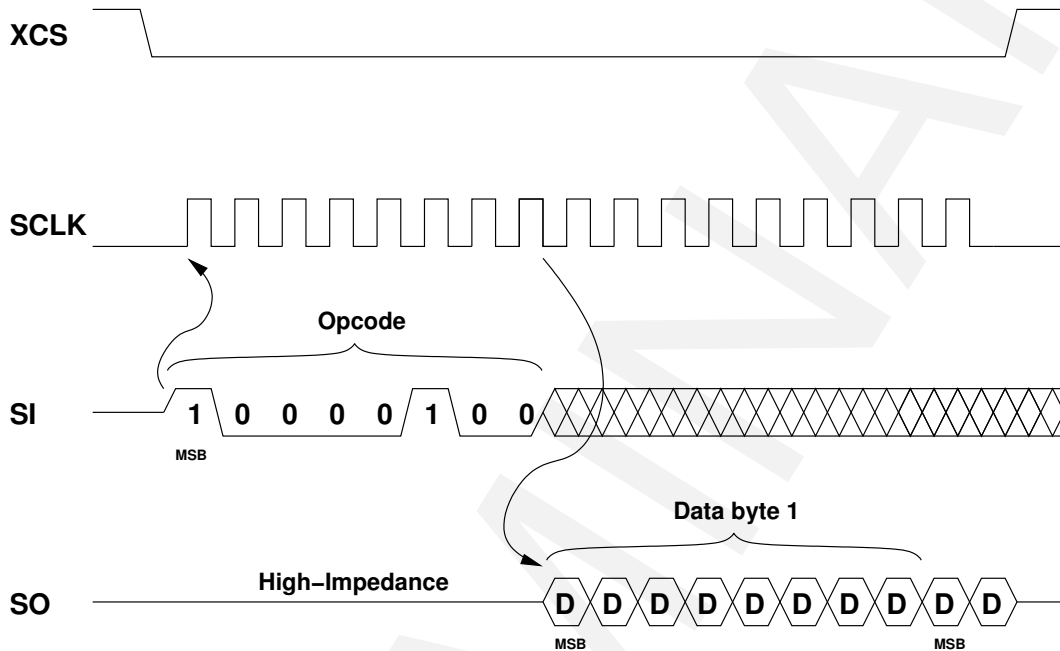
| Bits | | Name | Type | | Description |
|------|------|------|------|------|------|
| 7-6 | MDelay2 | SRAM2 delay | RW | 00 | Longest SRAM2 read delay (default) |
| | | | | 01 | 2nd longest SRAM2 read delay |
| | | | | 10 | 3rd longest SRAM2 read delay |
| | | | | 11 | Shortest SRAM2 read delay |
| 5-4 | MDelay1 | SRAM1 delay | RW | 00 | Longest SRAM1 read delay (default) |
| | | | | 01 | 2nd longest SRAM1 read delay |
| | | | | 10 | 3rd longest SRAM1 read delay |
| | | | | 11 | Shortest SRAM1 read delay |
| 3-0 | DisROpsn | Disable SPI register operations | RW | 0000 | Enabled (default) |
| | | | | 0001 | Disabled for IC#0 |
| | | | | 0010 | Disabled for IC#1 |
| | | | | 0100 | Disabled for IC#2 |
| | | | | ... | |
| | | | | 1111 | Disabled for ICs #0, #1, #2 and #3 |

**MDelay2**   MDelay2 bits set the read delay of SRAM2. "00" value is slowest and it is recommended.

**MDelay1**   MDelay1 bits set the read delay of SRAM1. "00" value is slowest and it is recommended.

**DisROpsn**   In Multi-IC setup DisROpsn bits are used to control the SPI writes to and reads from VS23S010D-L registers. SRAM operations and Multi-IC Control register accesses are not affected by this control. DisROps3 controls #3 VS23S010D-L device, DisROps2 controls the #2 VS23S010D-L and so on.

The low bit value "0" enables SPI writes to and reads from registers of particular device. The high bit value "1" disables the operations.

### 7.3.8   Write Multi-IC Control Register (B8h)

To write the Multi-IC Control register XCS pin must be first asserted and opcode B8h clocked into the device. After that byte-wide value is clocked in the device via SI pin. The value is input MSB (bit 7) first. The state of the Multi-IC register bits is changed according to the received byte after the SCLK goes low.

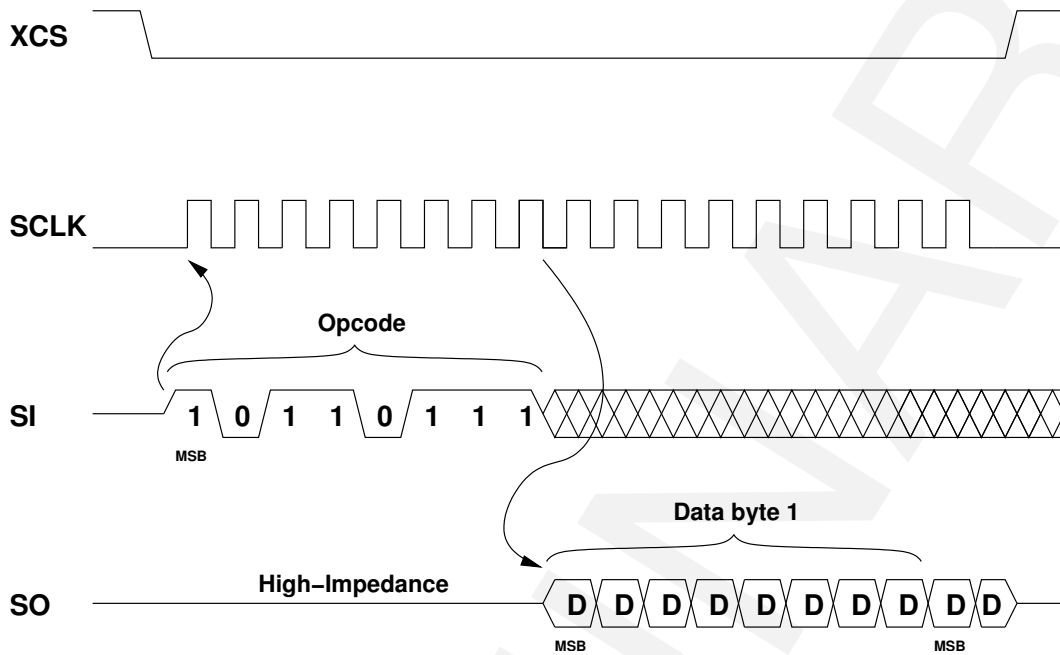| Write Multi-IC Control Register Format | | | | | | | |
|------|------|------|------|------|------|------|------|
| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| MDelay2 | | MDelay1 | | DisROps3 | DisROps2 | DisROps1 | DisROps0 |

Figure 44: SPI Read Multi-IC Control
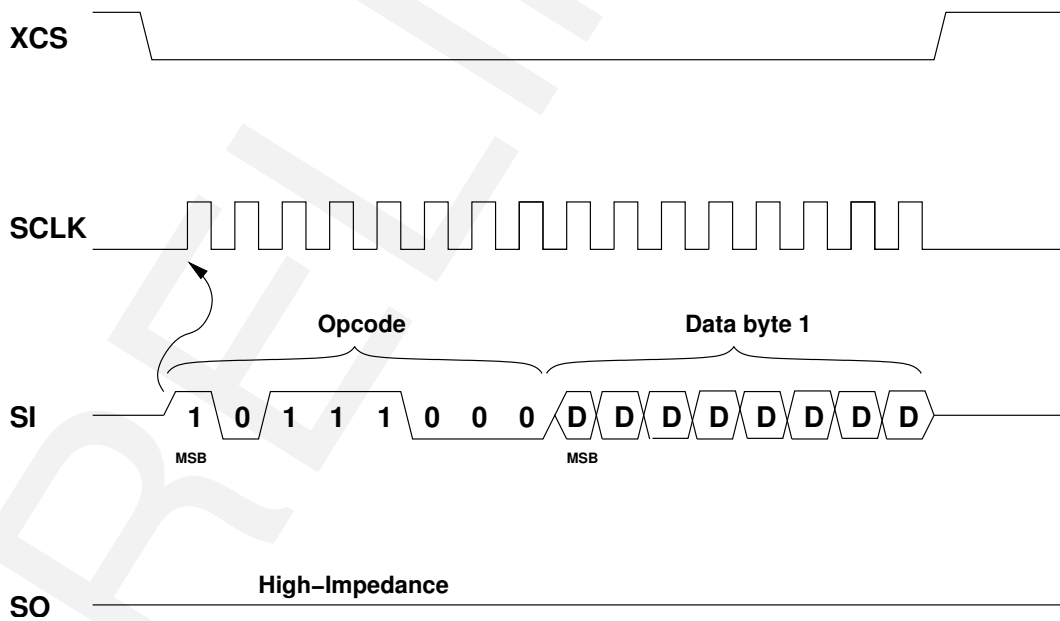


Figure 45: SPI Write Multi-IC Control

# 8   Video Display Controller Commands

## 8.1   Write Picture Start (28h)

Picture Start value defines the pixel position where the normal line starts. The position is defined by CSClk cycles (i.e. color subcarrier cycles) from the start of the line. The fixed 1.25 CSClk (10 VClk) cycles long sync level at the beginning of each line is additional to given Picture Start value. Note, that Picture Start value has to be less than Line Length divided by 8. The recommended minimum value of Picture Start is 7.

To write the Picture Start register XCS pin must be first asserted and opcode 28h clocked into the device. After that two byte value is clocked in the device via SI pin. The two byte value is input MSB (bit 15) first. The register value is 12 bits (11:0) wide, so bits 15 to 12 are don't cares. When XCS pin is deasserted the Picture Start register will be updated.
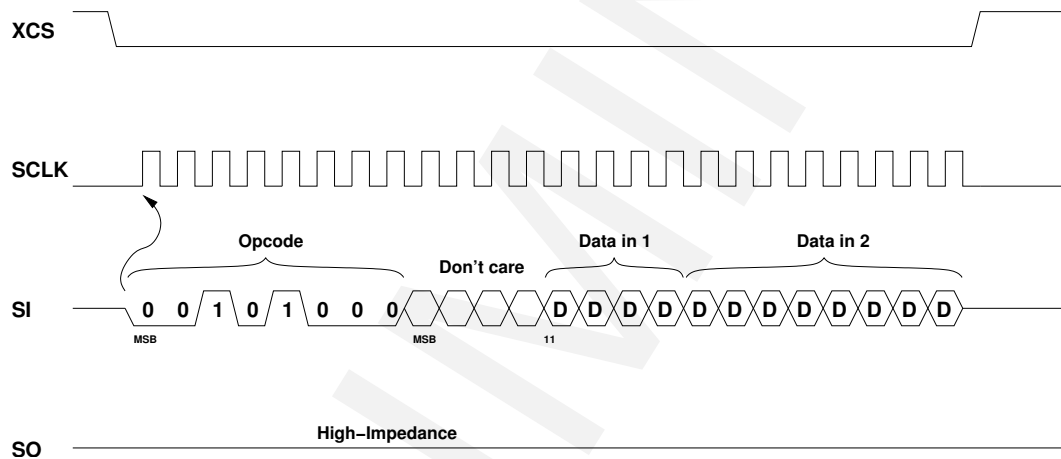


Figure 46: SPI Write Picture Start

## 8.2   Write Picture End (29h)

Picture End value defines the pixel position where the protoline starts after normal line. The position is defined by CSClk cycles (i.e. color subcarrier cycles) from the start of the line. The fixed 1.25 CSClk cycles long sync level at the beginning of each line is additional to given Picture End value. Note, that Picture End value has to be less than or equal to Line Length divided by 8. Also Picture End value has to be larger than Picture Start value.

To write the Picture End register XCS pin must be first asserted and opcode 29h clocked into the device. After that two byte value is clocked in the device via SI pin. The two byte value is input MSB (bit 15) first. The register value is 12 bits (11:0) wide, so bits 15 to 12 are don't cares. When XCS pin is deasserted the Picture End register will be updated.

Figure 47: SPI Write Picture End

## 8.3   Write Line Length (2Ah)

Line Length value defines the length of a single line. The Length is given in VClk cycles. The fixed 10 VClk cycles long sync level at the beginning of each line is additional to given Line Length value.

To write the Line Length register XCS pin must be first asserted and opcode 2Ah clocked into the device. After that two byte value is clocked in the device via SI pin. The two byte value is input MSB (bit 15) first. Bit 15 (VGP bit) of the register is used for selecting the digital 4-bit control output to PIO pins. The Line Length value is 12 bits (11:0) wide, so bits 14 to 12 are don't cares. When XCS pin is deasserted the Line Length register will be updated.



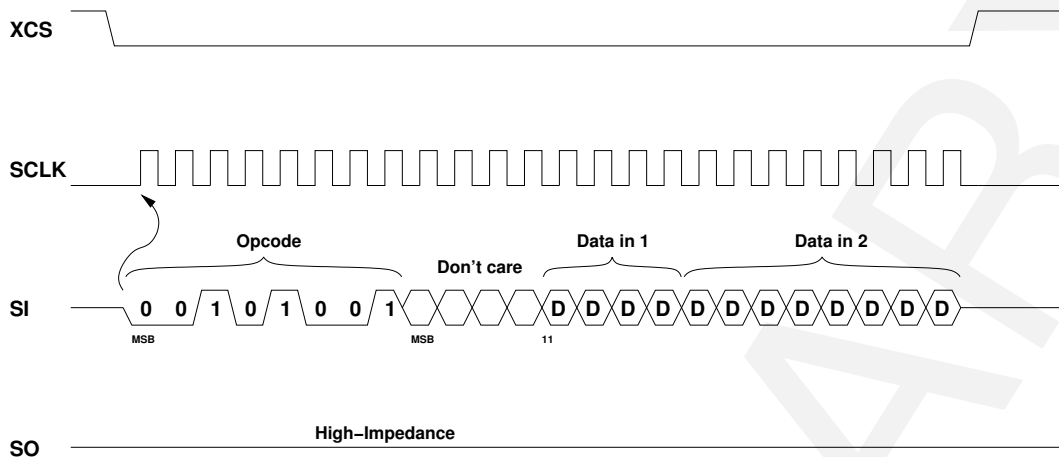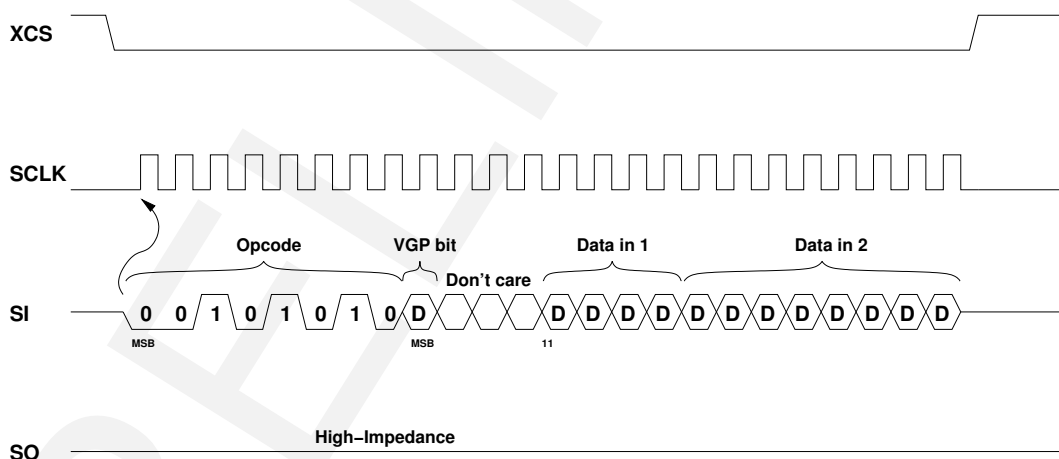Figure 48: SPI Write Line Length

In Direct DAC mode the Line Length is used to define the buffer length of DAC data buffer. The actual DAC data buffer length is the register value increased by one, i.e. the range is from 1 to 4096.

**8.4  Write Video Display Controller Control1 (2Bh)**

To write the Video Display Controller Control1 register XCS pin must be first asserted and opcode 2Bh clocked into the device. After that two byte value is clocked in the device via SI pin. The two byte value is input MSB (bit 15) first. When XCS pin is deasserted the Video Display Controller Control1 register will be updated.
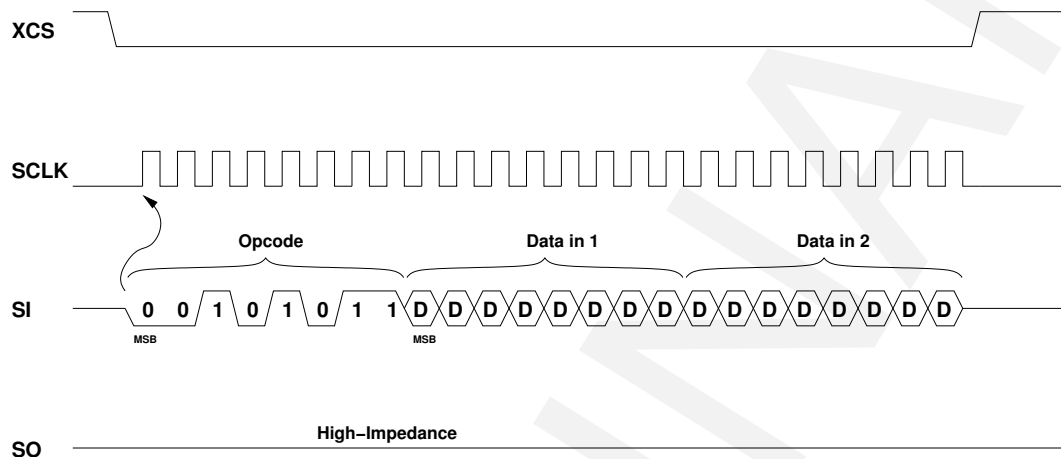


Figure 49: SPI Write Video Display Controller Control1

Video Display Controller Control1 register contains several parameters for Video Display Controller.

| Bit | | Name | Type | | Description |
|-----|---|------|------|---|-------------|
| 15 | DIRDAC | Direct DAC Mode | W | 0 | Direct DAC disabled (default) |
| | | | | 1 | Direct DAC enabled |
| 14 | TRUV | Translate U and V | W | 0 | U and V from SRAM (default) |
| | | | | 1 | U and V from table |
| 13 | CLKSEL | Clock select | W | 0 | VXTAL as clock source (default) |
| | | | | 1 | 8×PLL as clock |
| 12 | PLLENA | PLL enable | W | 0 | 8×PLL and crystal oscillator are disabled (default) |
| | | | | 1 | 8×PLL and crystal oscillator are enabled |
| 11-3 | DACDIV | Direct DAC clock divider bits 11-3 | W | 000h | High bits of divider (default) |
| 2-0 | UVSKIP | U and V skip cycles | W | 0h | UV skip disabled (default) |
| | | | | > 0h | UV skip enabled |

**DIRDAC Bit**  DIRDAC bit controls The Direct DAC mode of the Video Display Controller. In default mode after power-up bit value is "0", which means that Direct DAC mode is disabled.

Setting the bit "1" enables the Direct DAC mode and switches the controls of the Video Display Controller accordingly.

**TRUV Bit**   TRUV bit controls the use of U and V translate table. In default mode after power-up bit value is "0" and U and V data comes directly from SRAM according to microcode program.

When bit is set to "1" the U and V translate is enabled. In that mode with the data from SRAM is selected one of four 4-bit values from U and V tables.

**CLKSEL Bit**   CLKSEL bit selects the clock source of the Video Display Controller block. In default mode after power-up bit value is "0" and VXTAL crystal oscillator is used as clock input.

Setting the bit to "1" selects the output of 8x PLL as a clock source. Before the 8x PLL output can be selected as a clock source, 8x PLL has to be enabled by PLLENA bit and also it is good to check that the 8x PLL is locked to frequency of the VXTAL crystal oscillator.

**PLLENA Bit**   PLLENA bit enables the 8x PLL and the crystal oscillator. In default mode after power-up bit value is "0" and PLL and crystal oscillator are in power-down state.

Setting the bit to "1" sets the 8x PLL and crystal oscillator on. Writing PLLENA bit high is also used for starting the 8x PLL lock check sequence. After the PLLENA write the lock status can be checked by a SPI read of Current Line Value & PLL Lock . If 8x PLL is locked, then it can be switched as clock source for Video Display Controller. However, if 8x PLL is not locked the 8x PLL lock check sequence can be started again by writing "1" to PLLENA bit.

The Video DAC uses signals (band gap reference voltage and current bias) which are generated by 8x PLL. If Video DAC output is used then the 8x PLL has to be enabled also beforehand.

**DACDIV Bits**   These bits are the 9 MSBs of Direct DAC Mode clock divider. The 12-bit divider value is generated by concatenating DACDIV&"111" and the actual divider is DACDIV&"111"+1. The divider is used for dividing the Video Display Controller clock in Direct DAC mode so that lower frequency outputs can be generated. The divider range is from 8 to 4096 in increments of 8. The DACDIV default value is 000h.

**UVSKIP Bits**   These three bits are used for skipping the U and V data fetching from the SRAM for the given amount of microcode program runs. In default mode after power-up value of the bits is "000" and no U and V command lines of microcode program are skipped.

By setting the bits to a value larger than "000" then in the amount of microcode program runs defined by the UVSKIP bits the U and V command lines are skipped. This can be used to allocate relatively more data space of SRAM to Y information when needed.

## 8.5   Write Picture Index Start Address (2Ch)

To write the Picture Index Start Address register XCS pin must be first asserted and opcode 2Ch clocked into the device. After that the two byte value is clocked in the device via SI pin. MSB is clocked in first. Bits 15 and 14 are zeroes. When XCS pin is deasserted the Picture Index Start Address register will be updated.
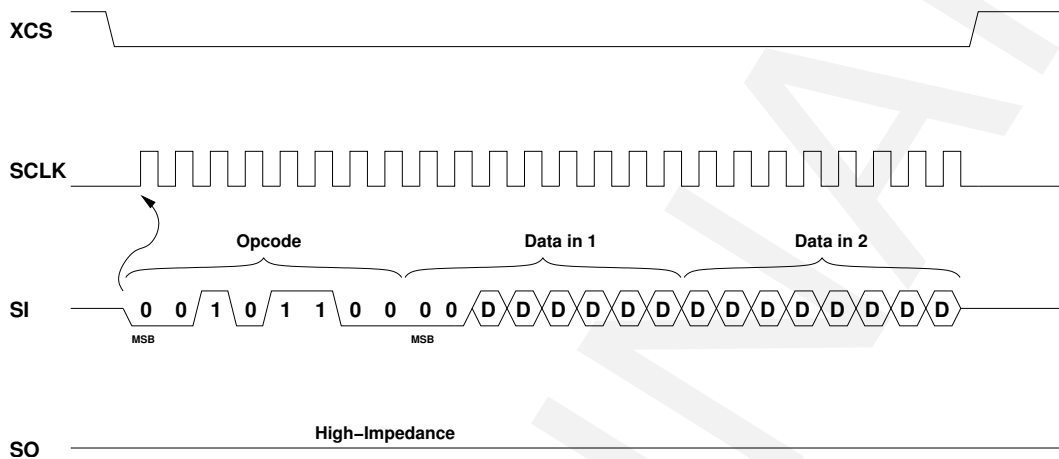


Figure 50: SPI Write Picture Index Start Address

The actual index start byte address is the register value shift left by two. At that address is the line index address of the line #0. Line index consists of three data bytes. Line index format is shown in detail in VS23S010D-L Guide. The line index addresses for consecutive lines are got by incrementing the picture index start byte address by three. The index addresses can be only in the first half of the SRAM.

If line index address is less than the index start byte address, then the current line is protoline, otherwise it is normal line (i.e. first protoline, then normal and finally end is again protoline). Note, that line index is a bit address and Picture Index Start Address has to be shift left by five for the above comparison.

Refer to VS23S010D-L Guide for more information about SRAM organization in Video Display Controller mode.

In Direct DAC mode the Index Start Address is used as the start address of DAC data buffer. The register value is shifted left by one to generate DAC data buffer start address, refer to VS23S010D-L Guide. In direct DAC mode all 16 bits of the Index Start address register are used. The value has to be larger than 0000h in Direct DAC mode.

## 8.6   Write Video Display Controller Control2 (2Dh)

To write the Video Display Controller Control2 register XCS pin must be first asserted and opcode 2Dh clocked into the device. After that two byte value is clocked in the device via SI

pin. The two byte value is input MSB (bit 15) first. When XCS pin is deasserted the Video Display Controller Control2 register will be updated.
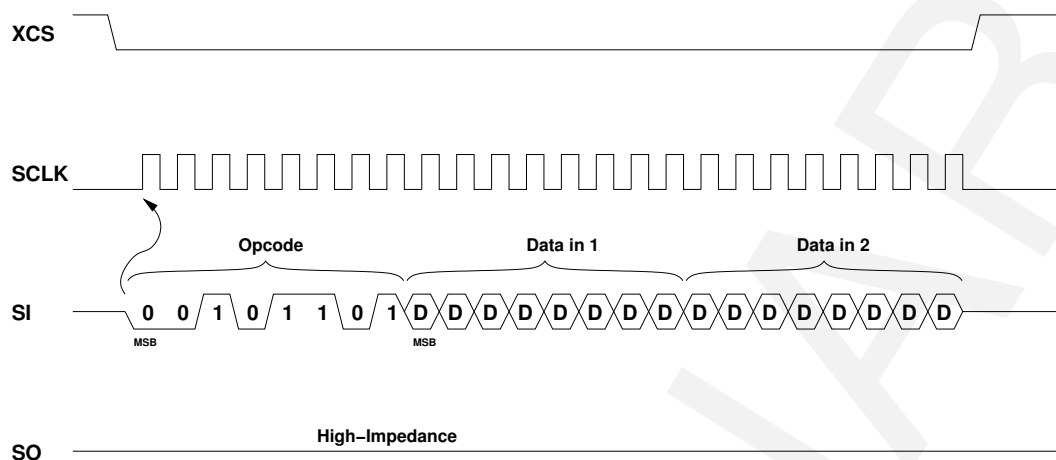


Figure 51: SPI Write Video Display Controller Control2

Video Display Controller Control2 register is written last to enable the Video Generator.

Video Display Controller Control2 register contains following parameters for Video Display Controller.

| Bit | | Name | Type | | Description |
|---|---|---|---|---|---|
| 15 | ENA | Enable Video Display Controller | W | 0 | Video Display Controller off (default) |
| | | | | 1 | Video Display Controller on |
| 14 | VMOD | Video Mode | W | 0 | NTSC (default) |
| | | | | 1 | PAL |
| 13-10 | PLEN | Program Length | W | 0h | PLEN+1 cycles, not allowed (default) |
| | | | | >0h | PLEN+1 cycles, usable range |
| 9-0 | LCNT | Line Count | W | 000h | LCNT+1 lines (default) |

**ENA Bit**   ENA bit enables the Video Display Controller. In default mode after power-up bit value is "0" and Video Display Controller is disabled.

Setting the bit to "1" will enable the Video Display Controller block. Before that the other Video Display Controller registers have to be written to correct values. Also line indexes and other video data need to be written to SRAM beforehand. It is of course possible to update video information in SRAM also when Video Display Controller is enabled.

**VMOD Bit**   VMOD bit is used to select between NTSC and PAL mode video output. Default value is "0" which selects NTSC mode.

Setting bit high selects PAL mode. In that mode the phase of part of the color information on the video signal is reversed with each line, i.e. V signal is negated.

When NTSC mode is selected, the CSClk frequency is 3.579545 MHz. When PAL is selected, the CSClk frequency is 4.433618 MHz.

**PLEN Bits**   PLEN bits define the amount of VClk cycles, which one run of the microcode program in normal line part lasts. The default value is 0h, which is not allowed. The protoline is not affected by these bits, there a program run lasts always eight cycles.

Write these bits to a value 1h or higher and then the program run lasts PLEN+1 VClk cycles.

**LCNT Bits**   LCNT bits are used to define the line count of video picture.  LCNT+1 is total amount of lines. Default value is 000h. Maximum amount of lines is 1024.

LCNT is used to define when the fetching of line indexes starts again from SRAM position given by Picture Index Start Address.

## 8.7   Write V Table (2Eh)

To write the V Table register XCS pin must be first asserted and opcode 2Eh clocked into the device. After that two byte value is clocked in the device via SI pin. The two byte value is input MSB (bit 15) first. When XCS pin is deasserted the V Table register will be updated.
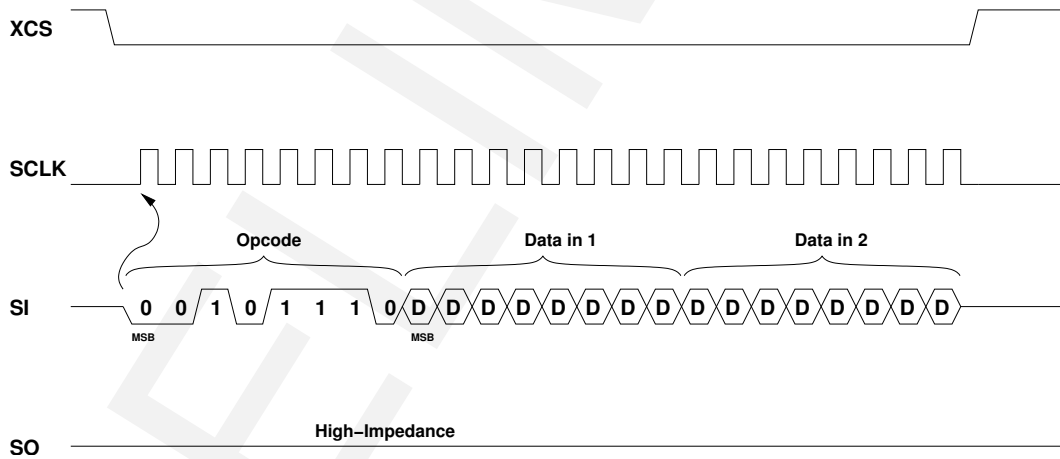


Figure 52: SPI Write V Table

| Bit | | Name | Type | | Description |
|---|---|---|---|---|---|
| 15-12 | V3 | V Table Value #3 | W | 0h | V#3 (default) |
| 11-8 | V2 | V Table Value #2 | W | 0h | V#2 (default) |
| 7-4 | V1 | V Table Value #1 | W | 0h | V#1 (default) |
| 3-0 | V0 | V Table Value #0 | W | 0h | V#0 (default) |

V Table is a register where four four-bit V values can be set.  Default value after power-up is 0000h.  V Table is used when TRUV bit in Video Display Controller Control1 register is set to

high. The two V bits fetched from SRAM by the microcode program are used select one of four-bit values from register as V output to Color Modulator instead of the value from SRAM. With SRAM bits "00" V0 is select as output, "01" selects V1, "10" selects V2 and finally with "11" the output is V3.

With TRUV bit and this table it is possible to generate with two SRAM bits an V output that is not symmetrical to mid-value.

## 8.8 Write U Table (2Fh)

To write the U Table register XCS pin must be first asserted and opcode 2Fh clocked into the device. After that two byte value is clocked in the device via SI pin. The two byte value is input MSB (bit 15) first. When XCS pin is deasserted the U Table register will be updated.
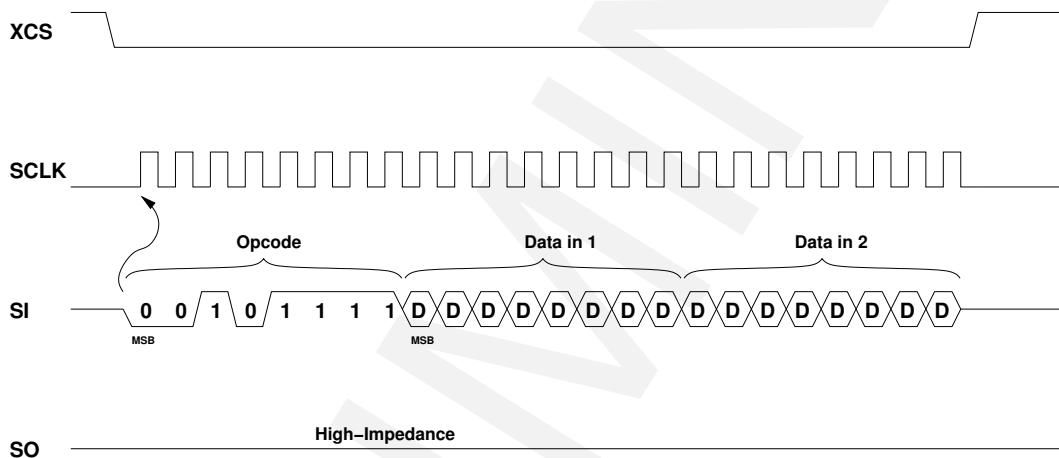


Figure 53: SPI Write U Table

| Bit | | Name | Type | | Description |
|---|---|---|---|---|---|
| 15-12 | U3 | U Table Value #3 | W | 0h | U#3 (default) |
| 11-8 | U2 | U Table Value #2 | W | 0h | U#2 (default) |
| 7-4 | U1 | U Table Value #1 | W | 0h | U#1 (default) |
| 3-0 | U0 | U Table Value #0 | W | 0h | U#0 (default) |

U Table is a register where four four-bit U values can be set. Default value after power-up is 0000h. U Table is used when TRUV bit in Video Display Controller Control1 register is set to high. The two U bits fetched from SRAM by the microcode program are used select one of four-bit values from register as U output to Color Modulator instead of the value from SRAM. With SRAM bits "00" U0 is select as output, "01" selects U1, "10" selects U2 and finally with "11" the output is U3.

With TRUV bit and this table it is possible to generate with two SRAM bits an U output that is not symmetrical to mid-value.

## 8.9  Write Program (30h)

To write the Program register XCS pin must be first asserted and opcode 30h clocked into the device. After that four byte value is clocked in the device via SI pin. The four byte value is input MSB (bit 31) first. When XCS pin is deasserted the Program register will be updated.
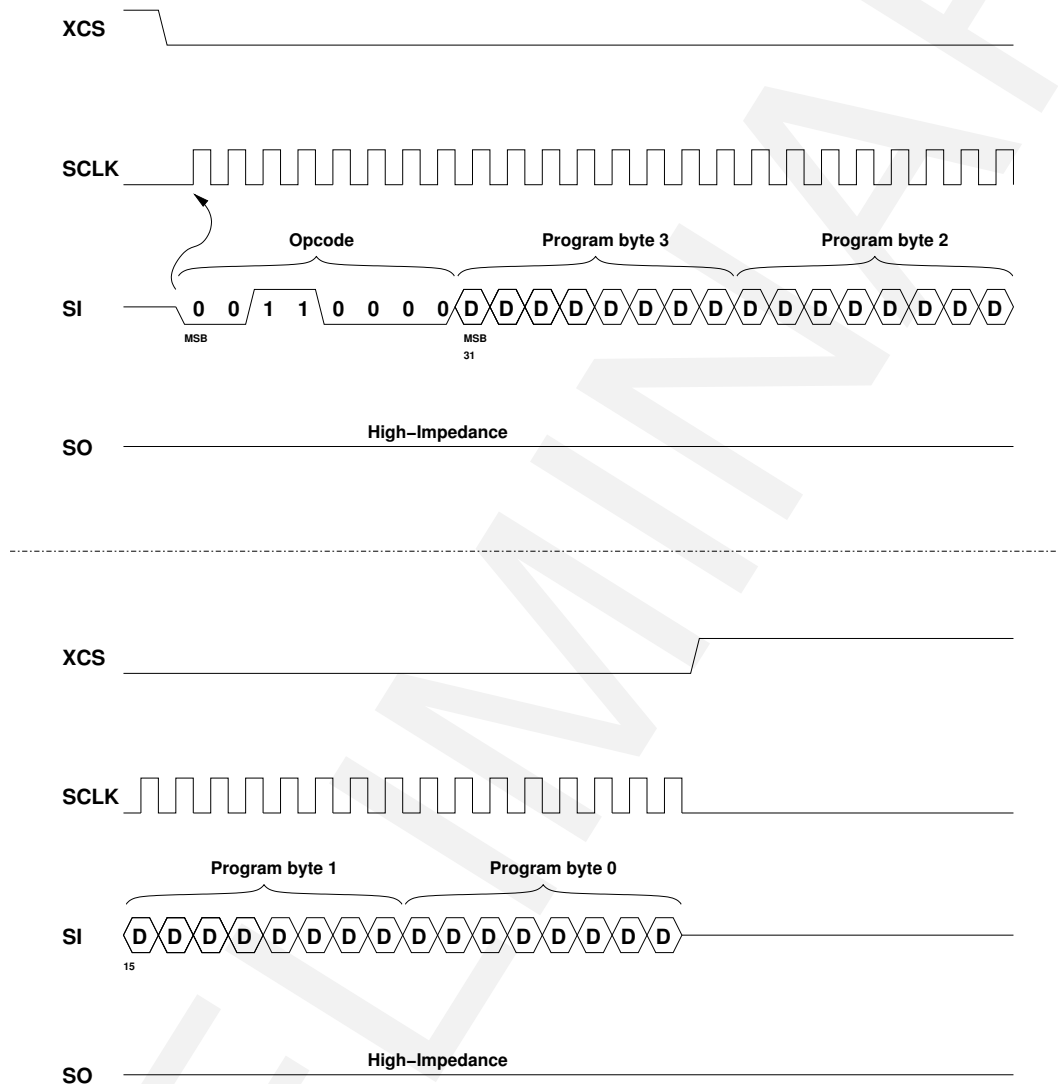


Figure 54: SPI Write Program

The Program register contains four lines (bytes) of microcode for the Video Generator. The next table shows the coding for one command line (byte). All four program bytes have the same coding. The default value of Program is 0000h after power-up.

| Bit | | Name | | Description |
|-----|-----|-----|-----|-----|
| 7-6 | CC | Command Code | 00 | Pick a (V) (default) |
| | | | 01 | Pick b (U) |
| | | | 10 | Pick y (Y) |
| | | | 11 | Pick - |
| 5-3 | BA | Bit Amount | 000 | Amount of bits taken (range 1 to 8) (default) |
| 2-0 | DS | Data Shifts | 000 | Amount of data shifting (range 0 to 6) (default) |

**CC Bits**   CC Bits are the command code for the operation. Pick a takes the V value either straight from SRAM data or from the V Table. Pick b takes the U value either straight from SRAM data or from the U Table. Pick y takes the Y value from the SRAM data. Pick - does not take any value, but it may do data shifting.

**BA Bits**   The amount of bits taken is BA+1. For U and V there is an upper limit of six bits. If U and V tables are used then two bits are needed for U and V.

**DS Bits**   DS bits define the shift amount of data. The shifts should equal the amount of bits taken. The shift range is from 0 to 6. If more than six bits are taken, then the rest of the shifts should be done on the next program cycle.

The program below translates to following 32-bit word, C4BC5C1Ch. Cycle 0 is in bits 7-0, cycle 1 in bits 15-8 and so on.

```
           pick          bits          shift
cycle      a|b|y|-       1...8         0...6

0          a             4             4          // take V(4), shift 4
1          b             4             4          // take U(4), shift 4
2          y             8             4          // take Y(8), shift 4
3          -             x             4          // idle, shift 4
```

Note, that the program defines the order of video data in SRAM. The data order in SRAM is the same as the order and amount of data taken in the microcode program.

## 8.10   Read Current Line and PLL Lock (53h)

The 10-bit Line Counter value can be read to determine on what line of the video picture the Video Display Controller is at the end of the SPI command. Additionally, 8x PLL lock state is given as is the state of the Video Generator Block Move, which is also shown on MVBLK pin.

To read the Video Display Controller Frame Length register XCS pin must be first asserted and opcode 53h clocked into the device. After that two byte value is clocked out from the device via SO pin. The two byte value is output MSB (bit 15) first. When XCS pin is deasserted, the clocking out of data is ended and SO pin goes to high-impedance state.

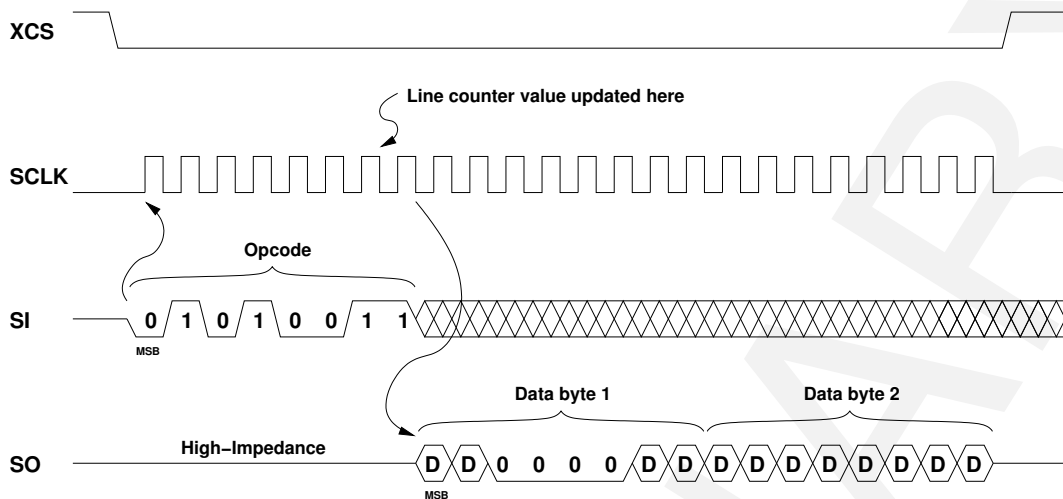| Bit | Name | | Type | | Description |
|-----|------|--|------|--|-------------|
| 15 | PLLLCK | 8×PLL Lock | R | 0 | PLL not locked (default) |
| | | | | 1 | PLL locked |
| 14 | MVBS | Block Move State | R | 0 | Block move idle (default) |
| | | | | 1 | Block move active |
| 9-0 | CL | Current Line | R | 000h | Line counter value (default) |

Figure 55: SPI Read Current Line and PLL Lock

**PLLLCK Bit**   PLLLCK is used to signal if the 8x PLL is locked to incoming VXTAL crystal oscillator frequency. The default value after power-up is "0" and 8x PLL is not locked when low value is read. If bit is high, 8x PLL is locked.

The PLL lock check sequence is described in Chapter 8.4.

**MVBS Bit**   The default value of MVBS is "0" and block move is inactive then. If bit is high, then block move is under way.

**CL Bits**   These bits show the current value of the Video Display Controller Line counter. Default value after reset is 000h. The range is from 0 to 1023. When the value is read, it is updated just before the SPI command is received by the VS23S010D-L.

## 8.11   Write Block Move Control1 (34h)

To write the Block Move Control1 register XCS pin must be first asserted and opcode 34h clocked into the device. After that five byte value is clocked in the device via SI pin. The five byte value is input MSB (bit 39) first. When XCS pin is deasserted the Block Move Control1 register will be updated.
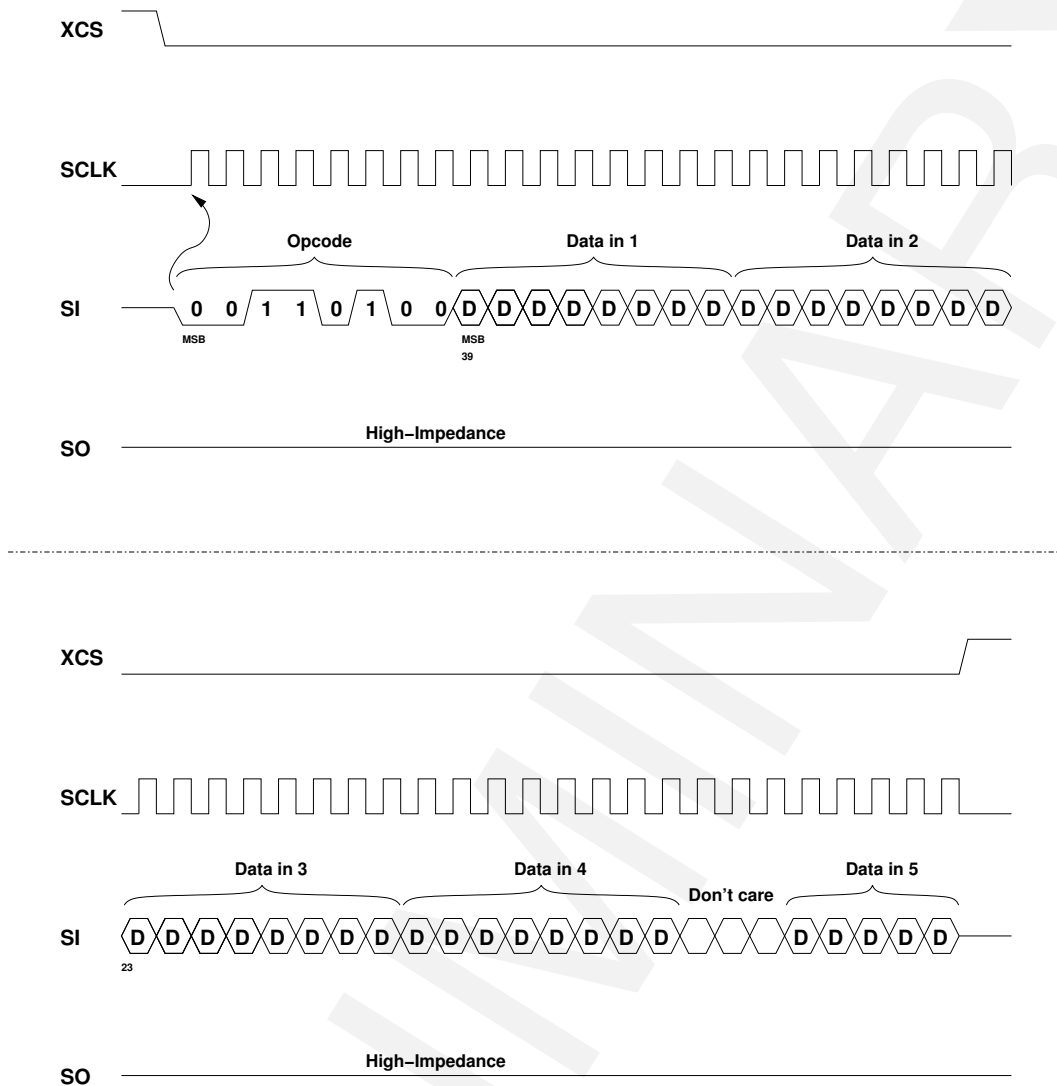
Figure 56: SPI Write Block Move Control1

| Bit | | Name | Type | | Description |
|---|---|---|---|---|---|
| 39-24 | MVSRC | Source Address | W | 0000h | Source address bits 16-1 (default) |
| 23-8 | MVTGT | Target Address | W | 0000h | Target address bits 16-1 (default) |
| 4 | PYF | Low-pass Y Filter | W | 0 | Filter disabled (default) |
| | | | | 1 | Filter enabled |
| 3 | DACC | DAC Control | W | 0 | Large current mode (default) |
| | | | | 1 | Small current mode |
| 2 | MVSRC0 | Source Address | W | 0 | Source address bit 0 (default) |
| 1 | MVTGT0 | Target Address | W | 0 | Target address bit 0 (default) |
| 0 | MVDIR | Move Direction | W | 0 | Move forward (default) |
| | | | | | Move backward |

Block Move is described generally in VS23S010D-L Guide.

**MVSRC, MVSRC0 Bits**   MVSRC bits define the 17-bit wide byte source start address for block move. The default value is 00000h. The address points to the first byte of the block. Note, address bit 0 is in position 2 of the 40-bit wide control word.

**MVTGT, MVTGT0 Bits**   MVTGT bits define the 17-bit wide byte target address for block move. The default value is 00000h. The address points to the first byte of the block target area. Note, address bit 0 is in position 1 of the 40-bit wide control word.

**PYF Bit**   PYF bit is used to enable the low-pass luminance filter. The default value after reset is "0" and the filter is disabled. To enable the filter write "1" to PYF bit.

**DACC Bit**   DACC bit is used to control Video DAC current. The default value set in reset is "0" which puts the Video DAC to large current mode. To change the Video DAC to small current mode write DACC bit to "1". Small current mode can be used with an external op amp.

**MVDIR Bit**   This bit selects the block move direction. The default value after reset is "0" and so the move direction is forward (i.e. SRAM addresses increase). By setting the bit high the move direction changes to backward (i.e. SRAM addresses decrease).

Note, when MVDIR bit is high, the MVSRC address is the for the last byte to be moved and also the MVTGT address is for the last target byte position.

### 8.12   Write Block Move Control2 (35h)

To write the Block Move Control2 register XCS pin must be first asserted and opcode 35h clocked into the device. After that four byte value is clocked in the device via SI pin. The four byte value is input MSB (bit 31) first. The five MSBs of the data are don't cares. When XCS pin is deasserted the Block Move Control2 register will be updated.

| Bit | | Name | Type | | Description |
|-----|-------|------------------|------|------|------------------------------------|
| 26-16 | MVSKP | Block Move Skip | W | 000h | Skip between lines (default) |
| 15-8 | MVLEN | Block Move Length | W | 00h | Length of block (X dir.) (default) |
| 7-0 | MVLIN | Block Move Lines | W | 00h | Amount of lines (Y dir.) (default) |

**MVSKP Bits**   MVSKP bits define the amount of bytes between two lines of the moved block. The default value is 000h and the range is from 1 to 2048 (i.e. the actual amount of bytes is MVSKP+1).
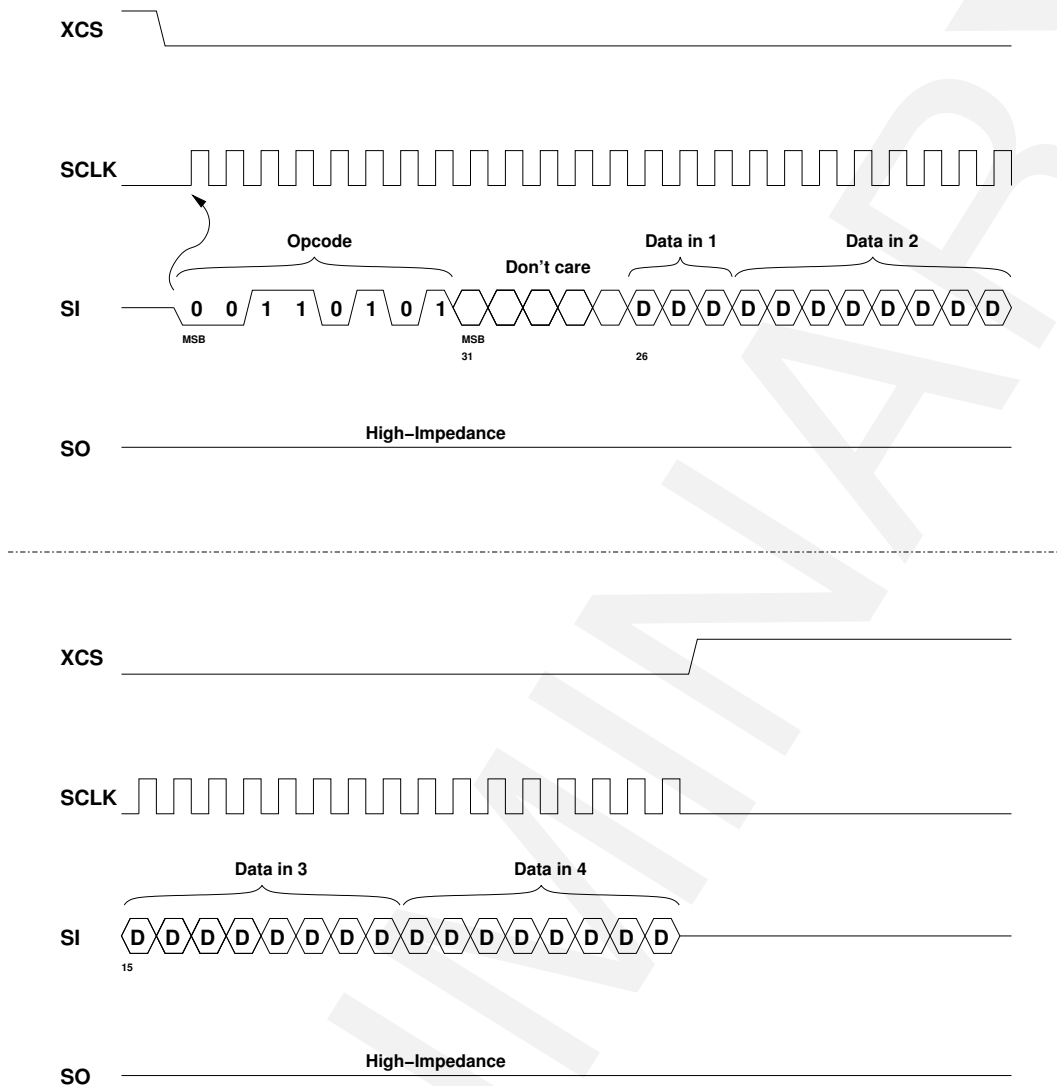
Figure 57: SPI Write Block Move Control2

**MVLEN Bits**   The MVLEN bits are used to define how many consecutive bytes belong to the block to be moved.  The MVLEN bits can be described as the X dimension of the block.  The default value after power-up is 00h and the range varies from 0 to 255.

**MVLIN Bits**   The MVLIN bits are used to define how many lines belong to the block to be moved. The MVLIN bits can be described as the Y dimension of the block. The default value after power-up is 00h and the range varies from 1 to 256 (i.e. the actual amount of lines is MVLIN+1).

## 8.13   Start Block Move (36h)

Start Block Move command is a one-byte command used to enable a single block move operation.  Before writing this command set the Block Move Control registers to correct values.

Check also that the previous block move is already finalized, i.e. MVBLK pin is low or MVBS bit is low, when Video Display Controller Status register is read.

To write the Start Block Move register XCS pin must be first asserted and opcode 36h clocked into the device.  When last bit of opcode is received the Block Move operation begins.  After writing the byte XCS pin is deasserted.
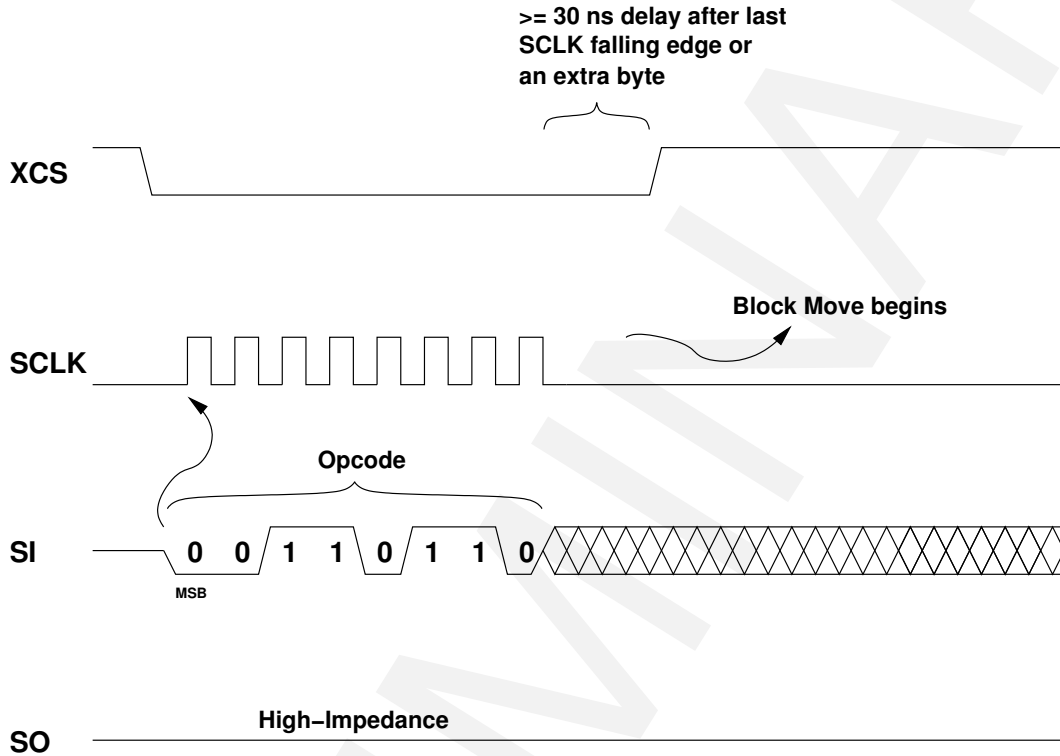


Figure 58: SPI Write Block Move Start

# 9   8-Bit Parallel Interface Commands and Addressing

8-bit parallel interface is an 8080 and NAND Flash type interface. It is an alternative interface to SRAM and when it is used the SPI interface must be inactive. So, XCS must be "1" when 8-bit parallel interface is used.

A valid 8-bit interface operation is started by first asserting XCSPAR pin. After that the host controller clocks out a valid 8-bit opcode. Following the opcode are three address bytes sent by the host controller. If there is a write operation the host sends data bytes to the device. In read operation the device starts clocking out data one clock cycle after the address. The operation is ended by deasserting the XCSPAR pin.

## 9.1   8-Bit Parallel Interface Read

The Read command can be used to sequentially read a continuous stream data from the device by providing clock signal once the initial starting address has been specified. The device has on internal address counter that increments on every cycle.

To perform a read operation, XCSPAR must first be asserted and read opcode 03h must be clocked into device. After the opcode three address bytes are clocked into the device to specify the starting address location of the first byte to read within SRAM. Note, that two LSBs of the address have to be zeros always.

After address bytes additional clock cycles will result in data being output on the parallel interface. When the last byte (1FFFFh) of the SRAM has been read, the reading will continue from the beginning of the array (00000h). If VS23S010D-L is part of the Multi-IC configuration then the reading will continue from the start address of the next VS23S010D-L in the system.

Deasserting the XCSPAR pin will terminate the read operation and parallel interface goes to high-impedance state.

## 9.2   8-Bit Parallel Interface Write

Prior to writing the device must be selected by bringing XCSPAR pin low. Once the device is selected the Write command can be started by issuing a Write instruction (opcode 02h) followed by a 24-bit address. Note, that two LSBs of the address have to be zeros always.

The device works in sequential mode where after the initial data byte additional bytes can be clocked into device. The internal address pointer is automatically incremented. When the internal address pointer reaches its maximum value (1FFFFh) it rolls over to 00000h. If VS23S010D-L is part of Multi-IC setup then the writing will continue to the beginning of the next VS23S010D-L SRAM array. This allows the operation to continue indefinitely, however, previ-
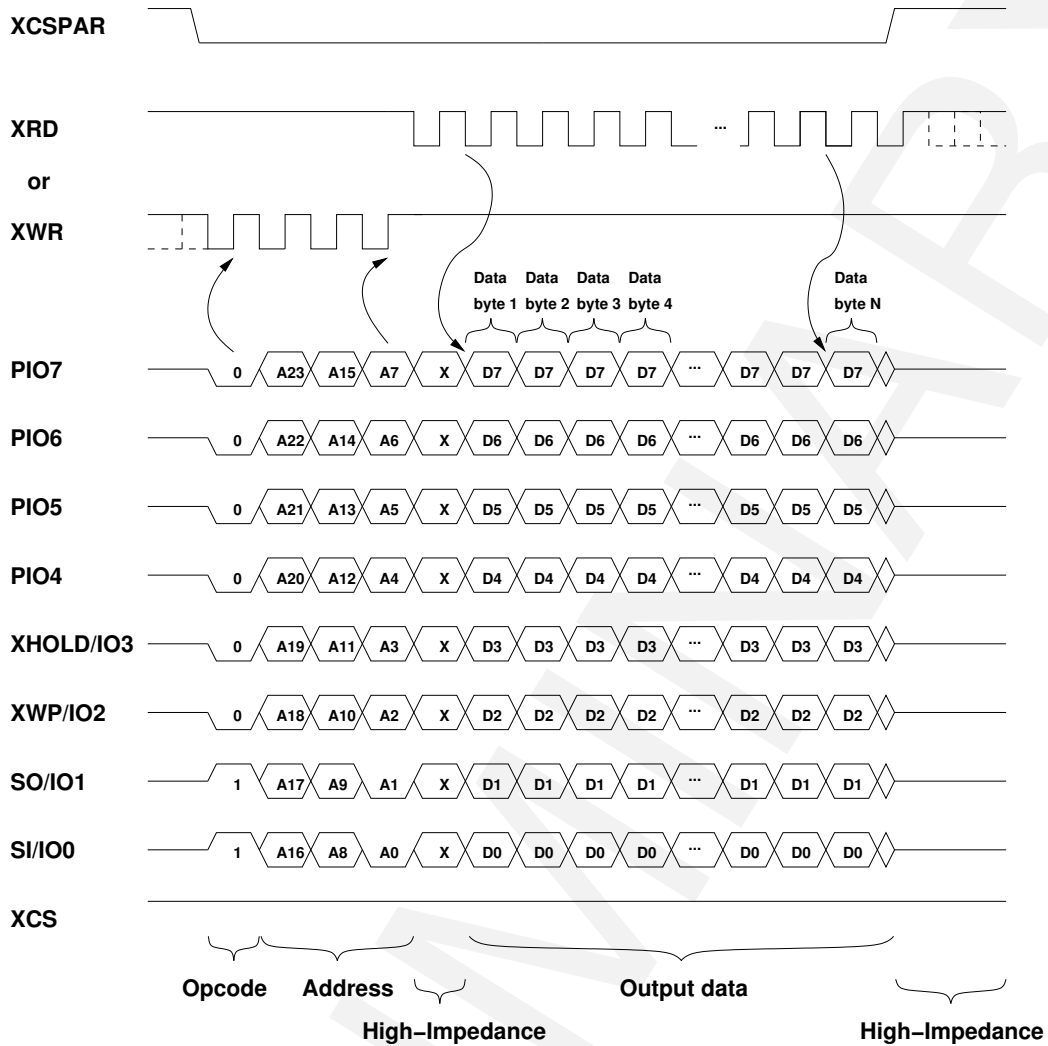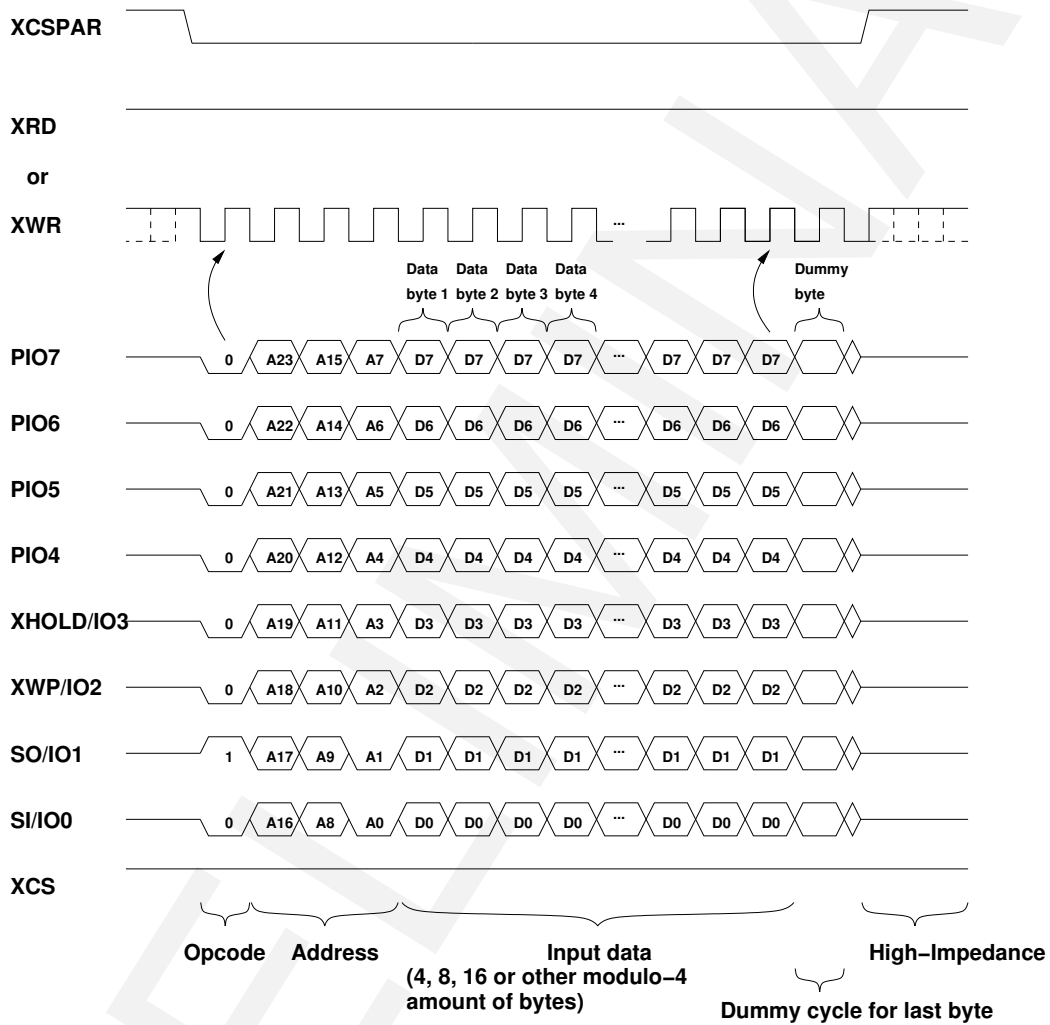
Figure 59: 8-Bit Parallel Interface Read

ous data will be overwritten. Note, that the amount of written data bytes has to be a multiple of four, e.g. 4, 8, 12, 16 and so on. Also note that after last byte at least one dummy byte is needed by the VS23S010D-L.

Figure 60: 8-Bit Parallel Interface Write

## 10 Errata

Below are described situations in which VS23S010D-L devices with date-code 1441 and 1519 behave differently than expected. VLSI Solution Oy has corrected these issues for current devices.

### 10.1 Powering Up

Depending on the rise time of VCC pin, the ambient temperature and the final level of VCC pin the startup of the VS23S010D-L can take relatively long time.

Typically when rise time of VCC is fast, the final VCC level is above 1.75 V and operating temperature is not much below room temperature, the VS23S010D-L is fully operational in 20 ms after power-up. However, if the slope of VCC is slow, the final level is below 1.7 V and the ambient temperature is near the lowest allowed, the powering up can take several seconds.

### 10.2 Idle Current

Typically when VS23S010D-L is in idle state the VCC current is below 100 $\mu$A. Sometimes the idle current of VS23S010D-L can be up to 300 $\mu$A after power-up.

There is a simple method for lowering the excess idle current. This can be done by making the following SPI operations five times. The SPI sequence for lowering idle current is as follows:

- Send a SPI command 2Bh and after that 1000h as data in single I/O mode.

- Send a SPI command 2Bh and after that 0000h as data in single I/O mode.

- Repeat the above sequence five times.

### 10.3 Slow Data Interface Clock Slope

If slope of a VS23S010D-L data interface clock (SCLK, XWR or XRD) is very slow (over 20 ns) then there may occur data errors when data is read from VS23S010D-L. The probability of this issue depends on data values and the used board design (crosstalk of signals and stability of power supply of VS23S010D-L).

## 11   Document Version Changes

This chapter describes the most important changes to this document.

**Version 0.96, 2018-10-01**

- Updated Chapter 3
- Changed couple of words to bytes.
- Fixed Chapter 6.1.4

**Version 0.95, 2017-06-15**

- Fixed XWP pin initial state.

**Version 0.94, 2017-01-13**

- Updated three 8-Bit Parallel Interface timing diagrams.

**Version 0.93, 2016-12-19**

- Fixed a typo.
- Updated schematic in Chapter 5

**Version 0.92, 2016-12-13**

- Changed and updated Chapter 3
- Changed U to V and vice versa.
- Separated Video Display Controller usage sections to VS23S010D-L Guide.

**Version 0.91, 2015-05-07**

- Changed and updated Chapter 3
- Added Chapter 10.3
- Corrected Video DAC current mode bit values
- Changed figures

**Version 0.9, 2015-01-16**

- Reorganized Chapter 3

**Version 0.8, 2015-01-09**

- VXTAL crystal oscillator for Video Display Controller clock
- Fast SPI write modes when Video Display Controller is on
- Digital video control outputs
- Added two bits to Status register.
- Added information about Video Display Controller use.
- Pull-up resistors in XWP/IO2 and XHOLD/IO3 pins
- Multi-bit address SPI modes
- Manufacturer and device ID  changed, amount of VS23S010D-Ls in system can be read.

**Version 0.7, 2013-05-30**

- Video Display Controller changed totally.
- Added Multi-IC functionality.
- Added SPI Word, Page and Sequential modes.
- Added Status register write.
- New packages and pin-outs

**Version 0.6, 2012-06-14**

- Updated clock frequency and power consumption information.
- Reorganized document according to functionality.

**Version 0.5, 2012-02-03**

- Added information for SOIC16 package.

## 12   Contact Information


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