

LOW NOISE JFET SF291



Introduction

The DSt Sensor Technologies Ltd – Charge resettable JFET SF291 has been approved by the Max Plank Institut fur Kern Physik in Heidelberg for the LEGEND project proving best in class performance for low intrinsic radioactivity, low noise and high sensitivity. LEGEND is one of the biggest Physics projects (Scaled up GERDA) which aims to develop a phased, 76Ge-based discovery of neutrinoless double-beta decay experiment with half-life beyond $1E28$ years. An extremely rare event to detect!

<https://www.mpp.mpg.de/en/research/astroparticle-physics-and-cosmology/gerda-andlegend-the-nature-of-the-neutrino/legend-future-of-germanium-detectors/>

Neutrinoless double-beta decay is only possible if neutrinos are their own antiparticle. Whether they are or not is not known, even though neutrinos are a fundamental ingredient for nuclear fission, nuclear fusion and the evolution of the universe and, thus, well researched. If they are their own antiparticle, this also contributes to one possible explanation for the disappearance of antimatter.

1.1 DESCRIPTION

The SF291 is a 3 terminal N-channel Low Noise JFET for amplifier applications requiring high transconductance and low noise. The device can be offered as an unsawn wafer with backside gold, or in a

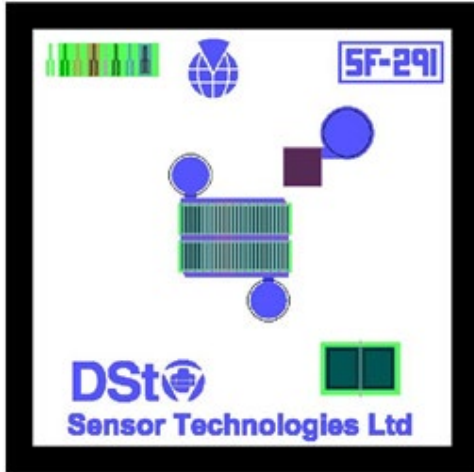
1.2 FEATURES

- Low Noise.
- High Transconductance
- Low leakage

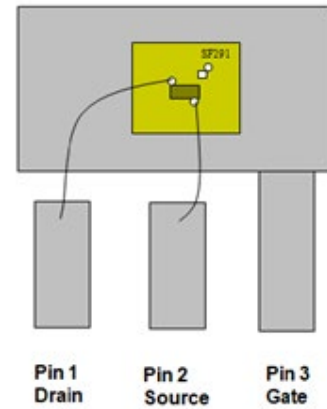
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SF291 Die Layout



T092 Pin-out



1.0 1.0 ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNITS
Drain Supply voltage	25	V
Drain Supply current	75	mA
Operating Temperature, TO	0 to 85	°C
Storage Temperature, TS	-40 - +105	°C

2.0 2.0 MECHANICAL SPECIFICATION

PARAMETER	RATING	UNITS
Chip size LxBxH	0.9 x 0.9 x 0.3	mm
Gate contact	On back-side, gold back-metal	
Bond pad sizes		microns

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3.0 ELECTRICAL SPECIFICATION

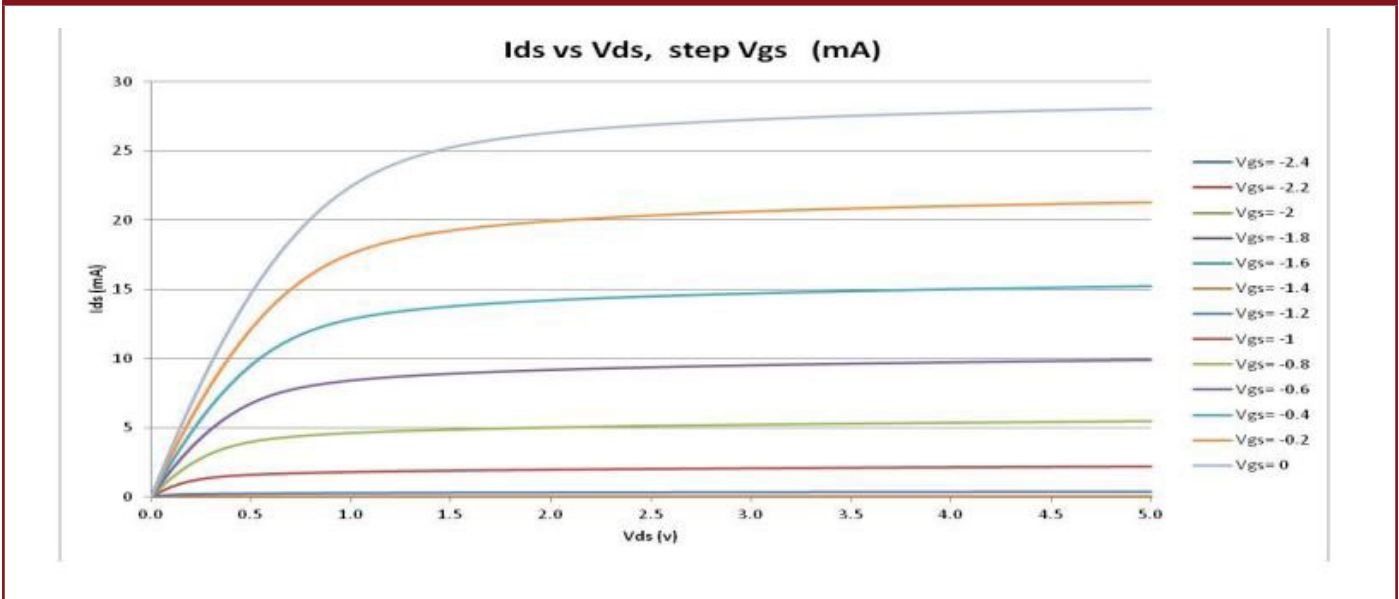
PARAMETER	SYMBOL	TEST CONDITIONS	SPEC	UNIT
Common-source forward transconductance.	gfs	Vgs = 0V, Vds = 3V	25 to 45	mS
Gate-source cut-off voltage	Vcutoff	Vds = 3V, Ids = 1uA	-0.8 to -2.5	V
Drain Current	Idss	Vds=3V, Vgs=0V	10 to 50	mA
Input capacitance	Ciss	Vds=0V, Vgs=0V	8 (typical)	pF
Gate-Source breakdown	BVgss	Vds= 0, Igs=1nA	< -15V	V

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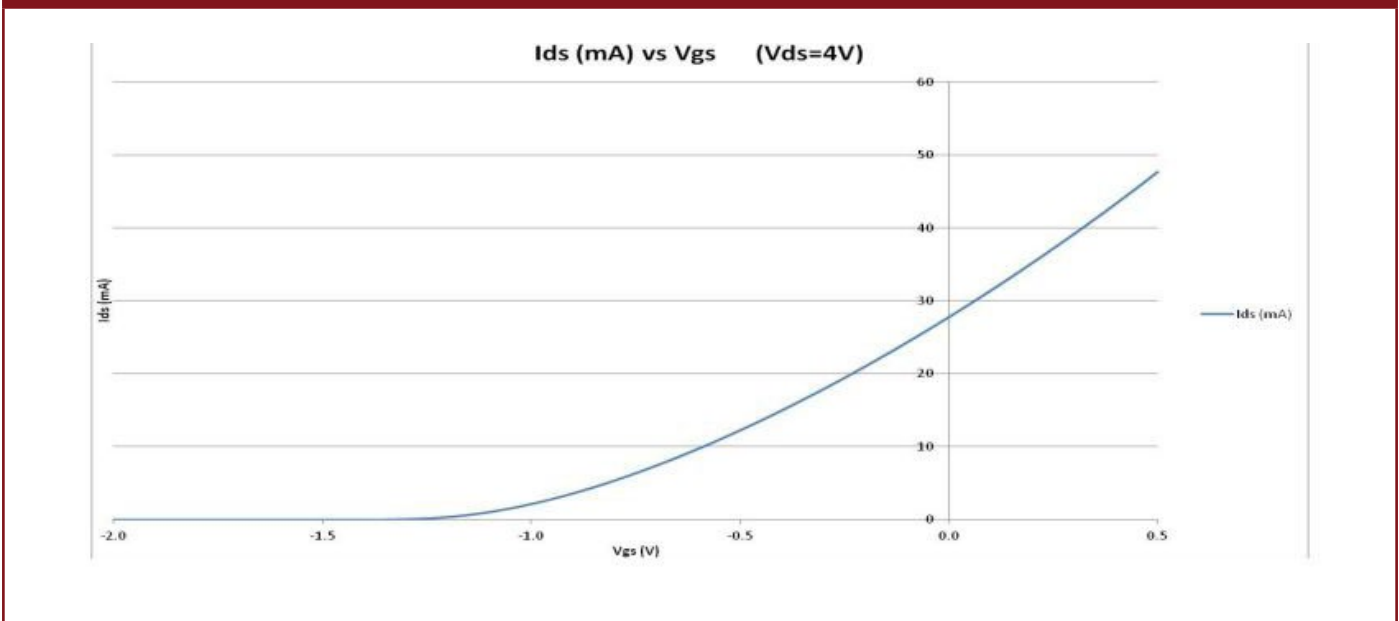


3.1 ELECTRICAL CURVES

Ids vs Vds, step Vgs (mA)



Ids (mA) vs Vgs (Vds=4v)



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4.0 TYPICAL NOISE DATA

Noise in $nV\sqrt{Hz}$

10Hz	100Hz	1kHz	10kHz	100kHz	V _{gs}
1.25	0.89	0.85	0.82	0.66	1.12

V_{ds} = 3V, I_{ds} = 10mA

5.0 APPLICATION NOTE

As typically used in Nuclear Particle Detection

Overview: Front End Electronics

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