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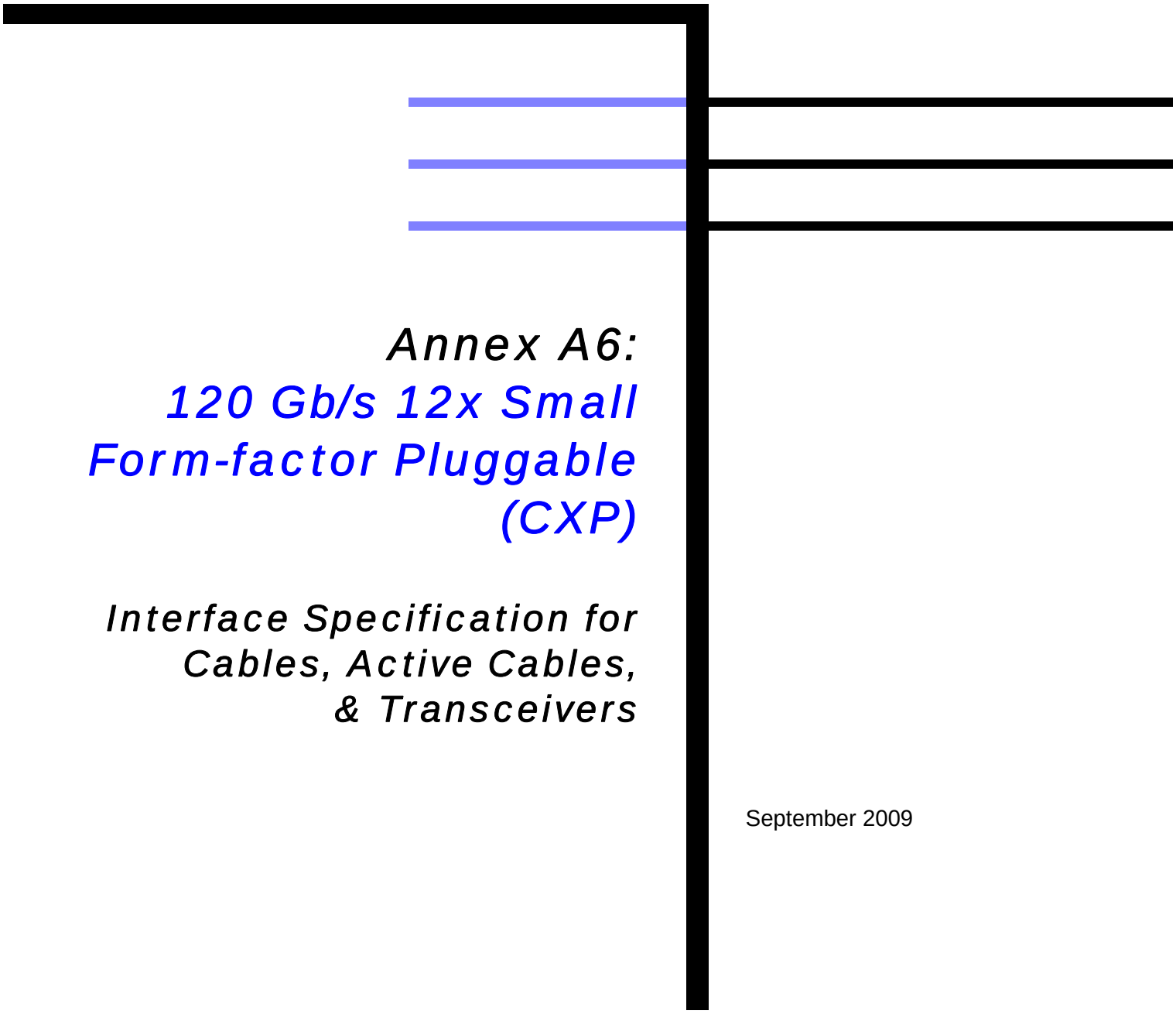

Annex A6:
120 Gb/s 12x Small Form-factor Pluggable (CXP)

Interface Specification for Cables, Active Cables, & Transceivers

September 2009

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Table 0 Revision History

Revision	Date	Revisions
1.0	9/18/2009	Released Version

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CHAPTER 1: OVERVIEW

This specification is a description of a 12x form-factor pluggable active device interface, with 12 transmit and 12 receive lanes, capable of supporting bit-rates in excess of 10 Gb/s per lane on a variety of electrical and optical transmission technologies.

This specification describes the form factor, electrical, mechanical, power, and thermal interfaces between the devices or cables and the systems. The transmission technology (e.g., optical or electronic), transmission medium (e.g., single-mode, multi-mode fiber, or copper), form factor (i.e., with cable attached to the pluggable device, or detachable with a separable connector), and physical layer definition for the communication between transceivers are not explicitly specified. However, the specifications are intended to support several different technologies, including VCSEL/MMF parallel ribbon fiber links.

The current primary target for this technology is the InfiniBand architecture, at the 12x-QDR (Quad Data Rate) rate, as well as DDR and SDR rates. Other standards, such as Ethernet at the 100 Gb/s data rate and Fibre Channel, may be supported as well.[1]

1.1 DESIGN TARGETS AND COMPATIBILITY

This paragraph describes the design targets of the device. These targets are used as foundation for making decisions regarding the design of the interface and related devices.

- Transmission Bandwidth: The interface should be capable of comfortably supporting data communications at up to 10.5 Gb/s on each of 12 lanes, in order to support at least the following link options.
  - 12x QDR InfiniBand links, operating at (12+12)x10.0 Gb/s.
  - 100 Gb/s Ethernet, using a 10-lane PHY and a 64b/66b line code (e.g., 10.3125 using 64b/66b on 10 lanes), as defined by the IEEE.
- Electrical Interface Compatibility: Low-speed signals should be compatible with electrical interface specifications of Section 2.3 on page 14, high-speed signals should be compatible with InfiniBand QDR

1. Terminology note: The name CXP is intended to derive from several sources:
C = the Roman numeral for 100, indicating a form-factor targeted for >100 Gb/s per direction transmission. C is also the hexadecimal character for 12, indicating an interface with 12 lanes per direction.
XP = eXtended-capability Pluggable form-factor.

electrical interface specifications defined in the *InfiniBand Specification, Vol. 2,* Chapter 6, as extended or modified in Chapter 3: High-Speed Electrical Signaling of this annex.

- Transmission Media Compatibility: This interface is expected to support modules or cables of at least the following types:
  - Copper Cable, un-equalized or passively equalized,
  - Active Copper Cable with receive-side active equalization,
  - Active Copper Cable with active equalization on both transmit and receive sides,
  - Active Optical Cable Assembly, and
  - Separable Optical Transceiver and fiber optic cable.

  This variety of transmission technologies allow cost-effective implementation across a wide range of link lengths using the same host receptacle and electrical interfaces. Example representative link lengths are shown in Table 1 on page 9. Note that these link lengths are not precise, and are not intended to be normative.

Table 1 Representative Transmission Media and Link Lengths

Transmission Medium	Transmission Speed		
	QDR 10.0 Gb/s	DDR 5.0 Gb/s	SDR 2.5 Gb/s
Copper Cable, un-equalized or passively equalized	~6-8 m	~9-12 m	12-15 m
Active Copper, Rx-side active	9-12 m	8-20 m	12-18 m
Active Copper, Both sides active	14-20 m	20-30 m	30-50 m
Active Optical Cable Assembly	~100 - 300 m	100-300 m	100-300 m
Optical Transceiver	Up to ~10 km	Up to ~10 km	Up to ~10 km

Note also that explicit transmission technology choices within an active cable assembly (e.g., single-mode vs. multi-mode optical transmission, glass vs. plastic optical fiber, or equalization and coding techniques) are not addressed by this specification. This document specifies the electrical, mechanical and thermal interfaces between "module" (cable plug, or transceiver) and the host. Any transmission technology which transports data transmission between two interfaces at the specified speed with good signal integrity at each end is compliant.

Figure 1 on page 10 illustrates the CXP conceptual model, with a single host interface receptacle supporting a variety of transmission technologies, cost-effectively supporting a variety of link lengths.

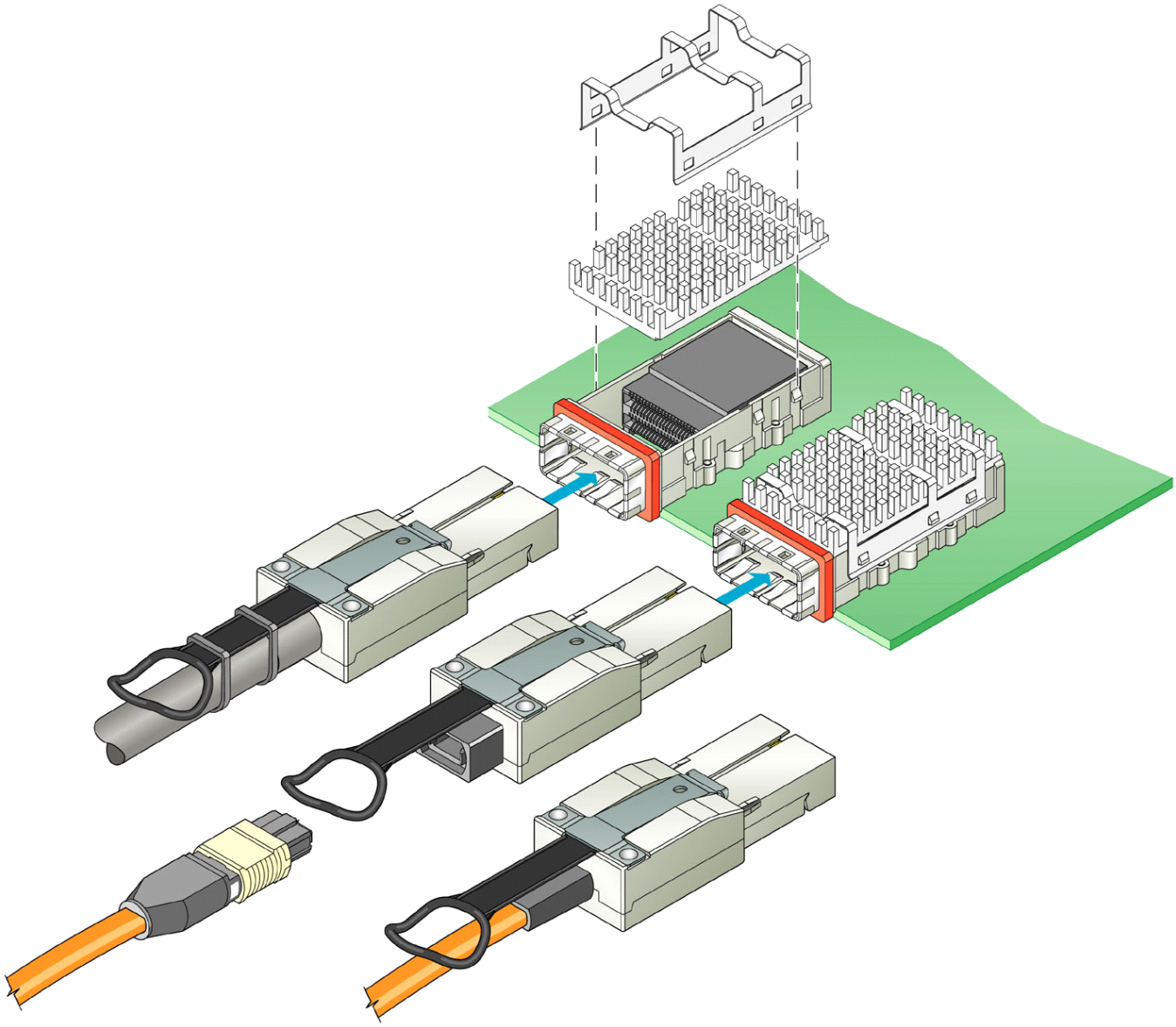

Figure 1 CXP Conceptual Model

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CHAPTER 2: ELECTRICAL SPECIFICATION

This chapter contains contact definitions for the CXP transceiver. Compliance points for high-speed signal electrical measurements are defined in Figure 4 on page 23. Compliance points for all other electrical signals are at comparable points at the host edge card connector.

2.1 ELECTRICAL CONNECTOR

Table 2 on page 13 shows the signal symbols and contact numbering for the CXP module edge connectors. The diagram shows the module PCB edge as a top and bottom view, for both circuit cards in the two-level connector. There are 21 pads per level, for a total of 84, with 48 pads allocated for (12+12) differential pairs, 28 for Signal Common or Ground (GND), 4 for power connections, 4 for control/service. Mapping of these contacts into physical locations in the device connector and the receptacle are shown in Figure 8 on page 32, and Figure 10 on page 34, respectively.

The operation of the low-speed control and status lines (PRSNT_L, Int_L/Reset_L, SCL, & SDA) is described in Section 2.3, "Low-Speed Electrical Contact/Signal Definitions," on page 14, and operation of the high-speed lines for receiving and transmitting data is described in Section 2.4, "High-Speed Electrical Contact/Signal Definitions," on page 16.

Table 2 Contact Assignments for 12x Pluggable-CXP Interface

Bottom side				Top Side		
I/O #	**Name**	**Contact Length**		**Contact Length**	**Name**	**I/O #**
Receiver -- Top Card						
C1	GND				GND	D1
C2	Rx1p				Rx0p	D2
C3	Rx1n				Rx0n	D3
C4	GND				GND	D4
C5	Rx3p				Rx2p	D5
C6	Rx3n				Rx2n	D6
C7	GND				GND	D7
C8	Rx5p				Rx4p	D8
C9	Rx5n				Rx4n	D9
C10	GND				GND	D10
C11	Rx7p				Rx6p	D11
C12	Rx7n				Rx6n	D12
C13	GND				GND	D13
C14	Rx9p				Rx8p	D14
C15	Rx9n				Rx8n	D15
C16	GND				GND	D16
C17	Rx11p				Rx10p	D17
C18	Rx11n				Rx10n	D18
C19	GND				GND	D19
C20	PRSNT_L				Vcc3.3-Rx	D20
C21	Int_L/Reset_L				Vcc12-Rx	D21
Transmitter -- Bottom Card						
A1	GND				GND	B1
A2	Tx1p				Tx0p	B2
A3	Tx1n				Tx0n	B3
A4	GND				GND	B4
A5	Tx3p				Tx2p	B5
A6	Tx3n				Tx2n	B6
A7	GND				GND	B7
A8	Tx5p				Tx4p	B8
A9	Tx5n				Tx4n	B9
A10	GND				GND	B10
A11	Tx7p				Tx6p	B11
A12	Tx7n				Tx6n	B12
A13	GND				GND	B13
A14	Tx9p				Tx8p	B14
A15	Tx9n				Tx8n	B15
A16	GND				GND	B16
A17	Tx11p				Tx10p	B17
A18	Tx11n				Tx10n	B18
A19	GND				GND	B19
A20	SCL				Vcc3.3-Tx	B20
A21	SDA				Vcc12-Tx	B21

2.2 HOST BOARD SCHEMATIC

Figure 2 on page 15 shows an example of a host board schematic for CXP, with connections to host SerDes and control logic. For EMI protection the signals to the connector should be shut off when the CXP transceiver is removed. Standard board layout practices such as connections to Vcc3.3 and Vcc12 and GND with vias, use of short and equal-length differential signal lines, use of microstrip-lines, and 50Ω /100Ω terminations are recommended. The chassis ground (case common) of the CXP module should be isolated from the module's circuit ground, GND.

Note that AC coupling capacitors on the high-speed signals are implemented inside the device or cable. This is opposite to the configuration described in *InfiniBand Architecture Specification, Volume 2*, Compliance Statement C6-8.2.1, which specifies that DC blocking capacitors shall not be mounted inside the cable assembly for cables using MicroGiga-CN connectors.

2.3 LOW-SPEED ELECTRICAL CONTACT/SIGNAL DEFINITIONS

2.3.1 SDA, SCL

SCL is the clock of the two-wire serial interface, and SDA is the data for the 2-wire serial interface. Operation of this interface is described in detail in Chapter 7: Management Interface, SCL and SDA must be pulled up in the host, through an pull-up resistor of value appropriate to the overall bus capacitance and the rise and fall time requirements listed in Table 19 on page 60.

2.3.2 INT_L/RESET_L

Int_L/Reset_L is a bidirectional signal. When driven from the host, it operates logically as a Reset signal. When driven from the module, it operates logically as an Interrupt signal. In both cases, the signal is asserted low, as indicated by the '_L' suffix. The Int_L/Reset_L signal requires open collector outputs in both the host and module, and must be pulled up on the host board, as described for SDA and SCL. Int_L and Reset_L indications are distinguished from each other by timing - a shorter assertion, driven by the module, indicates an interrupt, and a longer assertion of the signal, driven by the host, indicates a reset, as listed in Table 21 on page 62.

Int_L operation: When Int_L/Reset_L is pulled "Low" by the module for longer than the minimum interrupt pulse width ($t_{Int\_L,PW\text{-}min}$) and shorter than the maximum interrupt pulse width ($t_{Int\_L,PW\text{-}max}$) the signal signifies an interrupt. An interrupt indicates a possible module operational fault or a module status critical to the host system. The host identifies the cause of the interrupt using the 2-wire serial interface. Int_L must operate in pulse mode (vs. static mode), in order to distinguish a short interrupt signal from a longer reset signal, so the module must de-assert Int_L/Reset_L after the interrupt has been signaled.

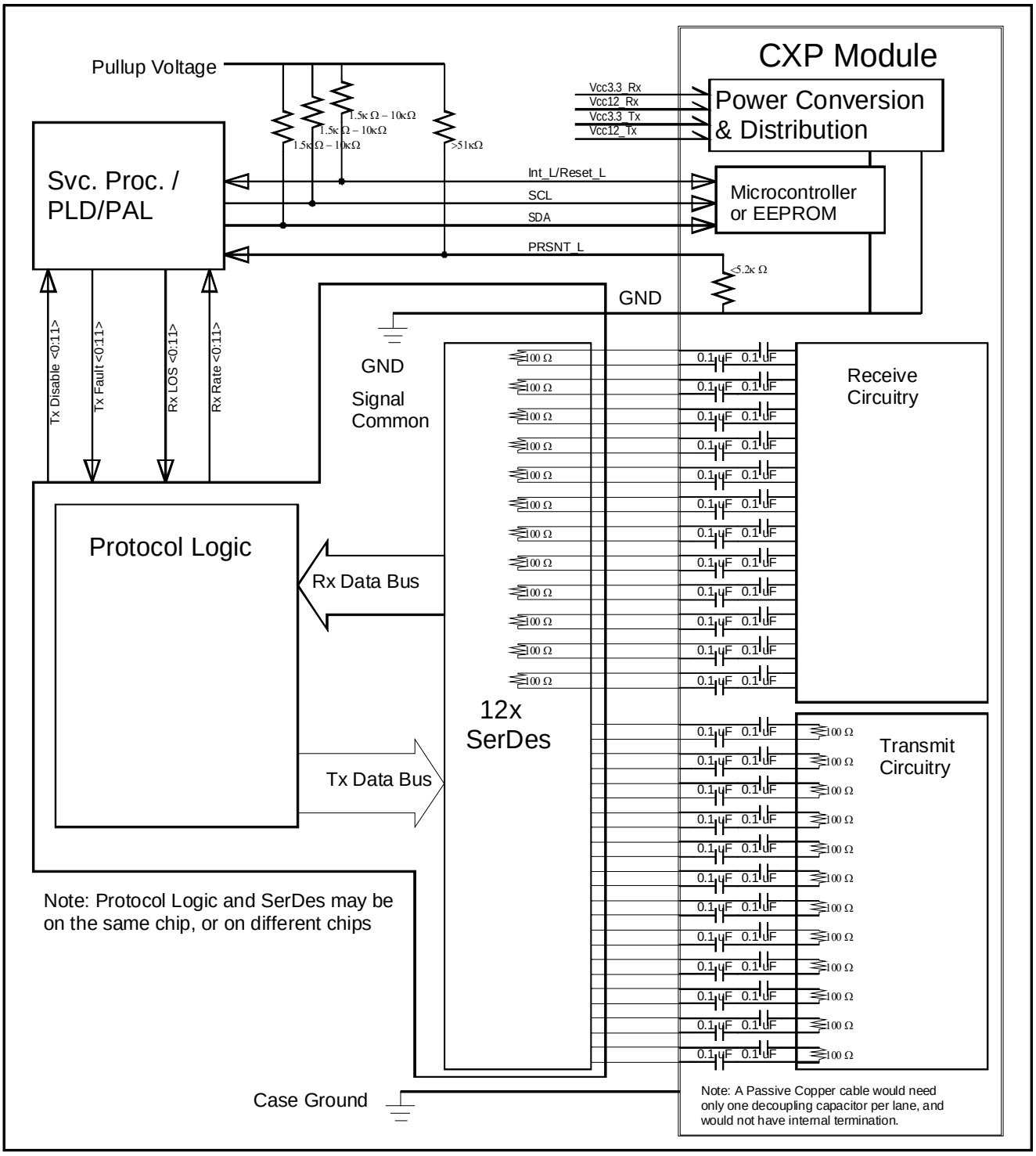


Figure 2 Example Host Board Schematic

Reset_L operation: When the Int_L/Reset_L signal is pulled "Low" by the host for longer than the minimum reset pulse length ($t_{reset\_L,PW\text{-}min}$), it initiates a complete module reset, returning all user module settings to their default state. There is no maximum reset pulse length. Module Reset Assert Time (**t_init**) starts on the rising edge after the low level on the Reset_L signal is released. During the execution of a reset (**t_init**) the host shall disregard all status bits until the module indicates a completion of the reset interrupt. The module indicates this by posting an Int_L signal with the Data_Not_Ready bit (Memory Map, Byte 2, bit 0) negated (set to 0). Note that on power up (including hot insertion) the module should post this completion of reset interrupt without requiring a reset from the host.

2.3.3 PRSNT_L

PRSNT_L is used to indicate when the module is plugged into the host receptacle. PRSNT_L is pulled up to Vcc3.3 on the host board through ≥50 kOhm. It is pulled down to signal common through 5.2 kOhm in modules requiring 12V power, and tied directly down to signal common (no resistor) in modules requiring 3.3V power only. The PRSNT_L signal is asserted "Low" when inserted and deasserted "High" when the module is physically absent from the host connector.

2.4 HIGH-SPEED ELECTRICAL CONTACT/SIGNAL DEFINITIONS

2.4.1 RECEIVE SIGNALS: RX[0-11][P/N]

Rx[0-11][p/n] are CXP module receiver data outputs. They are AC-coupled differential lines that should be terminated with 100 Ohm differential at the Host ASIC or SerDes. The AC coupling is inside the CXP module and not required on the Host board.

Output squelch for loss of input signal (Rx Squelch), is an optional function. Where implemented it shall function as follows. In the event of the optical or electrical signal on any physical lane becoming equal to or less than the level required to assert loss of signals (Rx LOS), then the receiver data output for that lane shall be squelched or disabled. In the squelched or disabled state, output impedance levels are maintained while the differential voltage swing shall be less than 50 mVpp, This voltage swing limit provides margin vs. the value specified for V_{RSD}, Signal Threshold for receiver signal detection (85 mVpp in Rel. 1.2.1) in *InfiniBand Architecture Specification, Volume 2*, Chapter 6: High Speed Electrical Signaling - 2.5, 5.0, & 10.0 Gb/s

In normal operation, where Rx Squelch is implemented, the default case has Rx Squelch active. Rx Squelch can be deactivated using Rx Squelch Disable through the 2-wire serial interface. Rx Squelch Disable is an optional function.

2.4.2 TRANSMIT SIGNALS: TX[0-11][P/N]

Tx[0-11][p/n] are CXP module transmitter data inputs. They are AC-coupled differential lines with 100 Ohm differential terminations inside the CXP module. The AC coupling is inside the CXP module and not required on the Host board.

Output squelch (Tx Squelch), for loss of input signal, (Tx LOS), is an optional function. Where implemented it shall function as follows. In the event of the differential, peak-to-peak electrical signal on any lane becomes equal to or less than 50 mVpp, then the transmitter optical output for that lane shall be squelched and the associated Tx LOS flag set. For an optical transceiver with separable optical connector, the optical modulation amplitude (OMA) when squelched shall be less than or equal to -26 dBm.

In normal operation, where Tx Squelch is implemented, the default case has Tx Squelch active. Tx Squelch can be deactivated using Tx Squelch Disable through the 2-wire serial interface. Tx Squelch Disable is an optional function.

2.5 POWER REQUIREMENTS

Power for the module is supplied through 4 contacts: Vcc3.3-Rx, Vcc12-Rx, Vcc3.3-Tx and Vcc12-Tx. Power is applied concurrently to them.

Since different classes of modules exist with pre-defined maximum power consumption limits, it is necessary to avoid exceeding the system power supply limits and cooling capacity when a module is inserted into a system designed to only accommodate lower power modules. It is recommended that the host, through the management interface, identify the power consumption class of the module before allowing the module to go into high power mode.

A host board together with the CXP module(s) forms an integrated power system. The host supplies stable power to the module. The module limits electrical noise coupled back into the host system and limits inrush charge/current during hot plug insertion.

All specifications shall be met at the maximum power supply current. No power sequencing of the power supply is required of the host system since the module sequences the contacts in the order of ground, supply and signals during insertion.

2.5.1 HOST POWER SUPPLY FILTERING

The host board should use the power supply filtering network shown in Figure 3 on page 18, or an equivalent. Any voltage drop across a filter network on the host is counted against the host DC set point accuracy spec-

ification. Inductors with DC Resistance of less than 0.1 Ω should be used in order to maintain the required voltage at the Host Edge Card Connector.

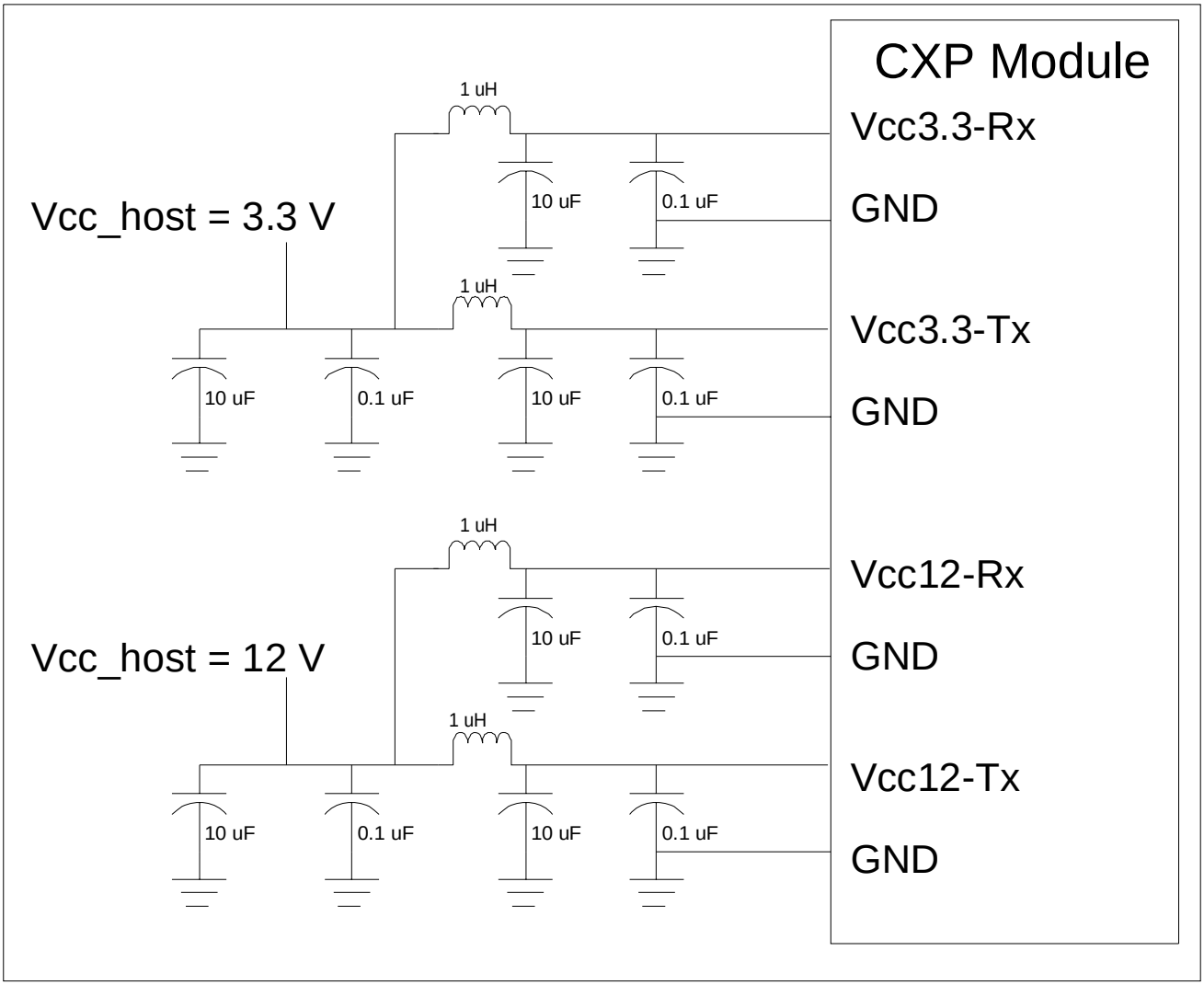


Figure 3 Recommended Host Board Power Supply Filtering

2.5.2 HOST POWER SUPPLY SPECIFICATIONS

The specification for the power supply is shown in Table 3 on page 19.

Table 3 Power Supply Specification

Parameter	Min	Nominal	Max	Unit	Condition
Vcc12_host		12			Measured at Vcc12-Tx and Vcc12-Rx
Vcc12 set point accuracy	-5		+5	%	Measured at Vcc12-Tx and Vcc12-Rx.
Vcc12 Power supply noise including ripple			50	mVpp	1kHz to frequency of operation
Vcc3.3_host		3.3		V	Measured at Vcc3.3-Tx and Vcc3.3-Rx
Vcc3.3 set point accuracy	-5		+5	%	Measured at Vcc3.3-Tx and Vcc3.3-Rx. Note 1
Vcc3.3 Power supply noise including ripple			50	mVpp	1kHz to frequency of operation
Module Maximum Current Inrush			1.25	A	On any contact.
Module Current Ramp Rate			100	mA/uS	

1. 5%-accurate power needed for VCSEL laser drivers

2.5.3 POWER BUDGET CLASSES

Power levels associated with classifications of modules are shown in Table 4 on page 19. In general, the higher power classification levels are associated with higher data rates and longer reach, for a particularly technology family.

Table 4 Power Budget Classification

Power Class	Max Power (W)	Power Class	Max Power (W)
0	0.25 or less	1	1.0 or less
2	1.5 or less	3	2.5 or less
4	4.0 or less	5	6.0 or less
6	Higher than 6 Watts	7	Reserved

Power Class 0 supports a management-interface-only power level, for devices such as passive copper cables which require little or no signal power.

Power Classes 1 through 5 describe devices with between 0.25W and 6.0 Watts, with roughly a factor of 1.5 differentiating each power class.

Power Class 6 (higher than 6 Watts), is intended as a special high-power class, allowing higher-power devices and cables to operate with more than 6 Watts only after negotiation with a host that can support the cooling and power-delivery infrastructure to support such devices. As described in the Memory map, at Byte 44 in the Tx lower page and Byte 148 in Upper Page 00h, a device may not draw more than 6 Watts unless actively allowed by a host system. The actual amount of power used by such a high-

power device or cable is described in the Read-only Byte 148 of Upper Page 00h.

The highest maximum power budget is determined by a current limit of 1.0 A for each power contact, and by the cooling capability provided by the system. Two contacts at each voltage level allow power supply of up to 6.6W of power at 3.3V, and 24W of power at 12V. Generally, cooling capability will limit the amount of power that a module may dissipate. The system designer is responsible for ensuring that the maximum temperature does not exceed the case temperature requirements.

2.6 ESD

The module high speed signal contacts shall withstand 1000 V electrostatic discharge using the Human Body Model module and all other contacts shall withstand 2000 V electrostatic discharge using the Human Body Model, per JEDEC Standard JESD22-A114B (March 2006), and 500 V using the charged device model, per JEDEC Standard JESD22-C101C (Dec. 2004), without damage or non-recoverable error including but not limited to latchup. A recoverable error is one that does not require reset or replacement of the device.

The module shall meet ESD requirements given in EN 61000-4-2, criterion B test specification such that when installed in a properly grounded housing and chassis the units are subjected to 15KV air discharges during operation and 8KV direct contact discharges to the case.

2.7 HOT INSERTION AND REMOVAL

CXP modules shall not be damaged by removal or insertion. Removal may occur while the link is operating without damage to either port or the link. Insertion or removal may occur with power on or power off.

CHAPTER 3: HIGH-SPEED ELECTRICAL SIGNALING

3.1 INTRODUCTION

This chapter describes the signaling that allows for InfiniBand link operation through CXP connector transmit and receive interfaces. The signaling specifications described here act as a supplement to *InfiniBand Architecture Specification, Volume 2*. For any signaling specifications not listed here, the specifications listed in *InfiniBand Architecture Specification, Volume 2*, Chapter 6: High Speed Electrical Signaling - 2.5, 5.0, & 10.0 Gb/s shall apply.

3.2 COMPLIANCE POINTS

Since the ASIC or Serdes pins are not accessible, signal levels and eye openings are described at the CXP connector contacts. All values are for an equivalent 100 Ω differential impedance load located at the test point. Correction or de-embedding must be performed to derive actual measure data, taking into account the configuration of the test setup. Nomenclature is shown in Figure 4 on page 23, consistent with *InfiniBand Architecture Specification, Volume 2*, Figure 34.

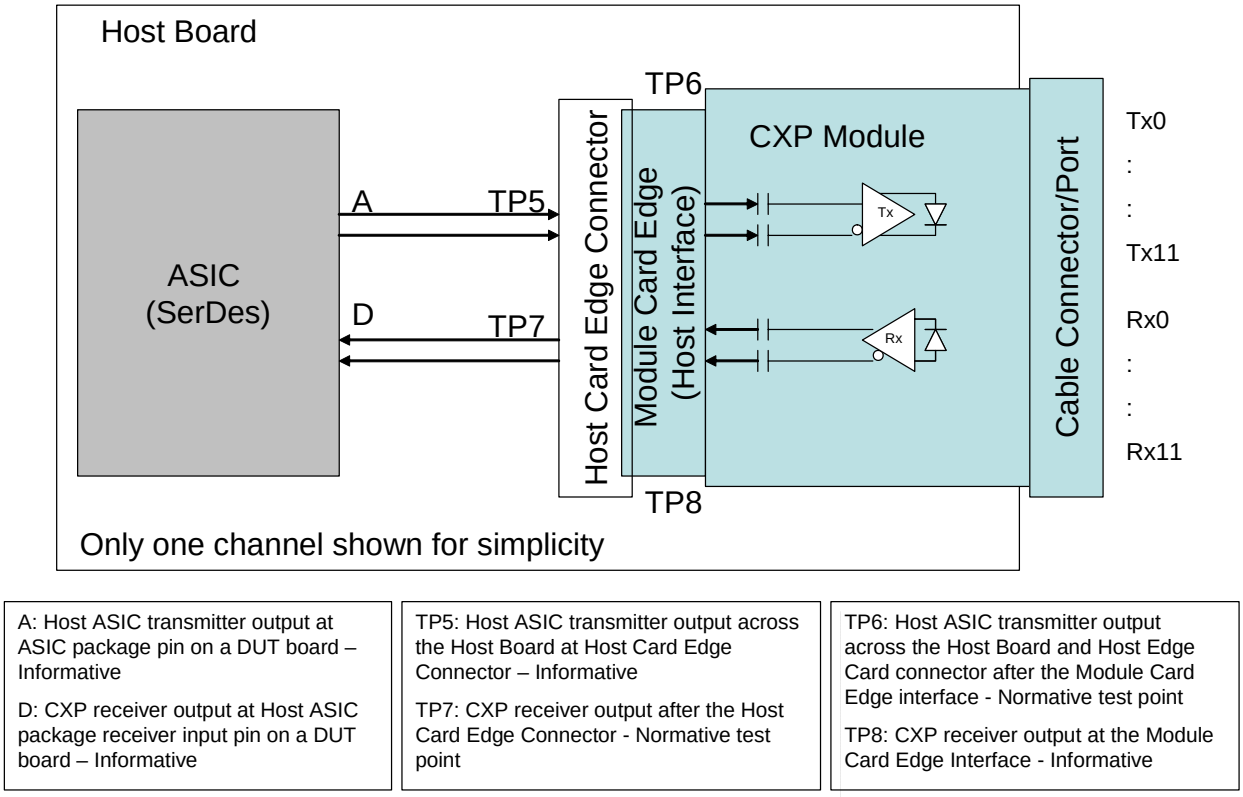


Figure 4 Application Reference Model and Compliance Points

3.3 LINEAR PASSIVE / LINEAR ACTIVE INTERFACE

For passive cables and for other types of modules that have linear transfer functions, interface requirements shall use transfer functions based on S-parameters as described in *InfiniBand Architecture Specification, Volume 2, Rel. 1.2.1,* except as modified here. In cases where there is conflict between values in Rel. 1.2.1 and this document, this one shall take precedence.

3.3.1 HOST DIFFERENTIAL DRIVER OUTPUTS

Differential Driver Output Characteristics for 10 Gb/s are as defined in *InfiniBand Architecture Specification, Volume 2*, Table 19.

3.3.2 COMPLIANT CHANNEL - MODULE TX INPUTS TO MODULE RX OUTPUTS

A compliant channel for QDR (10.0 Gb/s) signaling is defined in terms of frequency-dependent S Parameters for the path between signal pins at TP6 and TP8. Table 5, “Compliant Channel S Parameter Requirements for 10 Gb/s (QDR),” on page 24 describes the requirements for 10Gb/s

(QDR) bit rates. Requirements for operation at lower signaling rates are defined in *InfiniBand Architecture Specification, Volume 2*, Chapter 6: High Speed Electrical Signaling - 2.5, 5.0, & 10.0 Gb/s.

Table 5 Compliant Channel S Parameter Requirements for 10 Gb/s (QDR)[1]

Frequency	SDD11[2]	SDD21 (min.)
0.100 GHz	-10	-8.0
0.200 GHz	-10	-8.0
0.625 GHz	-10	-8.0
1.000 GHz	-10	-8.0
1.250 GHz	-9.8	-8.0
1.875 GHz	-9.3	-8.0
2.500 GHz	-8.8	-8.0
3.750 GHz	-8.1	-9.5
5.000 GHz	-6.8	-11.0
7.500 GHz	-4.5	-15
10.000 GHz	-2.9	-22

1. All values are measured in dB
2. Frequency dependent return loss derived from formula:
Frequency range 0.1 GHz - 1.0 GHz: SDD11(dB) = -10
Frequency range 1.0 GHz - 4.1 GHz: SDD11(dB) = -12+2*SQRT(f), f in GHz
Frequency range 4.1 GHz - 10.0 GHz: SDD11(dB) = -6.3+13*Log10(f/5.5), f in GHz

3.3.3 HOST DIFFERENTIAL RECEIVER INPUTS

Differential Receiver Input Characteristics for 10 Gb/s are as defined in *InfiniBand Architecture Specification, Volume 2*, Table 22.

3.4 LIMITING ACTIVE INTERFACE

For active transceivers and cables with limiting amplifiers, such as active copper cables, optical transceivers, and active optical cables, the electrical interface requirements are modified from the requirements described in *InfiniBand Architecture Specification, Volume 2*, Chapter 6, since these interfaces allow transmission with open eyes even to 10 Gb/s. For this interface, amplitude and jitter specifications on the eye diagram are used (similar to at 2.5 Gb/s rate).

Active modules have interface specifications similar to host ports, since an active CXP module's Tx electrical input is similar to a host receiver input, and an active CXP module's Rx electrical output is similar to a host driver.

3.4.1 HOST DIFFERENTIAL DRIVER OUTPUTS

Differential Driver output characteristics are as described in *InfiniBand Architecture Specification, Volume 2*, Table 19: Driver Characteristics for 10Gb/s, with the exceptions described in Table 6 below.

Table 6 Driver Characteristics for 10 Gb/s, for Limiting Active interfaces

Symbol	Parameter	Maximum	Minimum	Units	Notes
V_{diffc}	Differential output, (Note 1) TP6, Normative	1.2	0.5	V	Differential unsigned waveform amplitude into 100 ohm differential load. Replaces V_{diffc} row in *InfiniBand Architecture Specification, Volume 2*, Table 19, to tighten specifications for active limiting module interface
J_{D1}	Deterministic Jitter (Note 2) TP6, Normative	0.15		UI	Replaces J_{D1} row in *InfiniBand Architecture Specification, Volume 2*, Table 19, to remove requirement "Without pre-emphasis", i.e., to allow pre-emphasis by driver.
J_{T1}	Total Jitter (Note 2) TP6, Normative	0.30		UI	At +/- 7σ (10^{-12}) Replaces J_{T1} row in *InfiniBand Architecture Specification, Volume 2*, Table 19, to clarify bit error rate measurement requirement

1. Amplitude is measured for the first bit in a run.
2. Jitter is measured as defined in IBTA CIWG Test Specification

3.4.2 CXP MODULE TX INPUTS

A CXP Limiting Active module, shall be tolerant of input signals from the host port as described in *InfiniBand Architecture Specification, Volume 2*, Table 19: Driver Characteristics for 10Gb/s, with the exceptions described in Table 7 below.

Table 7 CXP Limiting Active Module Tx Input Characteristics for 10 Gb/s

Symbol	Parameter	Maximum	Minimum	Units	Notes
V_{diffc}	Differential input, (Note 1) TP6, Normative	1.2	0.5	V	Differential unsigned waveform amplitude into 100 ohm differential load. Replaces V_{diffc} row in *InfiniBand Architecture Specification, Volume 2*, Table 19, to tighten specifications for active limiting module interface.
J_{D1}	Deterministic Jitter (Note 2) TP6, Normative	0.15		UI	Replaces J_{D1} row in *InfiniBand Architecture Specification, Volume 2*, Table 19, to remove requirement "Without pre-emphasis", i.e., to allow pre-emphasis
J_{T1}	Total Jitter (Note 2) TP6, Normative	0.30		UI	At +/- 7σ (10^{-12}) Replaces J_{T1} row in *InfiniBand Architecture Specification, Volume 2*, Table 19, to clarify bit error rate measurement requirement
SDD11	Return Loss	By formula: See Note 3		dB	

1. Amplitude is measured for the first bit in a run.
2. Jitter is measured as defined in IBTA CIWG Test Specification.
3. Frequency dependent return loss derived from formula:
Frequency range 0.1 GHz - 1.0 GHz: SDD11(dB) = -10
Frequency range 1.0 GHz - 4.1 GHz: SDD11(dB) = -12+2*SQRT(f), f in GHz
Frequency range 4.1 GHz - 10.0 GHz: SDD11(dB) = -6.3+13*Log10(f/5.5), f in GHz

3.4.3 CXP MODULE RX OUTPUTS

The differential driver output characteristics of the Rx portion of a limiting active module are as described in *InfiniBand Architecture Specification, Volume 2*, Table 19: Driver Characteristics for 10Gb/s for a host port differential driver, with the exceptions described in Table 8 below.

Table 8 CXP Limiting Active Module Rx Output Characteristics for 10 Gb/s

Symbol	Parameter	Maximum	Minimum	Units	Notes
V_{diffc}	Differential output, (Note 1) TP8, Normative	1.2	0.2	V	Differential unsigned waveform amplitude into 100 ohm differential load.
J_{D1}	Deterministic Jitter (Note 2) TP7, Normative	0.40		UI	
J_{T1}	Total Jitter (Note 2) TP7, Normative	0.72		UI	At +/- 7σ (10^{-12})

1. Amplitude is measured for the first bit in a run if a Backplane port, for all bits of a Cable Port.
2. Jitter is measured as defined in IBTA CIWG Test Specification.

3.4.4 HOST DIFFERENTIAL RECEIVER INPUTS

Differential Receiver input characteristics are as described in *InfiniBand Architecture Specification, Volume 2*, Table 22: Receiver Characteristics for 10Gb/s, with the exceptions described in Table 9 below.

Table 9 Receiver Characteristics for 10 Gb/s

Symbol	Parameter	Maximum	Minimum	Units	Notes
J_{D1}	Deterministic Jitter (Note 1) TP7, Normative	0.40		UI	Replaces t_{REye1} row in *InfiniBand Architecture Specification, Volume 2*, Table 19, to clarify that limiting active interface will have an open eye at receiver at 10 Gb/s
J_{T1}	Total Jitter (Note 2) TP7, Normative	0.72		UI	Replaces t_{REye1} row in *InfiniBand Architecture Specification, Volume 2*, Table 19, to clarify that limiting active interface will have an open eye at receiver at 10 Gb/s
SDD11	Return Loss	By formula: See Note 2		dB	Replaces S_{DD11} row in *InfiniBand Architecture Specification, Volume 2*, Table 19, to tighten return loss specifications for active limiting module interface

1. Jitter is measured as defined in IBTA CIWG Test Specification.
2. Frequency dependent return loss derived from formula:
Frequency range 0.1 GHz - 1.0 GHz: SDD11(dB) = -10
Frequency range 1.0 GHz - 4.1 GHz: SDD11(dB) = -12+2*SQRT(f), f in GHz
Frequency range 4.1 GHz - 10.0 GHz: SDD11(dB) = -6.3+13*Log10(f/5.5), f in GHz

CHAPTER 4: MECHANICAL AND BOARD DEFINITION

4.1 INTRODUCTION

The overall transceiver CXP module defined in this document is illustrated in Figure 5 on page 28. The connector, receptacle, and receptacle housing dimensions described in this chapter, and the heat sink and heat sink clip dimensions described in Chapter 5: Environmental and Thermal Specifications are constant for all applications, to ensure intermateability and interchangeability between component parts. Dimensions not specifically called out may be modified, subject to intermateability and interchangeability constraints of the individual application.

The connector and housing assembly are designed to support copper cables with both active and passive data transmission, optical transceiver modules, and active optical cable assemblies. Other transmission technologies may defined in a vendor-specific manner, as long as the connector and receptacle interfaces are preserved.

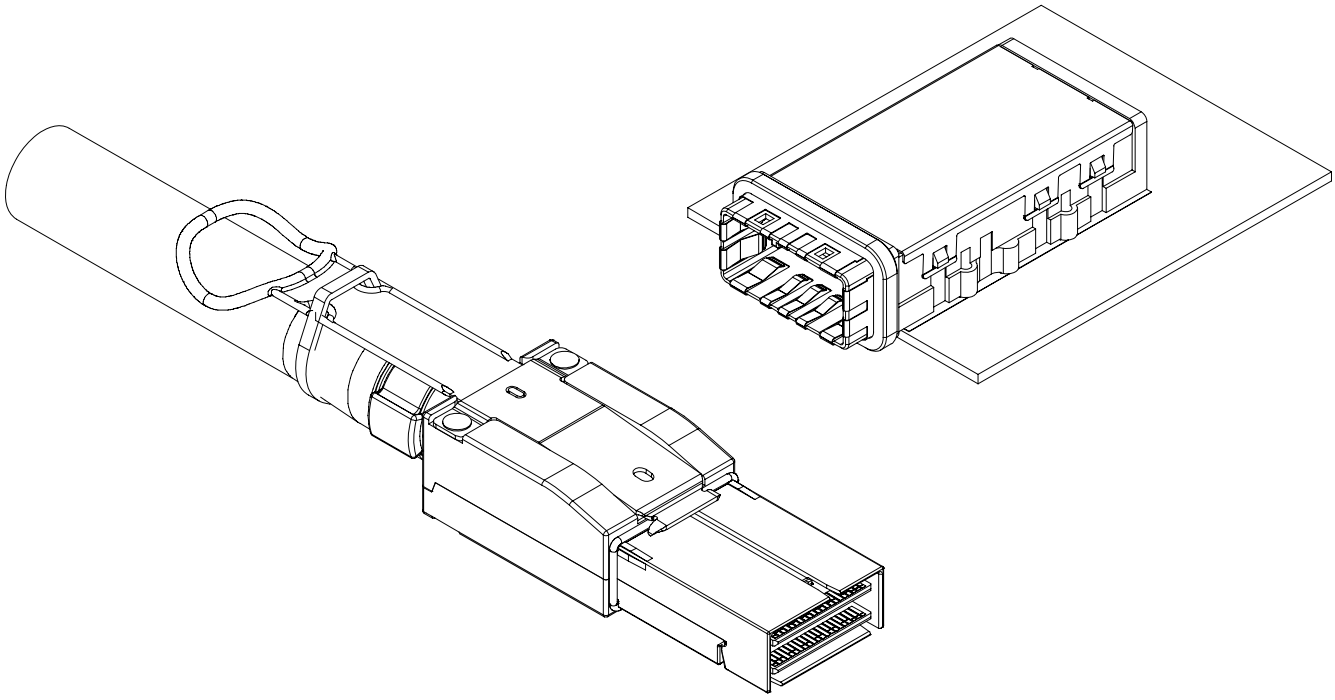


Figure 5 General view, CXP Cable Connector & Housing Assembly, w/o heat sink

4.2 CXP DATUMS AND COMPONENT ALIGNMENT

A listing of the datums for the various components is contained in Table 10 on page 29. The alignments of some of the datums are noted. All dimensions are in millimeters.

Table 10 Definition of Datums

Datum	Description	Where Shown
A	Width of Paddle Card	Figure 9
B	Top Surface of Paddle Card	Figure 9
C	Leading Edge of Short Signal Pads on Paddle Card	Figure 9
D	Width of Plug Snout	Figure 7
E	Body of Plug	Figure 6
F	Front Edge of Receptacle Snout (does not include EMI fingers)	Figure 6, Figure 10
G	Centerline of First Row of Connector Compliant Contacts	Figure 6, Figure 10
H	Centerline of Receptacle Contacts	Figure 6, Figure 10
I	not used	
J	Centerline of outer contacts in Row A PCB holes	Figure 13
K	Line along Row A of PCB holes	Figure 13, Figure 14
L	Surface of PCB	Figure 13
M	Width of Receptacle Snout Opening	Figure 10
N	Bottom Surface of Receptacle Housing	Figure 10
P	Bottom Surface of Plug Snout	Figure 7
X, Y	Reference 0,0 on Host Board - (application-specific)	Figure 13

The relationship of the transceiver/connector and receptacle housing relative to the host board and bezel is illustrated in Figure 6 on page 30 and in Figure 9 on page 33 by the location of the key datums of each of the components.

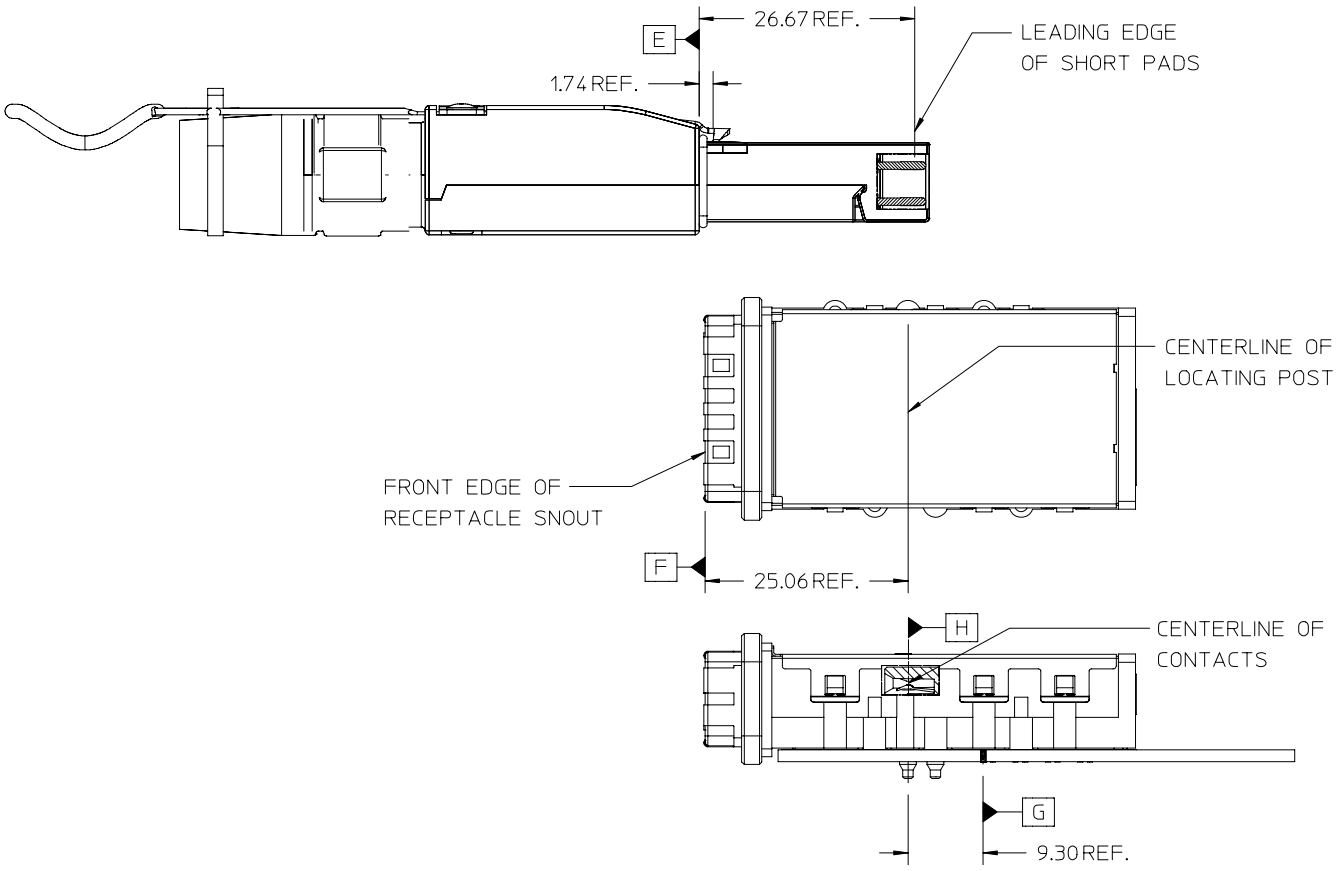


Figure 6 Cable Connector and Receptacle Housing Datums

4.3 CXP MODULE PACKAGE DIMENSIONS

A common mechanical outline is used for all CXP devices. The package drawing and dimensions for the CXP connector plug are defined in Figure 7 on page 31 and Figure 8 on page 32. Figure 9 on page 33 shows the dimensions of the paddle card and contacts inside the connector plug.

Package drawings and dimensions for the receptacle housing are shown in Figure 10 on page 34 and Figure 11 on page 35. Note that some dimensions of the receptacle housing relate specifically to the heat sink clip attachment, and are shown separately in Figure 19 on page 47.

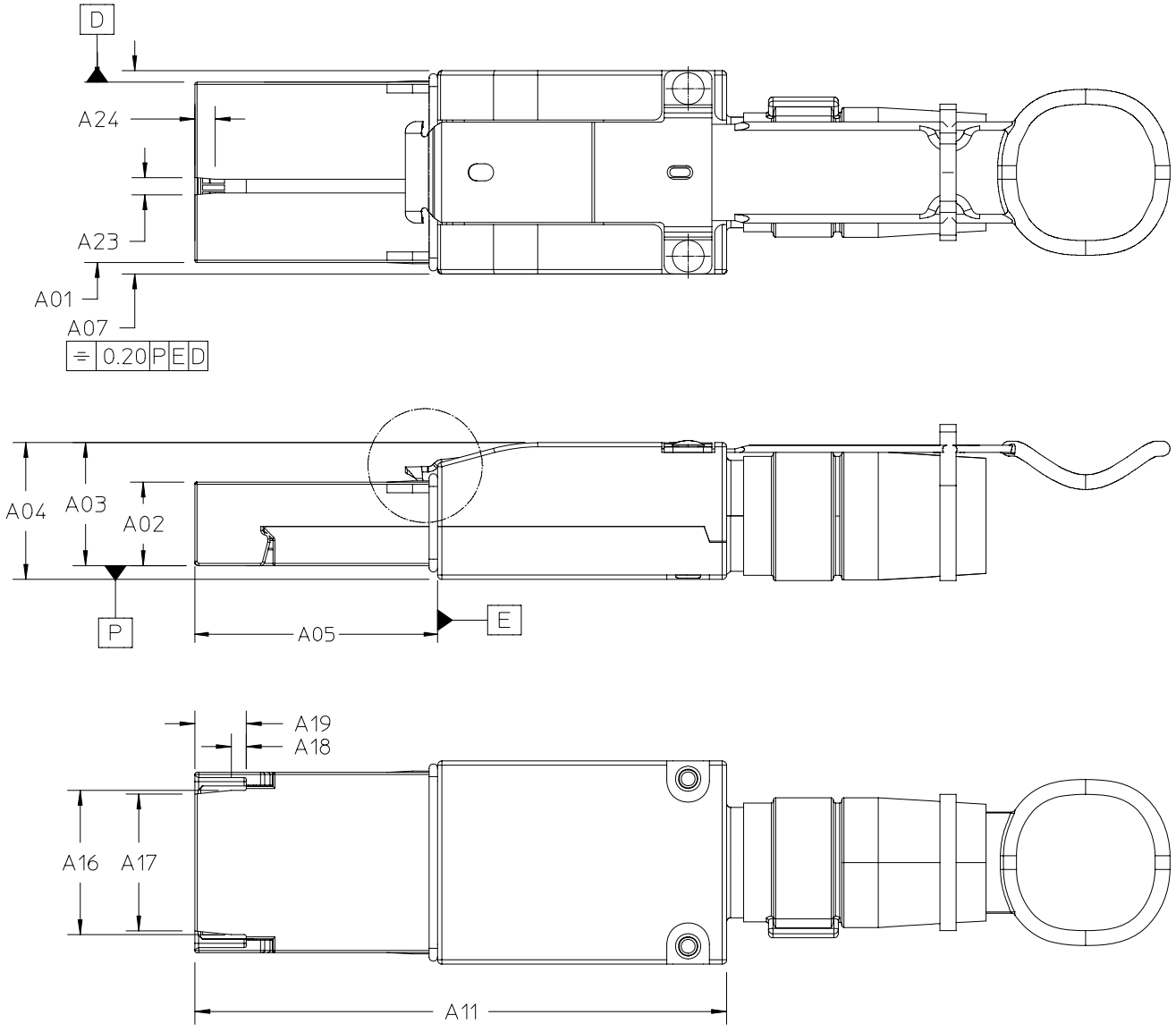
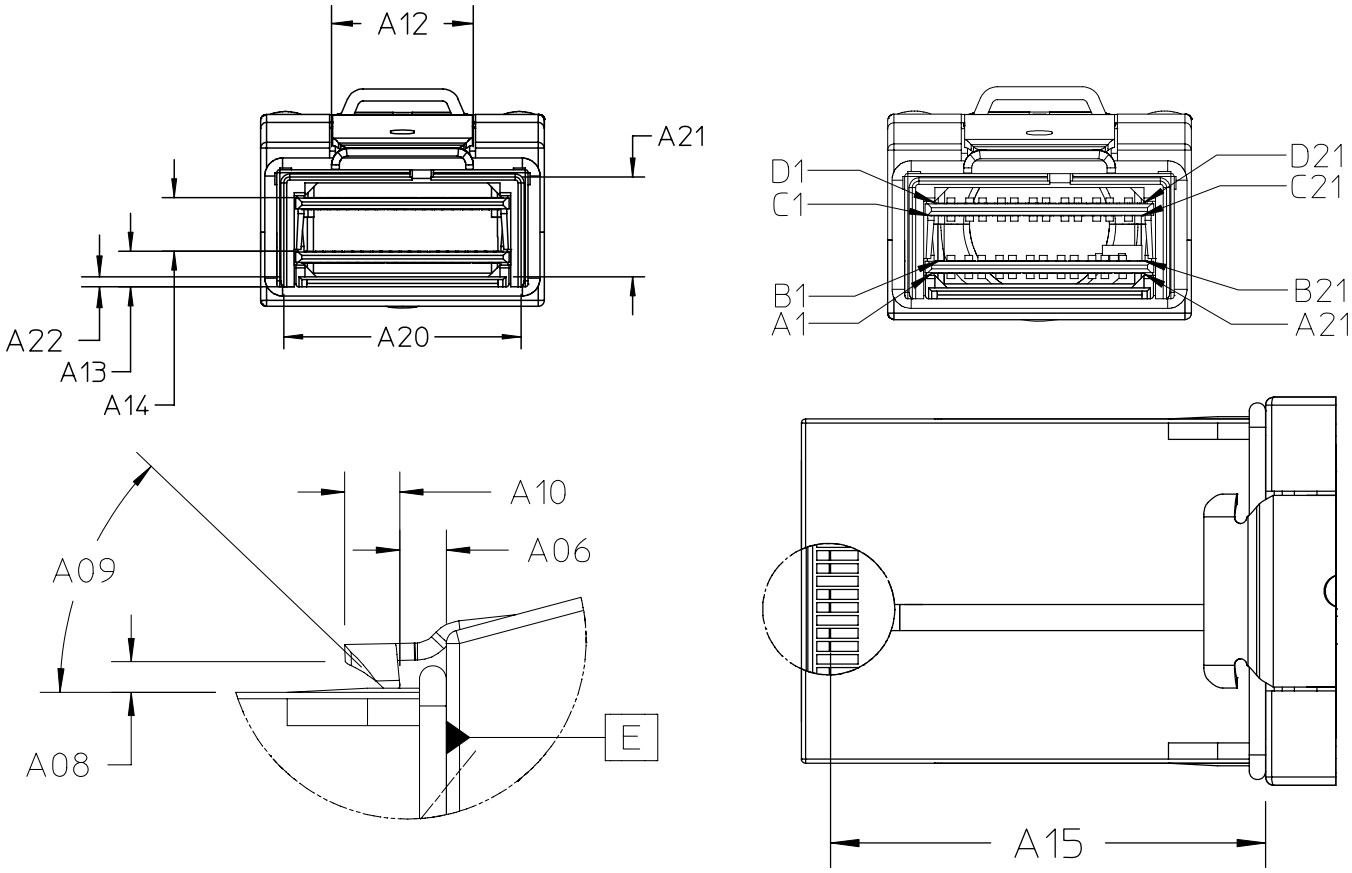
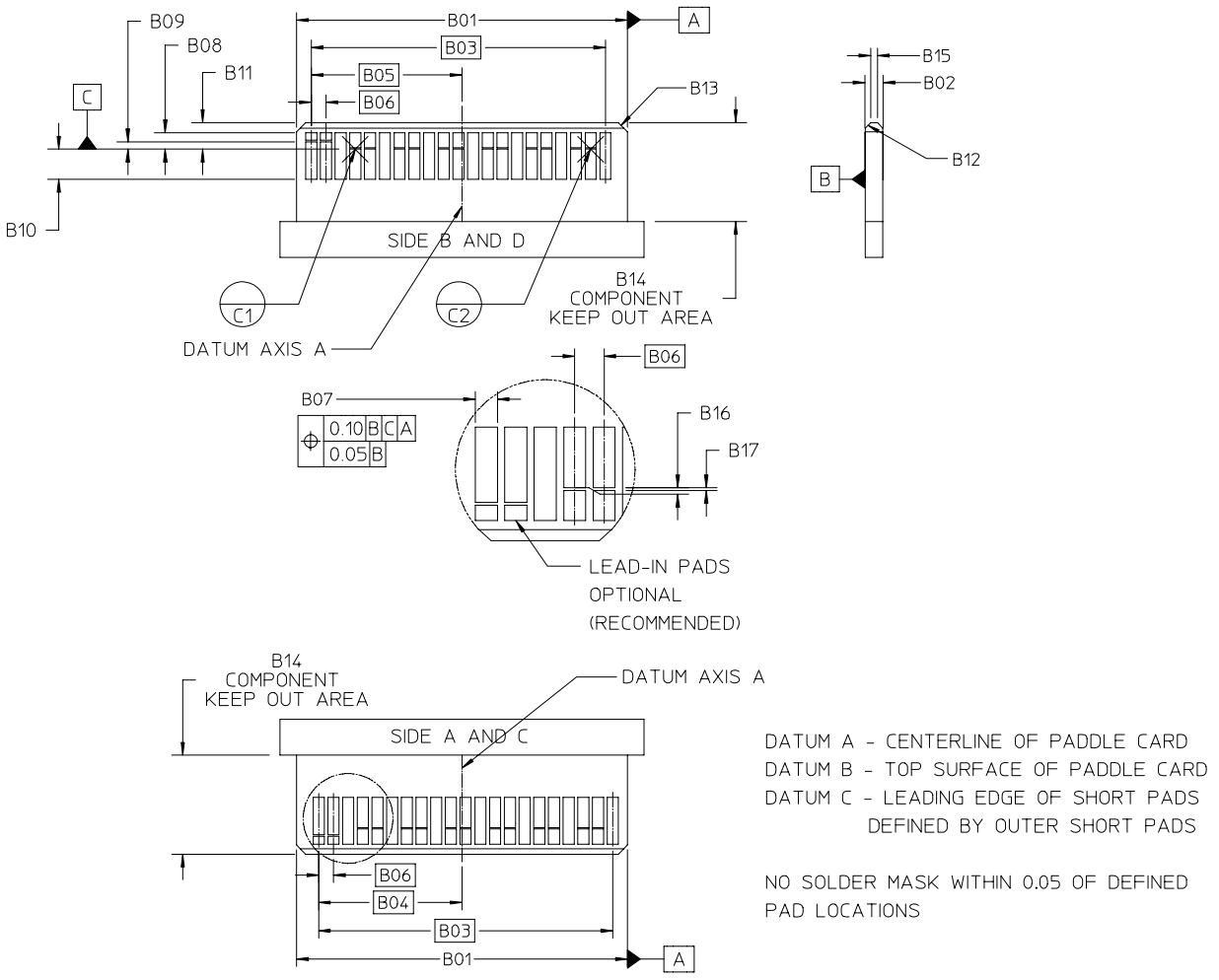


Figure 7 Shielded Free (Plug) Integrated Cable Connector



	Description	Dim.	Tol.		Description	Dim.	Tol.
A01	Snout Width	21.20	0.13	A13	Base of snout to top of 1st paddle card	2.99	0.20
A02	Snout Thickness	9.81	0.13	A14	Top of 1st to top of 2nd card	4.50	0.10
A03	Snout Bottom to Plug Top	14.60	Max	A15	Plug Body (Datum E) to short pad (Datum C)	26.67	0.20
A04	Plug Body Thickness	16.21	Max	A16	Tongue Width - Base	16.95	0.10
A05	Snout Length	28.45	0.13	A17	Tongue Width - Tip	16.10	0.20
A06	Plug Body (Datum E) to Latch	1.74	0.13	A18	Length of Tongue - Straight Section	1.80	0.10
A07	Body Width	24.05	Max	A19	Length of Tongue	6.00	Min.
A08	Barb Lead-in Height	1.14	0.10	A20	Inside Width of Snout	20.00	0.05
A09	Barb Lead-in Angle	45º	1º	A21	Inside Height of Snout	8.60	0.25
A10	Barb Length	2.05	0.10	A22	Tongue Thickness	0.60	Ref.
A11	Plug Overall Body Length	62.00	Ref	A23	Orientation Key Lead-In Width	2.00	0.25
A12	Latch Width	11.90	0.10	A24	Orientation Key Lead-in Length	2.40	0.25

Figure 8 Shielded Free (Plug) Integrated Cable Connector, cont'd



	Description	Dim.	Tol.		Description	Dim.	Tol.
B01	Paddle Card Width	18.00	0.10	B10	Pad Length	1.55	Min.
B02	Paddle Card Thickness	1.00	0.10	B11	Card Edge to Second Pad	1.45	0.10
:B03	Overall Pad Centers	16.00	Basic	B12	Lead-in Chamfer x 45º	0.30	0.05
B04	Card Center to outer Pad, Side A and Side C	7.80	Basic	B13	Lead-in Chamfer x 45º	0.50	0.05
B05	Card Center to outer Pad, Side B and Side D	8.20	Basic	B14	Component Keep Out Area	5.40	Min.
B06	Pad Center to Center (Pitch)	0.80	Basic	B15	Lead-in Flat	0.36	Ref
B07	Pad Width	0.60	0.03	B16	Short Pad to Datum C	0.00	0.03
B08	Front Pad Length	0.90	0.05	B17	Pad to Lead-in Pad	0.08	0.015
B09	Front Pad Spacing	0.40	0.05				

Figure 9 Paddle Card Dimensions and Definition of Datums

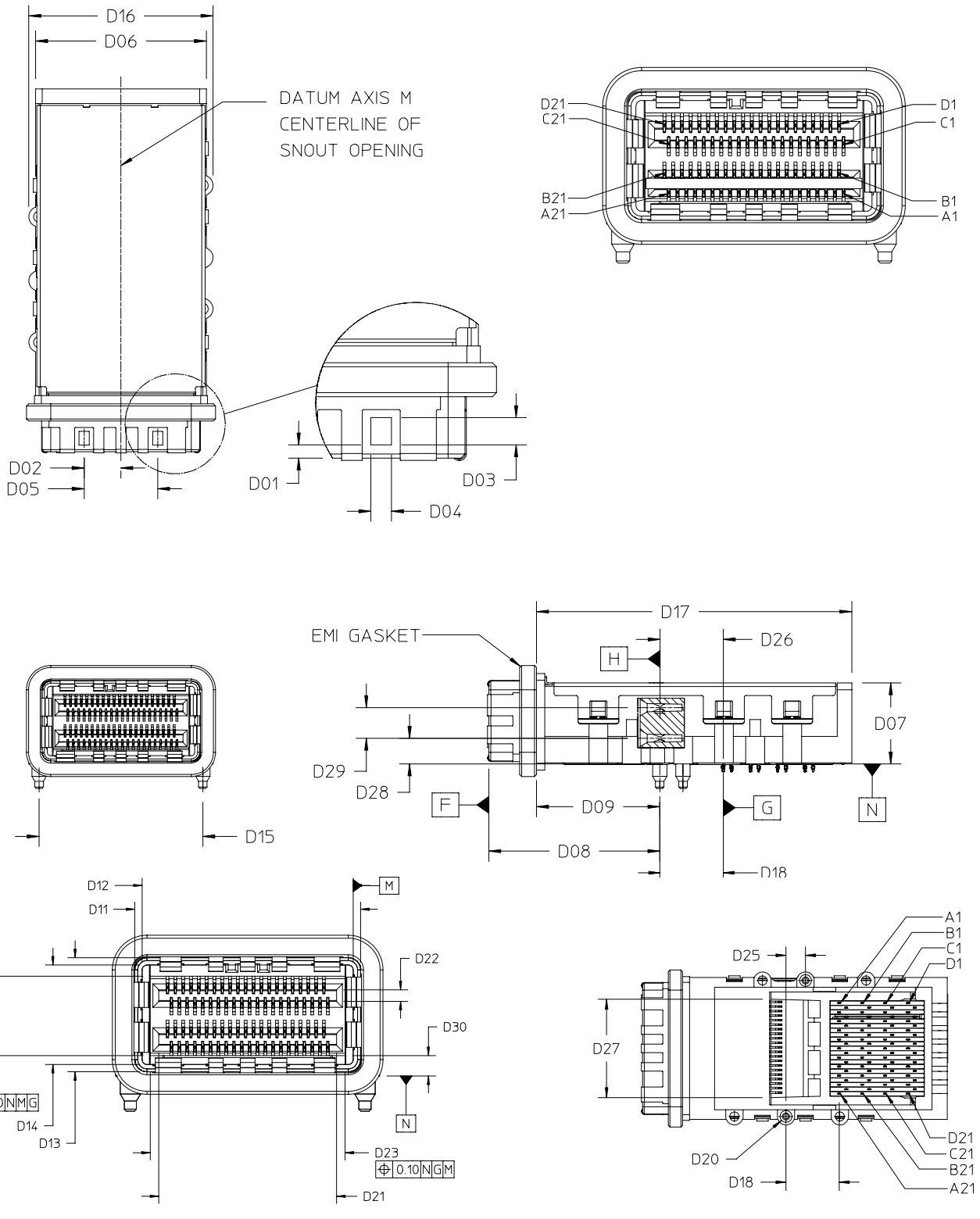


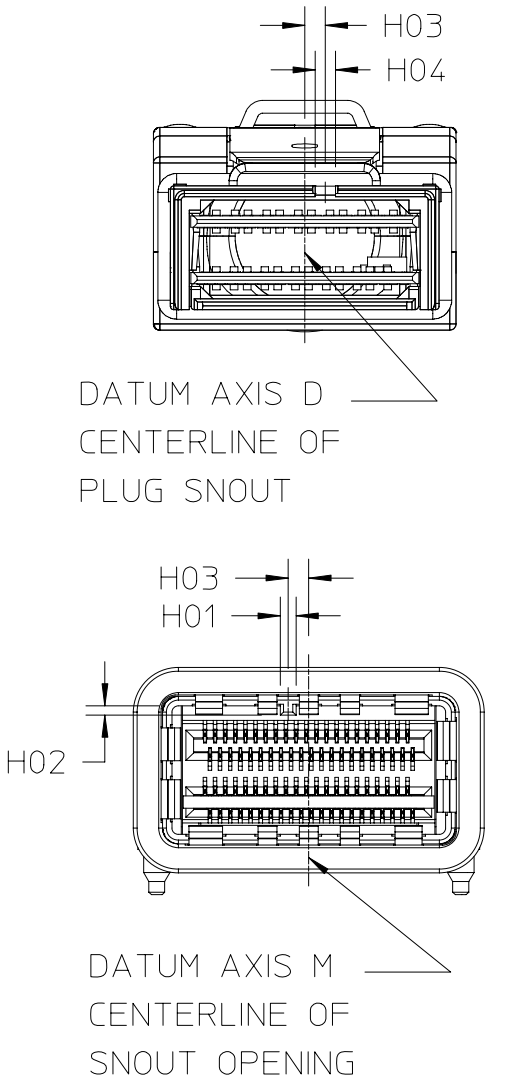
Figure 10 Fixed (Receptacle) Connector

	Description	Dim.	Tol.		Description	Dim.	Tol.
D01	Latch Hole from Face	0.97	0.05	D16	Shell Width at screw attach features	27.00	0.25
D02	Latch Hole from Datum M	5.40	0.10	D17	EMI Shell Base to Back	46.22	0.25
D03	Latch Hole Length	2.00	0.10	D18	Connector Contacts to Locating Post	9.30	0.05
D04	Latch Hole Width	1.50	0.10	D19	Not used		
D05	Latch Hole to Hole	10.80	0.05	D20	Peg Diameter	2.08	0.05
D06	Shell Width	25.05	0.25	D21	Card Slot Width	18.20	0.05
D07	Shell Height	11.88	0.13	D22	Card Slot Height	1.20	0.05
D08	Locating Post to Face	25.06	0.08	D23	Receptacle Body Width	19.89	0.08
D09	Locating Post to EMI Shell Base	18.06	0.13	D24	Receptacle Body Height	8.15	0.08
D10	Not used	-	~	D25	Peg Centerline to Peg Centerline	3.41	0.05
D11	Snout Width	23.10	0.08	D26	Contact Centerline to 1st Row of Compliant Pins	9.25	0.15
D12	Snout Opening Width	21.60	0.05	D27	Housing, Leg to Leg	17.35	0.05
D13	Snout Height	11.70	0.08	D28	PCB to Lower Card Slot Centerline	3.75	0.10
D14	Snout Opening Height	10.20	0.05	D29	Lower Card Slot to Upper Card Slot Centerline	4.50	0.10
D15	Peg Centerline to Peg Centerline	24.00	0.08	D30	Datum N to Bottom of Receptacle Housing	2.10	0.10

Figure 11 Dimensions for Fixed (Receptacle) Connector in Figure 10

4.4 CONNECTOR ORIENTATION KEY

Drawings and dimensions of an orientation key are shown in Figure 12 on page 36. This key assures that the plug is inserted into the receptacle with the correct side up.

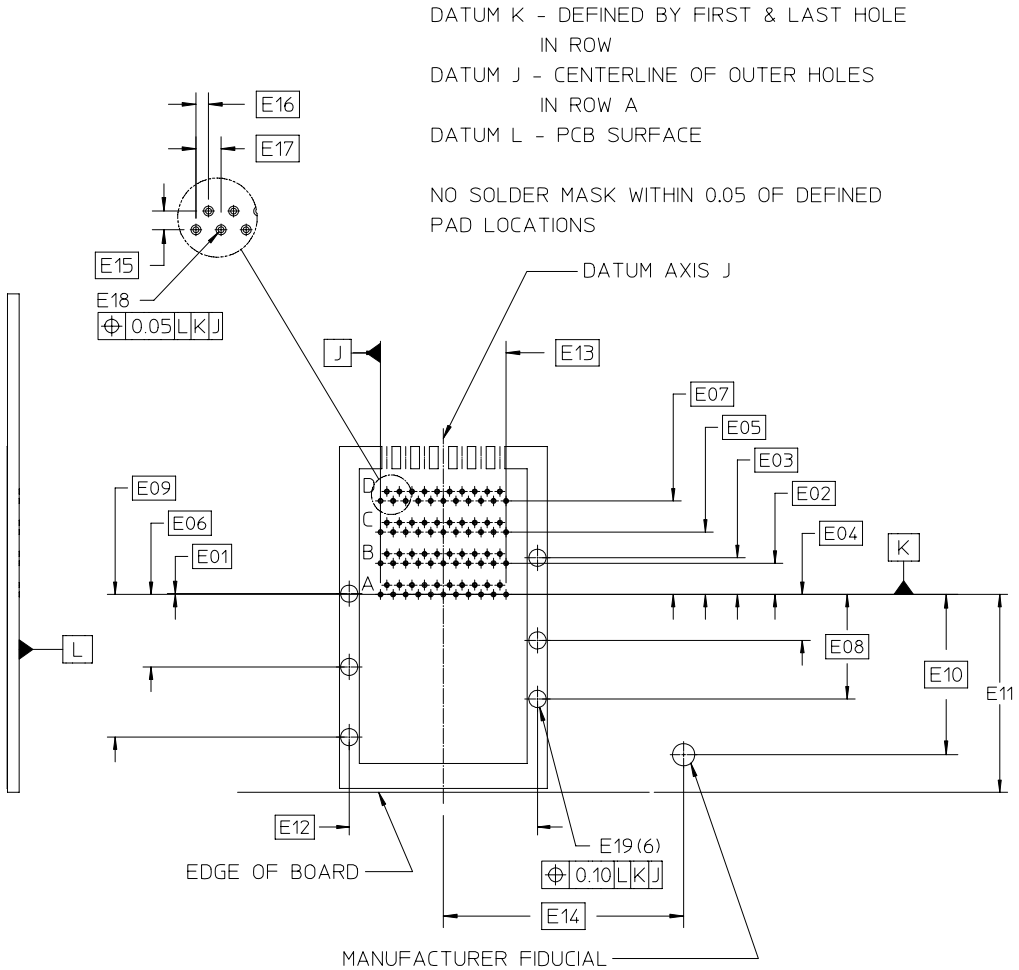


	Description	Dim.	Tol.
H01	Orientation Key Width	1.25	0.13
H02	Orientation Key Height	0.75	0.13
H03	Orientation Key Location	1.625	0.13
H04	Orientation Key Slot	1.60	0.13

Figure 12 Connector Key

4.5 HOST PCB FOOTPRINT

A typical host board mechanical footprint for attaching the CXP Connector and Receptacle system is shown in Figure 13 on page 37. The location on the host board is application specific.



	Description	Dim.			Description	Dim.	
E01	Shield Screw Hole to Datum K	0.10	Basic	E11	Connector Datum to Card Edge	25.38	0.25
E02	Row A (Datum K) to Row B	4.00	Basic	E12	Shield Mounting Hole to Mounting Hole	24.00	Basic
E03	Shield Screw Hole to Datum K	4.70	Basic	E13	Shield Pin Center to Center	16.00	Basic
E04	Shield Screw Hole to Datum K	5.89	Basic	E14	Connector Datum to Manufacturer Fiducial	Basic	N/A
E05	Row A (Datum K) to Row C	8.00	Basic	E15	Within Row pitch - Front to Back	1.20	Basic
E06	Shield Screw Hole to Datum K	9.30	Basic	E16	Within Row Horizontal Offset	0.80	Basic
E07	Row A (Datum K) to Row D	12.00	Basic	E17	Within Row pitch - Horizontal	1.60	Basic
E08	Shield Screw Hole to Datum K	13.40	Basic	E18	Contact Hole Finished Diameter	0.37	0.05
E09	Shield Screw Hole to Datum K	18.30	Basic	E19	Shield Mounting Hole Diameter	2.20	0.05
E10	Connector Datum to Manufacturer Fiducial	Basic	N/A				

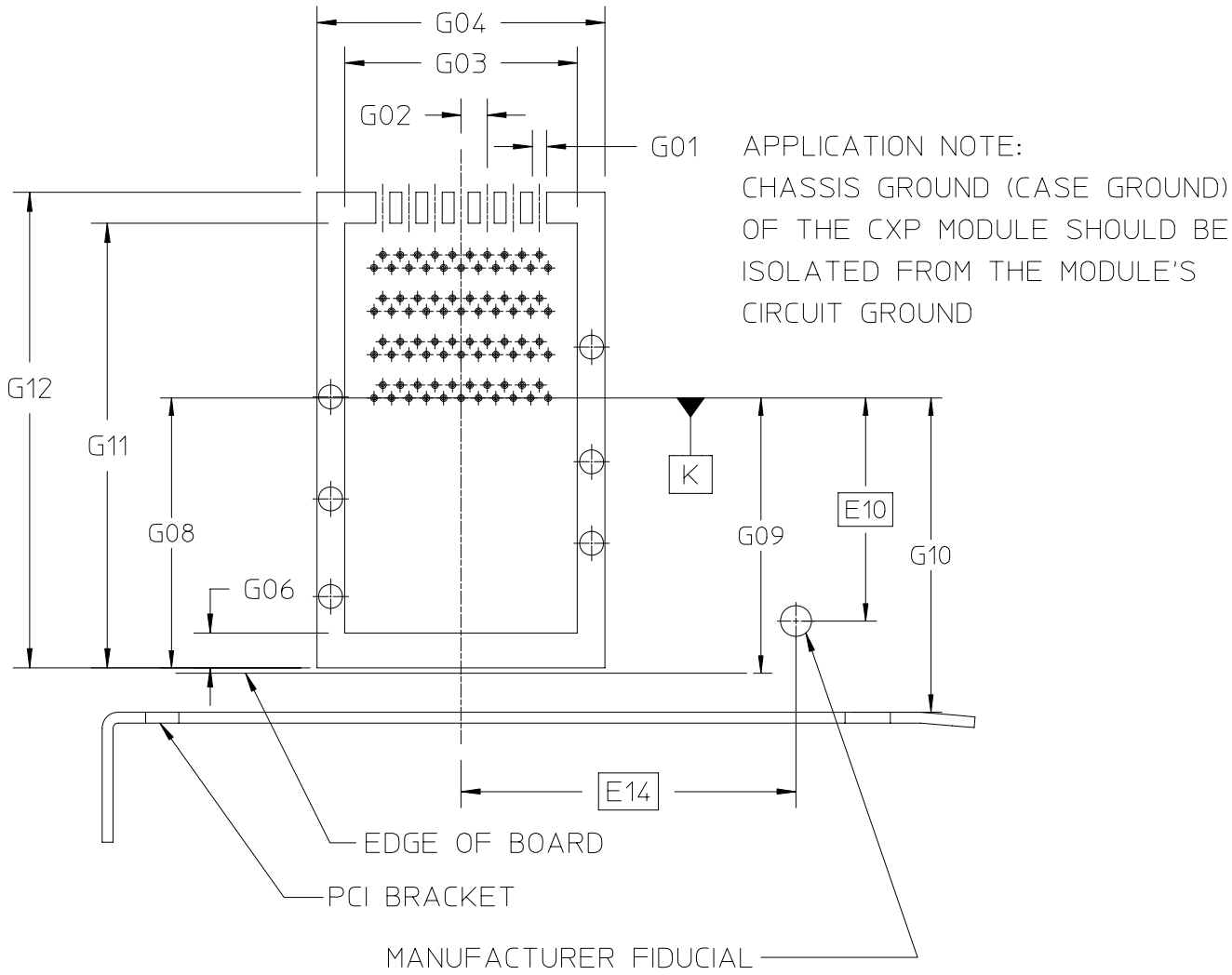
Figure 13 Footprint - Shown in example application, Low Profile PCIe card

4.5.1 GROUNDING PAD STRUCTURE

Structure of the ground pads connected to chassis ground are shown in Figure 14 on page 39.

4.5.2 MATING OF CXP MODULE & HOST PCBS TO CXP ELECTRICAL CONNECTORS

The cards and other components inside the CXP modules will require careful design to support 10Gb/s signaling on (12+12) differential pairs. Similarly, high-speed traces in host PCBs must be carefully designed to minimize impedance discontinuities and reduce losses to acceptable levels. These designs are outside the bounds of this specification.

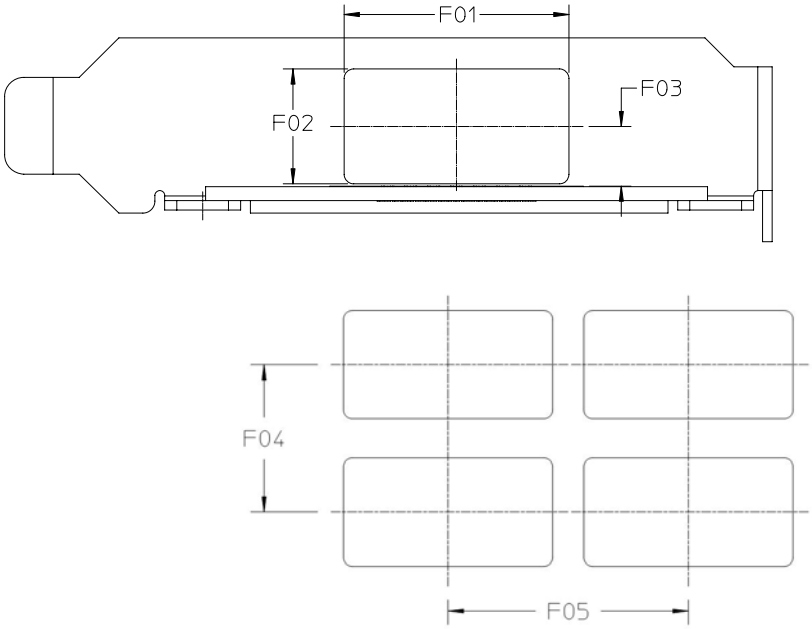


	Description	Dim.	Tol.		Description	Dim.	Tol.
G01	Ground Pad Alley Width	1.30	0.10	G07	Connector Datum to Manufacturer Fiducial	Basic	N/A
G02	Ground Pad Alley Spacing	2.40	0.10	G08	Connector Datum to Front Pad Edge	24.88	0.10
G03	Ground Pad Inner Width	21.40	0.10	G09	Connector Datum to Card Edge	25.38	Ref
G04	Ground Pad Width	26.49	0.10	G10	Connector Datum to Bezel	28.96	0.25
G05	Pad Center to Manufacturer Fiducial	Basic	N/A	G11	Ground Pad Edge to Inside Pad Edge	40.99	0.10
G06	Ground Pad Width	3.21	0.10	G12	Ground Pad Length	43.84	0.10

Figure 14 Ground Pad - Shown in example application, Low Profile PCIe card

4.6 BEZEL FOR SYSTEMS USING CXP TRANSCEIVERS

Host enclosures that use CXP devices should provide appropriate clearances between the CXP transceivers to allow insertion and extraction without the use of special tools and a bezel enclosure with sufficient mechanical strength. See Figure 15 on page 40 for the recommended bezel design for a single CXP device, and for spacing of individual receptacles.



	Description	Dim.	Tol.
F01	Cutout Length	23.50	0.05
F02	Cutout Height	12.10	0.05
F03	Cutout Location from PCB Surface	6.29	0.05

	Description	Dim.	Tol.
F04	Vertical Pitch	16.50	Min
F05	Horizontal Pitch (individual receptacles)	27.00	Min

Figure 15 Panel Cutout - Shown in example application, Low Profile PCIe card

The front surface of the receptacle housing may pass through the bezel. If EMI spring fingers are used, they shall make contact to the inside of the bezel cutout. If an EMI gasket is used, it shall make contact to the inside surface of the bezel or to the inside of the bezel cutout. To accept all housing designs, both bezel surfaces must be conductive and connected to chassis ground.

The CXP transceiver insertion slot should be clear of nearby moldings and covers that might block convenient access to the latching mechanisms, the CXP transceiver, or the cables connected to the CXP transceiver.

CHAPTER 5: ENVIRONMENTAL AND THERMAL SPECIFICATIONS

5.1 PHYSICAL AND MECHANICAL PERFORMANCE REQUIREMENTS

The requirement for insertion forces, extraction forces and retention forces are specified in Table 11 on page 41. The CXP receptacle housing and module design combinations must ensure that excessive force applied to a cable does not damage the CXP receptacle, housing, or host connector. If any part is damaged by excessive force, it should be the cable or module, and not the receptacle or receptacle housing, which are part of the host system.

Table 11 Module & Receptacle Connector Physical Requirements

Symbol	Parameter	Min	Max	Unit	Comments
F_i	CXP module insertion force		150	N	EIA 364-13
F_w	CXP module extraction		50	N	EIA 364-13
F_r	CXP module retention	90	170	N	Load pull, per EIA 364-38A No damage to transceiver below 90N
F_{rcl}	Cage retention (latch strength)	180		N	No damage to latch below 180N
F_{rhb}	Cage retention in host board	114		N	Force to be applied in a vertical direction, no damage to cage
N_{hc}	Insertion / removal cycles, connector/receptacle	100		Cycles	Number of cycles for the connector and receptacle with multiple transceivers
N_x	Insertion / removal cycles, CXP module	50		Cycles	Number of cycles for an individual module

It is also recommended that the connector interfaces meet the parameters defined in Table 12 on page 41

Table 12 Recommended Connector Physical Parameters

Symbol	Parameter	Min	Max	Unit	Comments
t_{pm}	Contact finish	0.76 Au over 1.27 Nickel		μm	As necessary to meet N_x requirements
F_n	Contact normal force	50		cN	per contact
S_{hcc}	Contact Hertz stress	170		kpsi	per contact
D_{wc}	Contact wipe length	0.75		mm	

It is recommended that all components and attach processes used for those components be compliant with RoHS directive 2002/95/EC issued January 27, 2003.

5.2 CONNECTOR ELECTRICAL PERFORMANCE REQUIREMENTS

The CXP module and Receptacle shall comply to the electrical specifications described in Table 13 on page 42.

Table 13 Module & Receptacle Connector Electrical Performance Requirements

Symbol	Parameter	Min	Max	Unit	Comments
LLCR	Low level contact resistance - initial		80	mΩ	through testing per EIA 364-23, measured across interface between paddle card trace and receptacle
ΔLLCR	Low level contact resistance - change		20	mΩ	through testing per EIA 364-23, as a result of any test group setup
I_{max}	Current rating, all contacts simultaneously	0.5		A	per EIA-364-70 or IEC 512-5-1 Test 5a, at 30°C temperature rise above ambient
$I_{max,s}$	Current rating, single contact	1		A	per EIA-364-70 or IEC 512-5-1 Test 5a, at 30°C temperature rise above ambient
R_{Iso}	Insulation Resistance	1000		MΩ	100 Vdc, between adjacent contacts
V_{Iso}	Dielectric Withstanding Voltage	300		Vdc	No defect or breakdown between adjacent contacts, 300 Vdc minimum for 1 minute
Z_{dco}(peak)	Differential Impedance - peak (connector area)	90	110	Ω	EIA 364-108 Rise time: 50ps (20-80%)
Z_{dco}(nom)	Differential Impedance (nominal)	95	105	Ω	Includes connector cable to connector interface and board termination pads and vias.
S_{cop}	Within-Pair Skew		5	ps	maximum (by design), measured at interface between paddle cards & receptacle. EIA 364-103
$NEXT_c$	Near End Crosstalk Isolation		-34	dB	EIA 364-90, 50 MHz to 10 GHz. Equivalent to 2% voltage crosstalk, power sum
L_{co}	Insertion Loss		1.0	dB	EIA 364-101, 50 MHz to 5 GHz

5.3 MECHANICAL AND ENVIRONMENTAL REQUIREMENTS

The CXP module and receptacle shall comply to the mechanical and environmental specifications described in Table 14 on page 43. Connectors shall meet or exceed the environmental performance requirements of EIA-

364.1000.01, including exposure to Mixed Flowing Gas consistent with the required product life

Table 14 Module and Receptacle Mechanical and Environmental Requirements

Parameter	Specification	Test Condition
Vibration	No damage No discontinuity longer than 1 μsec allowed. 20 mOhms maximum change from initial (baseline) contact resistance	EIA 364-28
Mechanical Shock	No damage 20 mOhms maximum change from initial (baseline) contact resistance	EIA 364-27
Thermal Shock	No Damage 20 mOhms maximum change from initial (baseline) contact resistance	EIA 364-32C, Condition 1 -55°C to +85°C
Temperature Life	No Damage 20 mOhms maximum change from initial (baseline) contact resistance	EIA 364-17, Method A Test Condition 2, Test Time Condition C Subject mated specimens to 70°C for 500 hours
Humidity-Temperature Cycling	No Damage 20 mOhms maximum change from initial (baseline) contact resistance	EIA 364-31, Method III Subject unmated specimens to 10 cycles (10 days) between 25°C and 65° at 80-100% RH
Mixed Flowing Gas	No Damage 20 mOhms maximum change from initial (baseline) contact resistance	EIA 364-65, Class 2A Subject specimens to environments Class 2A, 7 days unmated and 7 days mated
Thermal Disturbance	No Damage 20 mOhms maximum change from initial (baseline) contact resistance	EIA 364-32 Cycle the connector between 15±3°C and 85±3°C as measured on part. Temperature ramps should be a minimum of 2°C per minute and dwell times should ensure that the contacts reach the temperture extremes (a minimum of 5 minutes). Humidity is not controlled. Perform 10 such cycles.

5.4 THERMAL PERFORMANCE RANGES

The CXP module shall operate within one or more of the case temperatures ranges defined in Table 15 on page 44. The temperature ranges are applicable between 60 m below sea level and 1800 m above sea level, (Ref. NEBS GR-63) utilizing the host system's designed airflow. CXP is designed to allow for up to 16 adjacent transceivers in a 19-inch rack-

mount design using individual or ganged receptacles, with the appropriate thermal design for cooling / airflow. (Ref. NEBS GR-63).

Table 15 Temperature Classification of Module Case

Class	Case Temperature Range During Operation
Standard	0 through 70C
Extended	-5 through 85C
Industrial	-40 through 85C

5.5 CXP HOUSING ASSEMBLY THERMAL INTERFACES

Cooling requirements will be dependent on device technology. For devices or cables that require cooling inside the host, a receptacle housing with riding heat sink is shown in Figure 16 on page 44.

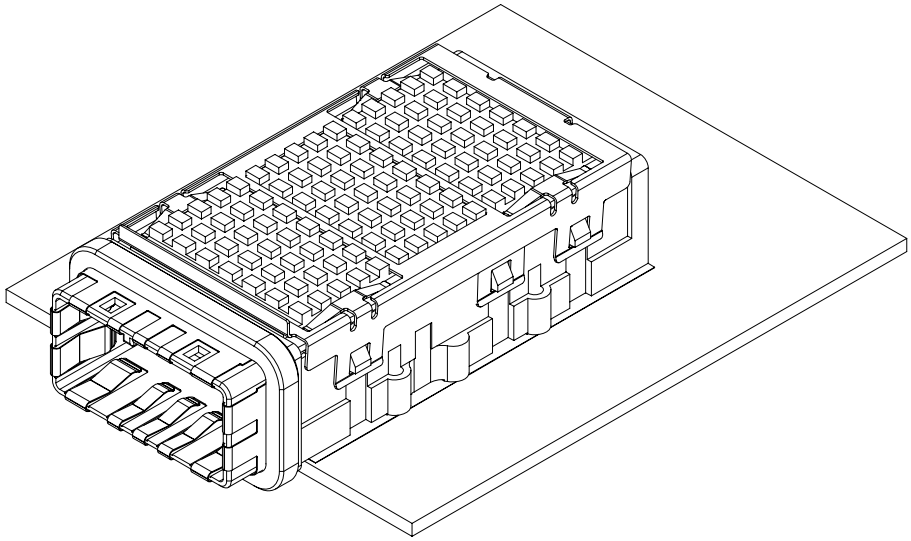
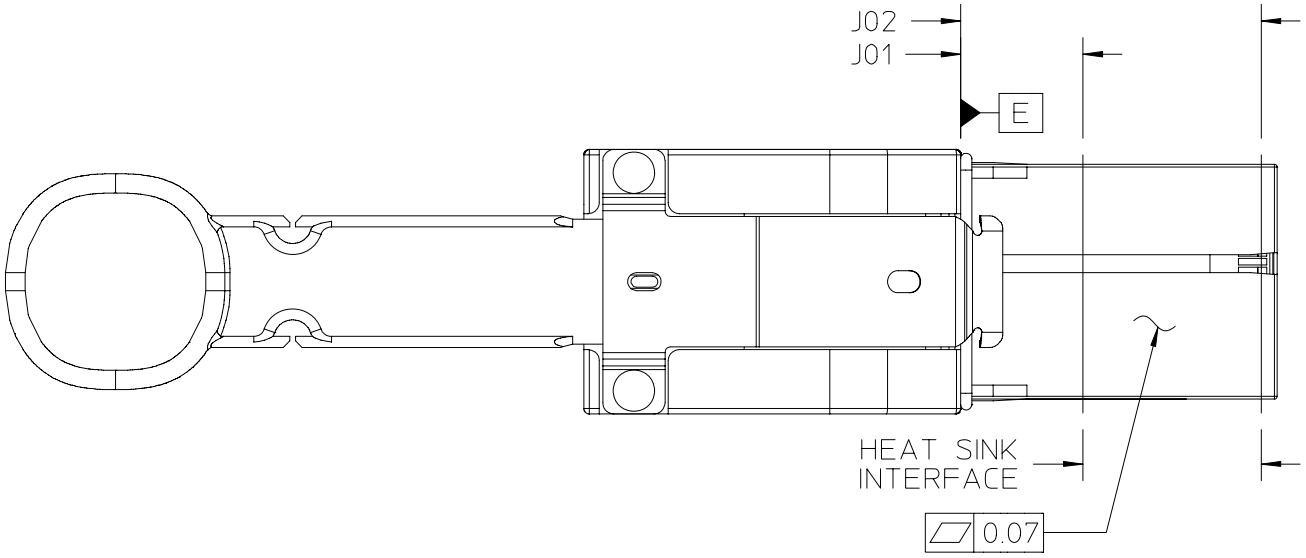


Figure 16 Receptacle Housing with Integrated Riding Heat Sink

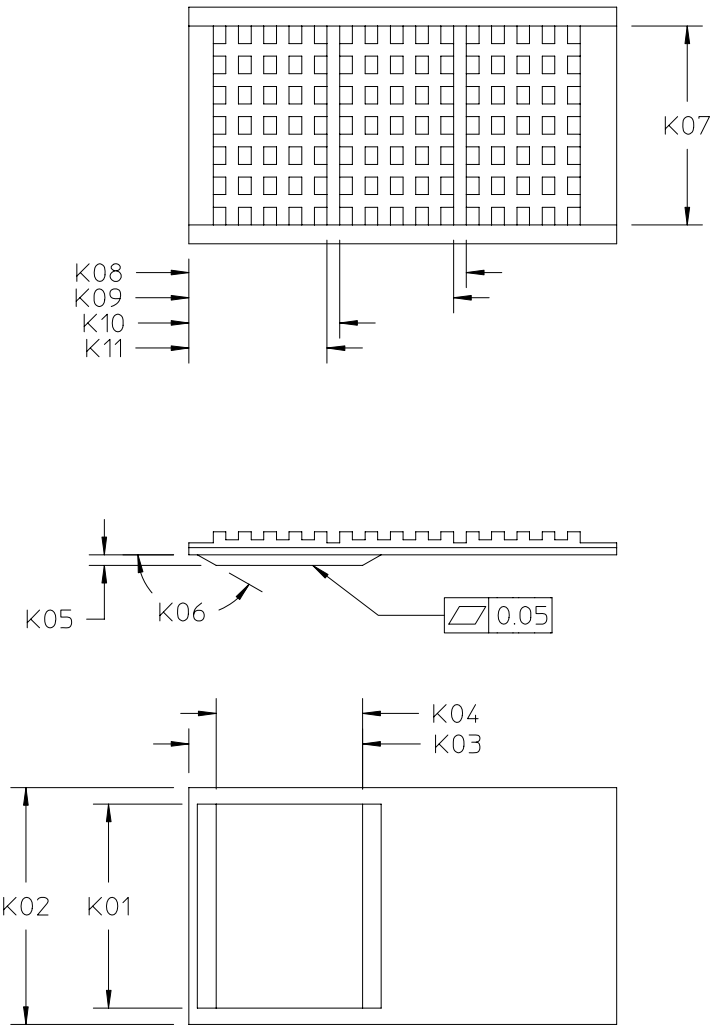
The thermal interface locations of the connector plug are shown in Figure 17 on page 45.



	Description	Dim.	Tol.
J01	Plug Body to Heat Sink Interface Start	11.00	Max
J02	Heat Sink Interface Zone	27.00	Min

Figure 17 Heat Sink Interface on Connector Plug

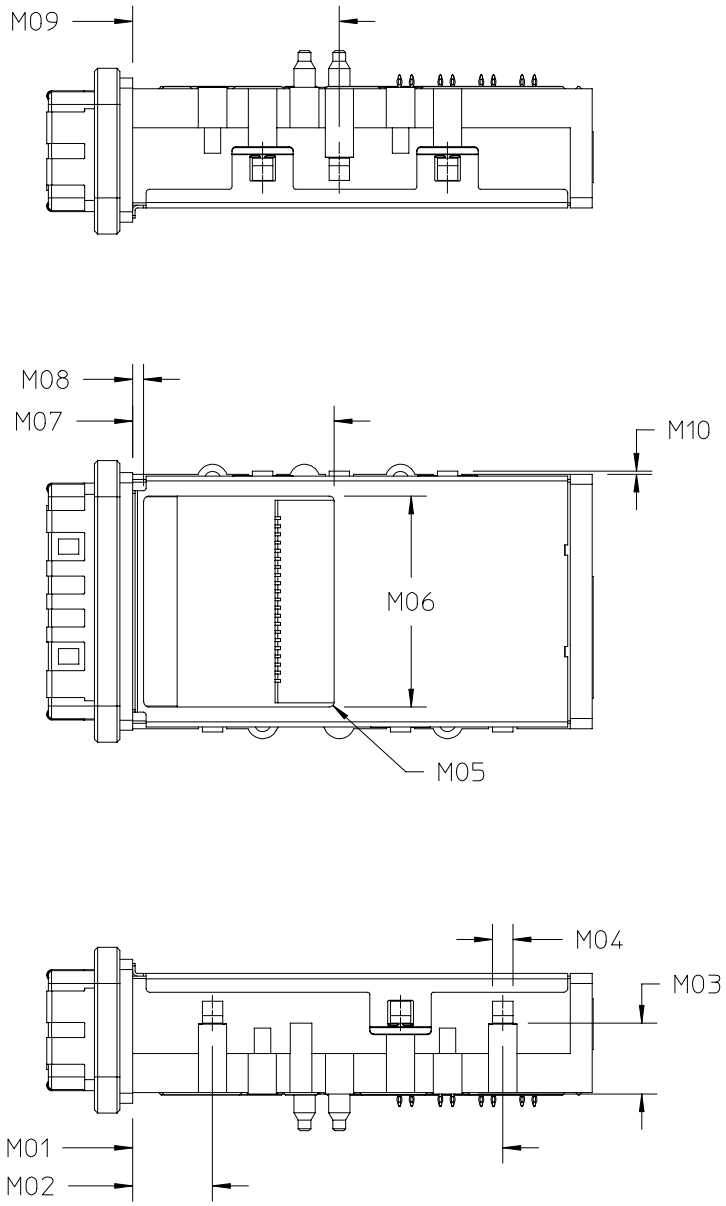
The dimensions for an example heat sink are shown in Figure 18 on page 46. Dimensions of the heat sink clip attachment points on the receptacle housing and for a heat sink clip are shown in Figure 19 on page 47 and Figure 20 on page 48, so that heat sinks appropriate to specific thermal environments or transmission media can be built. The heat sink clip in Figure 20 on page 48 interfaces with the example heat sink in Figure 18 on page 46. A modified heat sink would require a suitably-modified clip.



	Description	Dim.	Tol.
K01	Heat Sink Pad Width	20.75	0.10
K02	Heat Sink Width	23.50	0.10
K03	Heat Sink Pad Back Edge	15.57	0.10
K04	Heat Sink Pad Length	12.60	0.10
K05	Heat Sink Pad Height	0.94	0.10
K06	Heat Sink Lead-in Angle	150.00	5.00

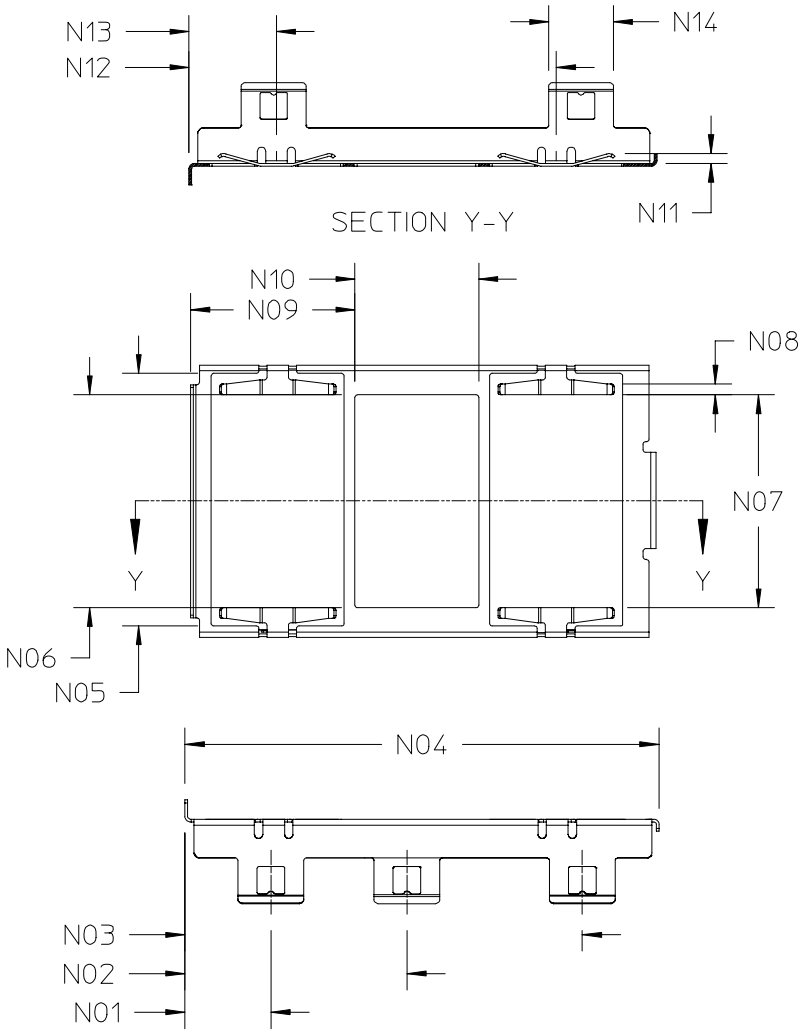
	Description	Dim.	Tol.
K07	Heat Sink Tower Width	19.75	0.10
K08	Heat Sink Clip Interface Zone	27.40	0.10
K09	Heat Sink Clip Interface Zone	26.15	0.10
K10	Heat Sink Clip Interface Zone	14.90	0.10
K11	Heat Sink Clip Interface Zone	13.65	0.10

Figure 18 Heat Sink Thermal Interface Profile



	Description	Dim.	Tol.		Description	Dim.	Tol.
M01	Flange to Heat Sink Attach Point	36.25	0.10	M06	Heat Sink Cover Opening Width	20.75	0.10
M02	Flange to Heat Sink Attach Point	7.84	0.10	M07	Flange to Heat Sink Cover Opening	18.65	0.10
M03	Heat Sink Attach Point Height	6.96	0.10	M08	Heat Sink Cover Opening Length	1.10	0.10
M04	Heat Sink Attach Point Width	2.00	0.10	M09	Flange to Heat Sink Attach Point	20.25	0.10
M05	Heat Sink Cover Opening Radius	0.50	0.10	M10	Height of Heat Sink Attach Point Feature	0.30	Min

Figure 19 Heat Sink Clip Attach Points on Receptacle Housing

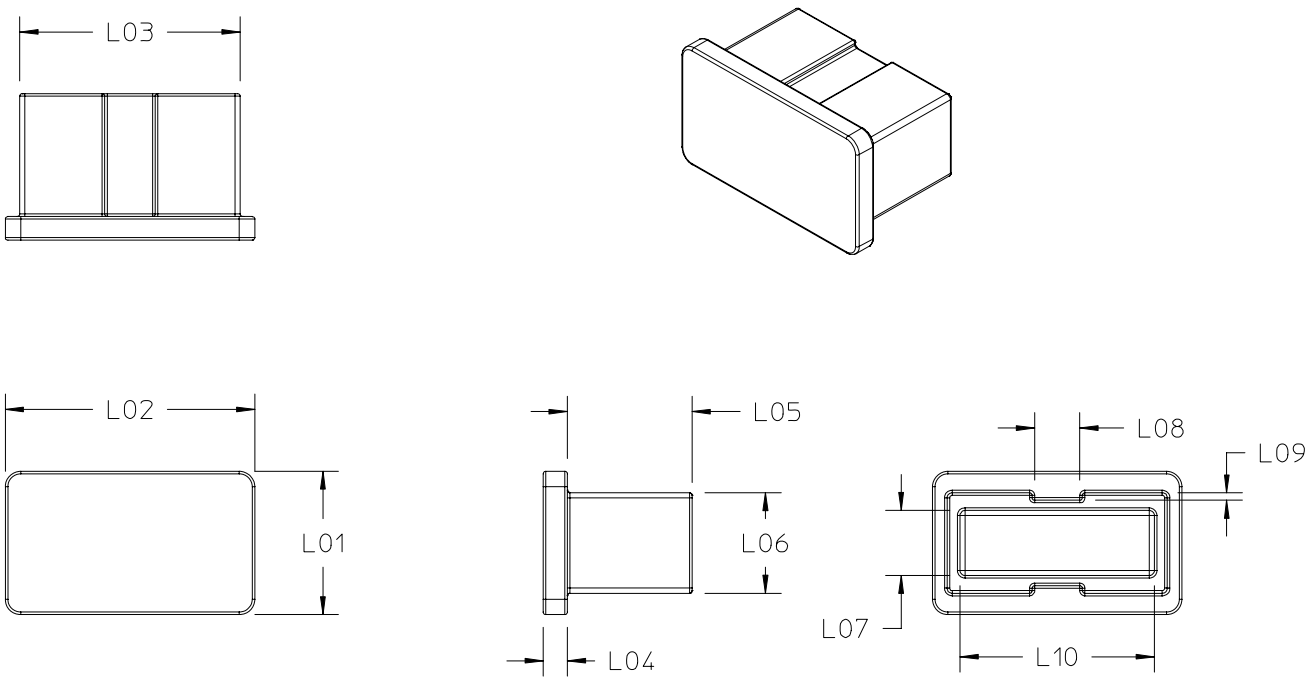


	Description	Dim.	Tol.		Description	Dim.	Tol.
N01	Heat Sink Clip Flange to Attach Point	7.84	0.10	N08	Heat Sink Clip Finger Width	1.00	Ref
N02	Heat Sink Clip Flange to Attach Point	20.25	0.10	N09	Heat Sink Clip Cut Out Length	15.28	0.10
N03	Heat Sink Clip Flange to Attach Point	36.25	0.10	N10	Heat Sink Clip Cut Out Length	11.50	0.10
N04	Heat Sink Clip Length	43.25	0.10	N11	Heat Sink Clip Finger Height	0.91	Ref
N05	Heat Sink Clip Cut Out Width	23.60	0.10	N12	Heat Sink Clip Finger Location	33.97	Ref
N06	Heat Sink Clip Cut Out Width	19.90	0.10	N13	Heat Sink Clip Finger Location	8.09	Ref
N07	Heat Sink Clip Finger to Finger	19.90	0.10	N14	Heat Sink Clip Attach Point Width	6.25	Max.

Figure 20 Heat Sink Clip Structure

5.6 EMI / DUST COVER FOR RECEPTACLE

If an EMI cover or dust cover for the receptacle is used, it shall have the dimensions shown in Figure 21 on page 49.



	Description	Dim.	Tol.		Description	Dim.	Tol.
L01	Front Height	14.00	Max	L06	Body Height	9.81	0.10
L02	Front Width	24.00	Max	L07	Body Inner Height	6.35	0.10
L03	Body Width	21.20	0.10	L08	Groove Width	4.35	0.10
L04	Front Thickness	2.00	Min.	L09	Groove Depth	0.73	Ref
L05	Body Length	12.00	Max	L10	Body Inner Width	18.70	0.10

Figure 21 EMI cover / Dust Cover

CHAPTER 6: CABLE DESIGN

6.1 DEVICE, MODULE, AND CABLE OPTIONS

A variety of modules, devices, and cables are envisioned for this interface. This list is not normative or restrictive, but will clarify potential design options.

6.1.1 SEPARABLE OPTICAL TRANSCEIVER

Figure 22 on page 50 shows an optical transceiver with separable optical optical, using a 24-fiber MPO-style connector. Details of the optical interface are described in Section 6.5 on page 56.

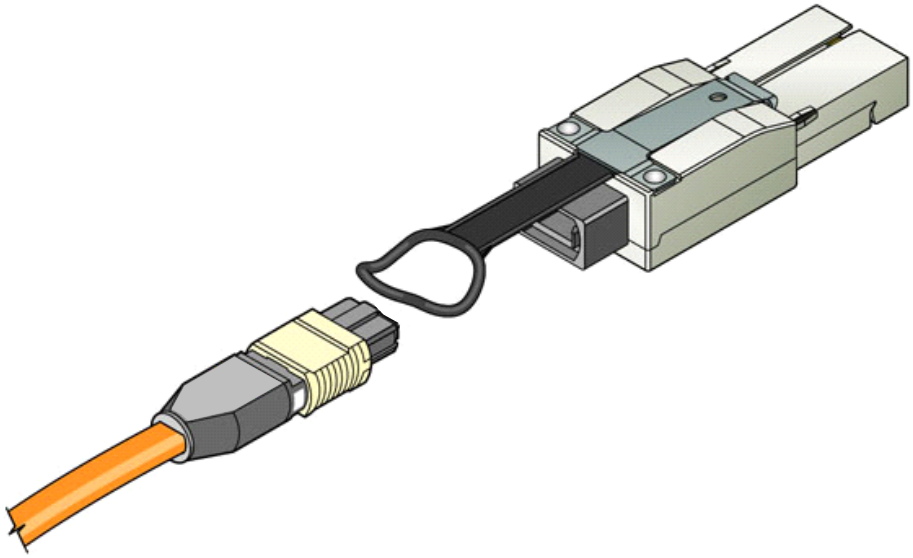


Figure 22 Optical Transceiver with separable optical cable

6.1.2 ACTIVE OPTICAL CABLE

Figure 23 on page 51 shows an active optical cable with CXP interfaces on each end.

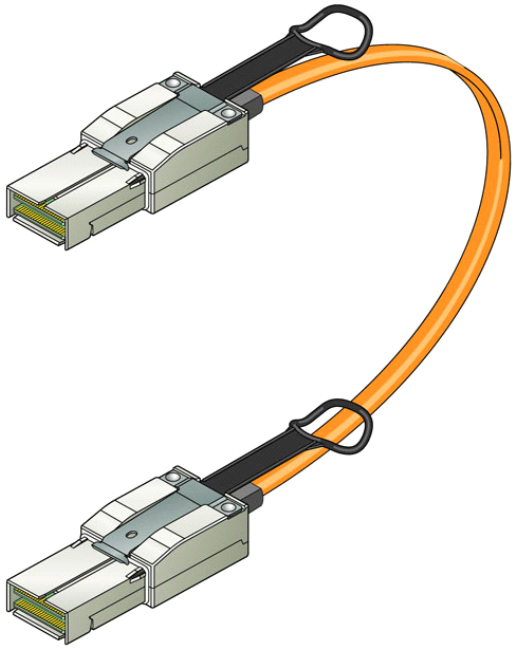


Figure 23 Active Optical Cable

6.1.3 COPPER CABLE

Figure 24 on page 51 shows a copper cable, which may be passively or actively equalized.

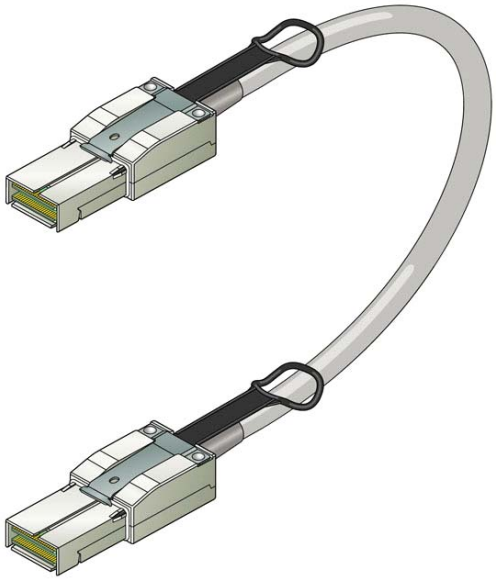
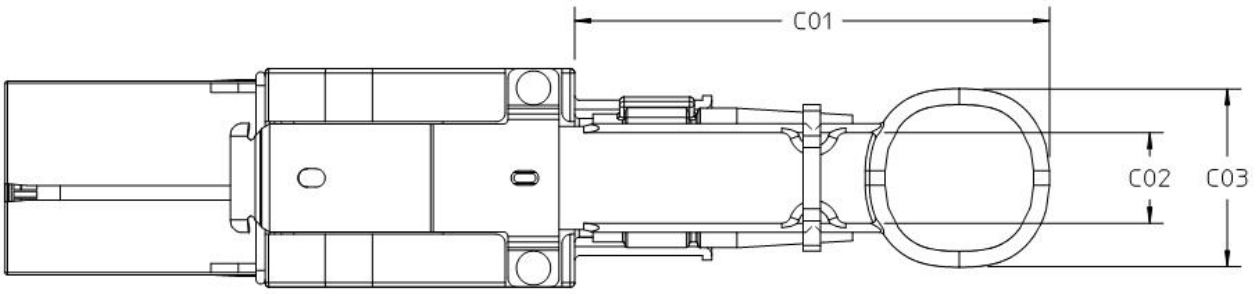


Figure 24 Passive or Active Copper Cable

6.2 LATCH RELEASE

CXP modules and cables need a releasable latch for retention into the receptacle housing assembly. Since a latch release mechanism is not an interface that affects interoperability, the design of the latch release mechanism may be media-dependent and vendor-dependent, and is not part of this specification.

Figure 25 on page 52 shows an example of a pull-tab type latch release mechanism for a cable connector.



	Description	Dim.	Tol.
C01	Pull Tab Length	50.00	Ref
C02	Pull Tab Inner Diameter	9.91	Ref
C03	Pull Tab Width	19.51	Ref

Figure 25 Exemplary Latch Release Mechanism for a Cable Connector

6.3 CABLE CONNECTIVITY

6.3.1 CABLE CONNECTIVITY MAPPING

Any cable, regardless of transmission medium, requires a mapping describing which signal contacts in each end connect to which signal contacts in the other end. This connectivity diagram is shown in Table 16 on page 53 below.

Table 16 Cable Connector Signal Assignment

Plug 1		Plug 2	
Contact Number	Signal	Contact number	Signal
A2	Tx1p	C2	Rx1p
A3	Tx1n	C3	Rx1n
A5	Tx3p	C5	Rx3p
A6	Tx3n	C6	Rx3n
A8	Tx5p	C8	Rx5p
A9	Tx5n	C9	Rx5n
A11	Tx7p	C11	Rx7p
A12	Tx7n	C12	Rx7n
A14	Tx9p	C14	Rx9p
A15	Tx9n	C15	Rx9n
A17	Tx11p	C17	Rx11p
A18	Tx11n	C18	Rx11n
B2	Tx0p	D2	Rx0p
B3	Tx0n	D3	Rx0n
B5	Tx2p	D5	Rx2p
B6	Tx2n	D6	Rx2n
B8	Tx4p	D8	Rx4p
B9	Tx4n	D9	Rx4n
B11	Tx6p	D11	Rx6p
B12	Tx6n	D12	Rx6n
B14	Tx8p	D14	Rx8p
B15	Tx8n	D15	Rx8n
B17	Tx10p	D17	Rx10p
B18	Tx10n	D18	Rx10n

Plug 1		Plug 2	
Contact Number	Signal	Contact number	Signal
C2	Rx1p	A2	Tx1p
C3	Rx1n	A3	Tx1n
C5	Rx3p	A5	Tx3p
C6	Rx3n	A6	Tx3n
C8	Rx5p	A8	Tx5p
C9	Rx5n	A9	Tx5n
C11	Rx7p	A11	Tx7p
C12	Rx7n	A12	Tx7n
C14	Rx9p	A14	Tx9p
C15	Rx9n	A15	Tx9n
C17	Rx11p	A17	Tx11p
C18	Rx11n	A18	Tx11n
D2	Rx0p	B2	Tx0p
D3	Rx0n	B3	Tx0n
D5	Rx2p	B5	Tx2p
D6	Rx-2	B6	Tx2n
D8	Rx4	B8	Tx4p
D9	Rx4n	B9	Tx4n
D11	Rx6p	B11	Tx6p
D12	Rx6n	B12	Tx6n
D14	Rx8p	B14	Tx8p
D15	Rx8n	B15	Tx8n
D17	Rx10p	B17	Tx10p
D18	Rx10n	B18	Tx10n

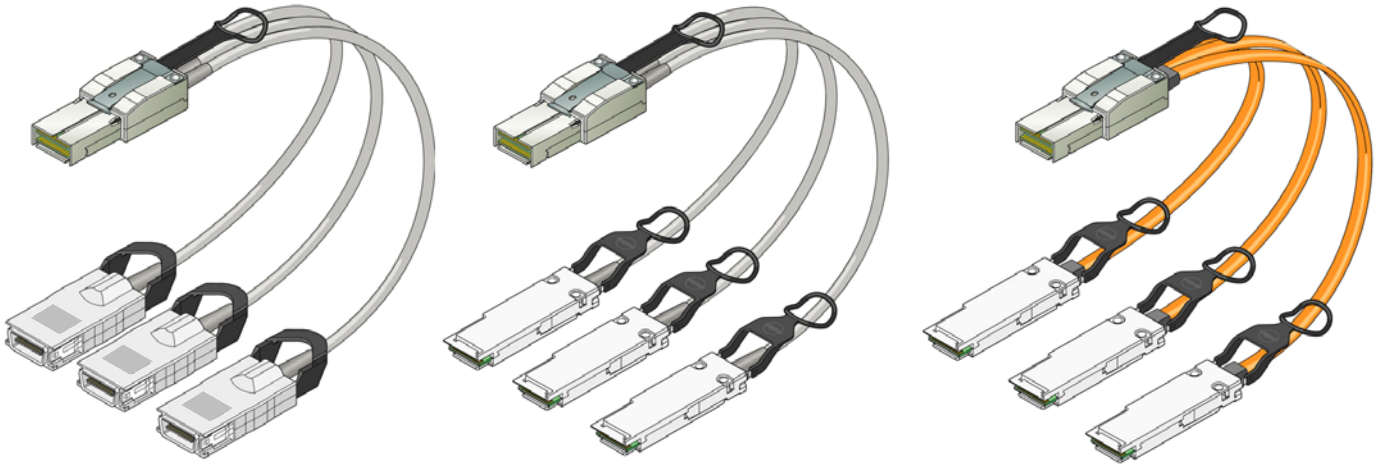
A1, A4, A7, A10, A13, A16, A19, B1, B4, B7, B10, B13, B16, B19, C1, C4, C7, C10, C13, C16, C19, D1, D4, D7, D10, D13, D16, D19 on each plug are connected to local Signal Ground. They are not connected through cable.

A20, A21, C20, and C21 are connected to local management interface. They are not connected through cable.

B20, B21, D20, and D21 provide local power. They are not connected through cable.

6.3.2 12X TO 3-4X CABLES

The 12x to 3-4x cables are used for connecting to devices which may configurably operate with a single 12x port, or with three separate 4x ports, using the same pins. The 12x to 3-4x cable provides an interface to a 12x interface board CXP connector, operating as either a single 12x port or as three 4x ports. The opposite side of the cable provides three separate 4x cable connectors. Figure 26 on page 54 shows these configurations, for copper and active optical cables.



a. CXP to 4x MicroGiga-CN

b. CXP to QSFP passive copper or active copper

c. CXP to QSFP active optical

Figure 26 12x to 3-4x cables

6.3.2.1 PIN ASSIGNMENTS

The pin assignment listed in Table 17 on page 55 below shall be used for the board connector for InfiniBand 12x to 3-4x cables.

Table 17 12x Board Connector Signal Assignment for 12x to 3-4x Cables

Pin Number	Contact (single 12x connector)	Signal (three 4x ports)[1,2]	Pin Number	Signal (single 12x port)	Signal (three 4x ports)
B2	Tx0p	IBtx.1Op(0)	D2	Rx0p	IBtx.1Ip(0)
B3	Tx0n	IBtx.1On(0)	D3	Rx0n	IBtx.1In(0)
A2	Tx1p	IBtx.1Op(1)	C2	Rx1p	IBtx.1Ip(1)
A3	Tx1n	IBtx.1On(1)	C3	Rx1n	IBtx.1In(1)
B5	Tx2p	IBtx.1Op(2)	D5	Rx2p	IBtx.1Ip(2)
B6	Tx2n	IBtx.1On(2)	D6	Rx-2	IBtx.1In(2)
A5	Tx3p	IBtx.1Op(3)	C5	Rx3p	IBtx.1Ip(3)
A6	Tx3n	IBtx.1On(3)	C6	Rx3n	IBtx.1In(3)
B8	Tx4p	IBtx.2Op(0)	D8	Rx4	IBtx.2Ip(0)
B9	Tx4n	IBtx.2On(0)	D9	Rx4n	IBtx.2In(0)
A8	Tx5p	IBtx.2Op(1)	C8	Rx5p	IBtx.2Ip(1)
A9	Tx5n	IBtx.2On(1)	C9	Rx5n	IBtx.2In(1)
B11	Tx6p	IBtx.2Op(2)	D11	Rx6p	IBtx.2Ip(2)
B12	Tx6n	IBtx.2On(2)	D12	Rx6n	IBtx.2In(2)
A11	Tx7p	IBtx.2Op(3)	C11	Rx7p	IBtx.2Ip(3)
A12	Tx7n	IBtx.2On(3)	C12	Rx7n	IBtx.2In(3)
B14	Tx8p	IBtx.3Op(0)	D14	Rx8p	IBtx.3Ip(0)
B15	Tx8n	IBtx.3On(0)	D15	Rx8n	IBtx.3In(0)
A14	Tx9p	IBtx.3Op(1)	C14	Rx9p	IBtx.3Ip(1)
A15	Tx9n	IBtx.3On(1)	C15	Rx9n	IBtx.3In(1)
B17	Tx10p	IBtx.3Op(2)	D17	Rx10p	IBtx.3Ip(2)
B18	Tx10n	IBtx.3On(2)	D18	Rx10n	IBtx.3In(2)
A17	Tx11p	IBtx.3Op(3)	C17	Rx11p	IBtx.3Ip(3)
A18	Tx11n	IBtx.3On(3)	C18	Rx11n	IBtx.3In(3)
A1, A4, A7, A10, A13, A16, A19, B1, B4, B7, B10, B13, B16, B19, C1, C4, C7, C10, C13, C16, C19, D1, D4, D7, D10, D13, D16, D19 on each plug are connected to local Signal Ground. They are not connected through cable.					
A20, A21, C20, and C21 are connected to local management interface. They are not connected through cable.					
B20, B21, D20, and D21 provide local power. They are not connected through cable.					

1. Nomenclature for signals is described in Vol. 2, Table 4.
2. Note that Pin Numbers / Contact Numbers are not specified, since they will be different for MicroGigaCN and QSFP connectors. Please refer to relevant specifications for contact numbers used for signals listed in this column.

6.4 LANE USAGE FOR 10-LANE INTERFACE

If 10 lanes are being used, as for a 100 Gb Ethernet interface, the middle lanes should be active, as they are less likely to see stress than the outer lanes. That is, logical lanes 0 through 9 in a 10-lane interface should be implemented on physical pins corresponding to lanes 1 through 10 in Table 2 on page 13, with the outer two lanes (0 and 11) in each direction left unused.

6.5 MEDIA-SPECIFIC REQUIREMENTS - OPTICAL TRANSCEIVERS AND OPTICAL CABLES

While most specified interface parameters are not dependent on which the transmission technology is used, some extra definition is required for specific transmission technologies, which have other interfaces. This section includes interface specifications for features which are useful for some device or cable technologies, but which are not required for all of them.

6.5.1 COLOR CODING AND LABELING OF CXP OPTICAL TRANSCEIVERS

For optical transceivers with separable optical connectors, an exposed feature of the CXP transceiver (a feature or surface extending outside of the bezel) shall be color coded as follows:

- Beige for 850 nm
- Blue for 1310 nm
- White for 1550 nm

Each CXP transceiver shall be clearly labeled. The complete labeling need not be visible when the CXP transceiver is installed and the bottom of the device is the recommended location for the label. Labeling shall include:

- Appropriate manufacturing and part number identification
- Appropriate regulatory compliance labeling
- A manufacturing traceability code

Also the label shall include clear specification of the external port characteristics such as:

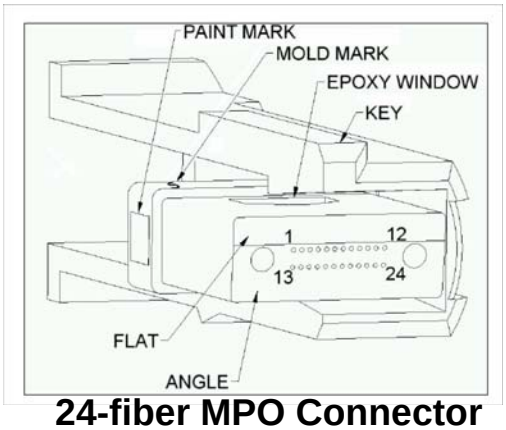
- Optical wavelength
- Required fiber characteristics
- Operating data rate
- Interface standards supported
- Link length supported

The labeling shall not interfere with the mechanical, thermal or EMI features.

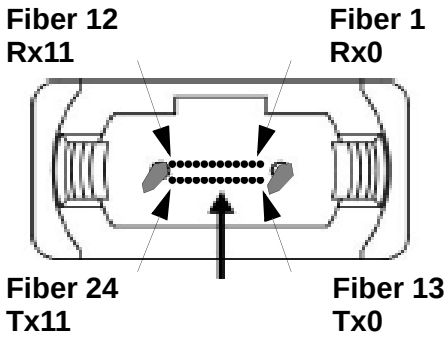
6.5.2 OPTICAL CONNECTOR INTERFACES FOR 24-FIBER TRANSCEIVERS

One potentially useful transmission medium is parallel optical transmission over 24 fibers, with 12 fibers transporting data in each direction. In the case of an optical transceiver, with dematable optical connector, as shown in the middle of Figure 1 on page 10, a 24-fiber MPO (also known as MTP) connector can support bidirectional transmission across (12+12) fibers, and fits within the CXP form factor.

For this transmission technology, transceivers shall use a 24-fiber MPO receptacle with the connector key oriented relative to Rx and Tx lane numbers as shown in Figure 1 on page 10. Optical cables with 24-fiber MPO-style connectors on each end shall be built "Key up/Key down", so that the helix half-twist incurred when the cable is plugged into transceivers will correctly connect transmitter lanes to receiver lanes, lanes 0 to lanes 0, and lanes 11 to lanes 11. MPO-style "male" alignment pins shall be used in the receptacle, and a "female" MPO-style connector shall be used on the cable connector. This is shown in Figure 27 on page 57 below.



24-fiber MPO Connector



24-fiber MPO Receptacle

Rotated 24-fiber MPO Receptacle, e.g., for below-PCB mounting

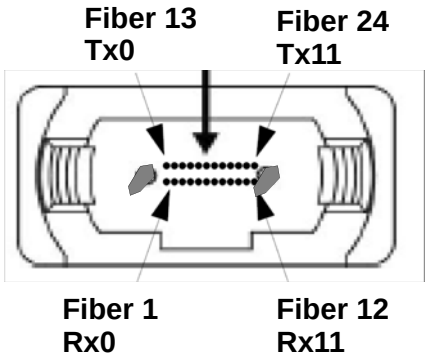


Figure 27 Connector orientation for 24-fiber MPO/MTP connector

6.5.3 INTERFACE BETWEEN 24-FIBER CONNECTOR AND DUAL 12-FIBER CONNECTORS

Interface between the 24-fiber MPO-style receptacle and a pair of 12-fiber MPO receptacles or male MPO-style connectors is shown Figure 28 on page 58 below.

This will be used for interfacing with prior 12x InfiniBand ports, or with structured cabling that uses 12-fiber MPO-style connectors and cables.

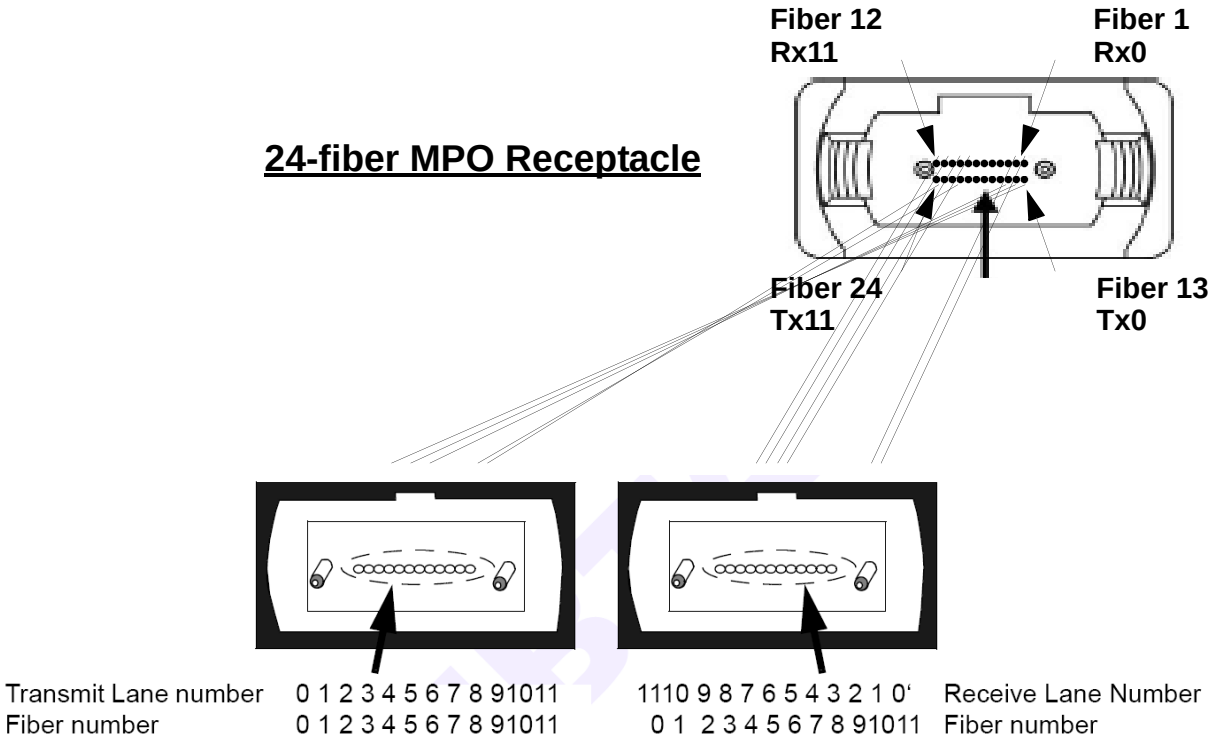


Figure 28 Connector interface between 24-fiber and Two 12-fiber connectors

CHAPTER 7: MANAGEMENT INTERFACE

7.1 INTRODUCTION

A management interface, as already commonly used in other form factors like GBIC, SFP, XFP and QSFP is specified in order to enable flexible use of the transceiver by the user. The specification has been modeled on the definition of the QSFP (Quad Small Form-factor Pluggable) multi-lane receiver, with extensions as needed to support 12-lane operation, at up to (120+120) Gb/s. Some timing requirements are critical, especially for a multi-lane device, so the interface speed has been increased relative to single-lane devices such as GBIC, SFP, and XFP.

7.2 VOLTAGE AND TIMING SPECIFICATION

7.2.1 MANAGEMENT INTERFACE VOLTAGE SPECIFICATION

Management signaling logic levels are based on Low Voltage CMOS operating at 3.3V Vcc. Host shall use a pull-up to Vcc3.3 for the 2-wire interface SCL (clock), SDA (address & data), and Int_L/Reset_L signals.

The electrical specifications are given in Table 18 on page 59. This specification ensures compatibility between host bus masters and the 2-wire interface

Table 18 Low Speed Control and Sense Signal Specifications

Parameter	Symbol	Min	Max	Units	Condition
Module Input Voltage Low	Vil	-0.3	0.4	V	Pull-up to 3.3V.
Module Input Voltage High	Vih	2.3	3.6	V	Min Vih = 0.7*3.3V.
Module Output Voltage Low	Vol	-0.3	0.3	V	Condition IOL=3.0 mA. Pull-up to 3.3V.
Module Output Voltage High	Voh	2.8	3.6	V	Min Voh = 3.3V - 0.5V.
Module Output Current High	Ioh	-10	10	µA	-0.3V < Voutput < 3.6V
Capacitance of module on SCL & SDA contacts	$C_{i,SCLSDA}$		14	pF	Allocate 10 pF for IC, 4 pF for module PCB
Capacitance of module on Int_L/Reset_L I/O contact	C_{i,INT_L}		36	pF	Allocate 28 pF for IC, 8 pF for module PCB
Total bus capacitive load, SCL, SDA, and Int_L/Reset_L I/O pin	Cb		100	pF	3.0 kOhms Pullup resistor, max
			200	pF	1.6 kOhms Pullup resistor, max

7.2.2 MANAGEMENT INTERFACE TIMING SPECIFICATION

In order to support a multi-lane device a 400 kHz clock rate for the serial interface is expected. The timing requirements are shown in Figure 29 on

page 60 and specified in Table 19 on page 60. All values are referred to VIH(min) and VIL(max) levels shown in Table 18 on page 59.

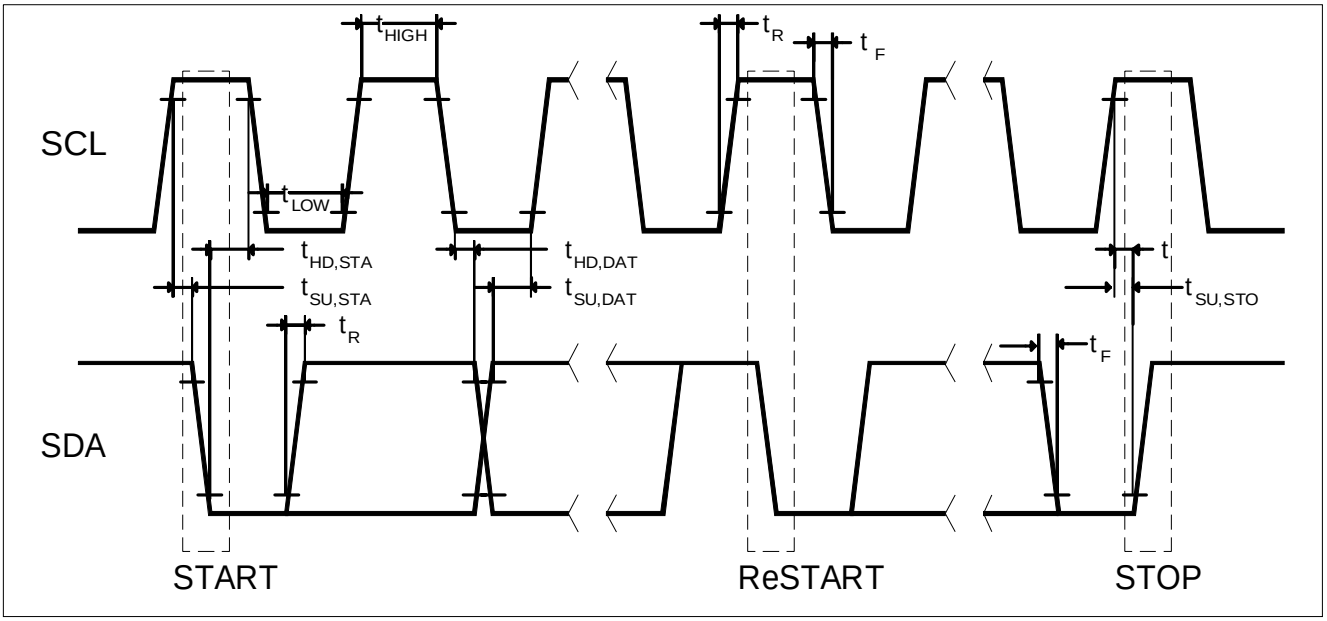


Figure 29 CXP 2-wire Serial Interface Timing Diagram

Table 19 CXP 2-Wire Serial Interface Timing Specifications

Parameter	Symbol	Min	Max	Unit	Condition
Clock Frequency	f_{SCL}	0	400	kHz	
Clock Pulse Width Low	t_{LOW}	1.3		µs	
Clock Pulse Width High	t_{HIGH}	0.6		µs	
Time bus free before new transmission can start	t_{BUF}	20		µs	Note 1
START Set-up Time	$t_{SU,STA}$	0.6		µs	
START Hold Time	$t_{HD,STA}$	0.6		µs	
Data Set-up Time	$t_{SU,DAT}$	0.1		µs	Note 2
Data Hold Time	$t_{HD,DAT}$	0		µs	Note 3
SDA and SCL rise time	$t_{R,400}$		0.3	µs	Note 4
SDA and SCL fall time	$t_{F,400}$		0.3	µs	Note 5
STOP Set-up Time	$t_{SU,STO}$	0.6		µs	

1. Between STOP & START and between ACK & ReSTART.
2. Data In Set Up Time is measured from Vil(max)SDA or Vih(min)SDA to Vil(max)SCL.
3. Data In Hold Time is measured from Vil(max)SCL to Vil(max)SDA or Vih(min)SDA.
4. Rise Time is measured from Vol(max)SDA to Voh(min)SDA.
5. Fall Time is measured from Voh(min)SDA to Vol(max)SDA.

7.3 MEMORY INTERACTION SPECIFICATIONS

CXP memory may be accessed in either single-byte or multiple-byte memory blocks. The largest multiple-byte contiguous write operation that a module shall handle is 4 bytes. The minimum size write block is 1 byte.

7.3.1 TIMING FOR MEMORY TRANSACTIONS

CXP memory transaction timings are given in Table 20.

Table 20 CXP Memory Transaction Timing Specification

Parameter	Symbol	Min	Max	Unit	Condition
Serial Interface Clock Holdoff - “Clock Stretching”	T_clock_hold		500	µs	Note 1
Complete Single or Sequential Write	t_{WR}		40	ms	Note 2
Endurance (Write cycles)		50,000		cycles	3

1. Maximum time the CXP module may hold the SCL line low before continuing with a read or write operation.
2. Complete up to 4 Byte write. Timing should start from Stop bit at the end of the sequential write operation and continue until the module responds to another operation.
3. 50K write cycles at 70C.

7.3.2 TIMING FOR CONTROL AND STATUS FUNCTIONS

Timing for CXP control & status functions are described in Table 21.

Table 21 I/O Timing for Control and Status Functions

Parameter	Symbol	Min	Max	Unit	Condition, and Notes
Initialization Time	t_{init}		2000	ms	Note [1] [2], [3]
Reset Pulse Width - Min.	$t_{reset\_L,PW-min}$	25		ms	Note [4]
Monitor Data Ready Time	t_{data}		2000	ms	Note [5]
Reset Assert Time	$t_{RSTL,OFF}$		2000	ms	Note [6]
Int_L Assert Time	$t_{Int\_L,ON}$		200	ms	Note [7]
Interrupt Pulse Width - Min	$t_{Int\_L,PW-min}$	5		µs	Note [8]
Interrupt Pulse Width - Max	$t_{Int\_L,PW-max}$		50	µs	Note [9]
Int_L Deassert Time	$t_{Int\_L,OFF}$		0.5	ms	Note [10]
Rx LOS Assert Time	$t_{LOS,ON}$		100	ms	Note [11]
Tx Fault Assert Time	$t_{Txfault,ON}$		200	ms	Note [12]
Flag Assert Time	$t_{flag,ON}$		200	ms	Note [13]
Mask Assert Time	$t_{mask,OFF}$		100	ms	Note [14]
Mask Deassert Time	$t_{mask,ON}$		100	ms	Note [15]
Select Change Time	$t_{ratesel}$		100	ms	Note [16]
Power_over-ride or Power-set Assert Time	$t_{Pdown,ON}$		100	ms	Note [17]
Power_over-ride or Power-set Deassert Time	$t_{Pdown,OFF}$		300	ms	Note [18]

1. Time from power on, hot plug or rising edge of Reset until the module is fully functional. This time does not apply to non-Power Level 0 modules in the Low Power State.
2. Power on is defined as the instant when supply voltages reach and remain at or above the minimum level specified in Table 3.
3. Fully functional is defined as Int_L asserted due to Data Not Ready (Byte 2, bit 0) deasserted. The module should also meet optical and electrical specifications.
4. This is the minimum Reset_L pulse width required to reset a module. Assertion of Reset_L activates a complete module reset, i.e., module returns to factory default control settings. While Reset_L is Low, Tx and Rx outputs are disabled and the module does not response to the two-wire serial interface.
5. Time from power on to Data Not Ready (Byte 2, bit 0) deasserted and Int_L asserted.
6. Time from rising edge on the Reset_L contact until the module is fully functional. During the Reset Time module will not respond to a “low” on the Int_L/Reset_L signal.
7. Time from occurrence of condition triggering Int_L until Vout:Int_L = Vol.
8. Int_L operates in pulse mode. Static mode (Int_L stays low until reset by host) is not supported for Int_L.
9. Int_L pulse width must not exceed $t_{Int\_L,PW-max}$, to distinguish Int_L from a Reset for other devices on bus.
10. Time from clear on read operation of associated flag until Int_L Status (Lower page, byte 2, bit 1) is cleared. This includes deassert times for Rx LOS, Tx Fault and other flag bits. Measured from falling clock edge after stop bit of read transaction.
11. Time from Rx LOS state to Rx LOS bit set (value = 1b) and Int_L asserted.
12. Time from Tx Fault state to Tx Fault bit set (value = 1b) and Int_L asserted.
13. Time from occurrence of condition triggering flag to associated flag bit set (value = 1b) and Int_L asserted.
14. Time from mask bit set (value = 1b) until associated Int_L assertion is inhibited.
15. Time from mask bit cleared (value = 0b) until associated Int_L operation resumes.
16. Time from change of state of Application or Rate Select bit until transmitter or receiver bandwidth is in conformance with appropriate specification.
17. Time from P_Down bit set (value = 1b) until module power consumption enters Power Class 0.
18. Time from P_Down bit cleared (value = 0b) until the module is fully functional.

7.3.3 TIMING FOR SQUELCH AND DISABLE FUNCTIONS

Squelch and disable times are described in Table 22.

Table 22 I/O Timing for Squelch and Disable

Parameter	Symbol	Min	Max	Unit	Condition and Notes
Rx Squelch Assert Time	$t_{Rxsq,ON}$		0.080	ms	Note 1
Rx Squelch Deassert Time	$t_{Rxsq,OFF}$		0.080	ms	Note 2
Tx Squelch Assert Time	$t_{Txsq,ON}$		400	ms	Note 3
Tx Squelch Deassert Time	$t_{Txsq,OFF}$		400	ms	Note 4
Tx Disable Assert Time	$t_{Txdis,ON}$		100	ms	Note 5
Tx Disable Deassert Time	$t_{Txdis,OFF}$		400	ms	Note 6
Rx Output Disable Assert Time	$t_{Rxdis,ON}$		100	ms	Note 7
Rx Output Disable Deassert Time	$t_{Rxdis,OFF}$		100	ms	Note 8
Squelch Disable Assert Time	$t_{Sqdis,ON}$		100	ms	Note 9
Squelch Disable Deassert Time	$t_{Sqdis,OFF}$		100	ms	Note 10

1. Time from loss of Rx input signal until the squelched output condition is reached. See Section 2.4.1.
2. Time from resumption of Rx input signals until normal Rx output condition is reached. See Section 2.4.1.
3. Time from loss of Tx input signal until the squelched output condition is reached. See Section 2.4.2.
4. Time from resumption of Tx input signals until normal Tx output condition is reached. See Section 2.4.2.
5. Time from Tx Disable bit set (value = 1b) until optical output falls below 10% of nominal.
6. Time from Tx Disable bit cleared (value = 0b) until optical output rises above 90% of nominal. Measured from Stop bit low-to-high SDA transition.
7. Time from Rx Output Disable bit set (value = 1b) until Rx output falls below 10% of nominal.
8. Time from Rx Output Disable bit cleared (value = 0b) until Rx output rises above 90% of nominal.
9. This applies to Rx and Tx Squelch and is the time from bit set (value = 1b) until squelch functionality is disabled.
10. This applies to Rx and Tx Squelch and is the time from bit cleared (value = 0b) until squelch functionality is enabled.

7.4 DEVICE ADDRESSING AND OPERATION

Serial Clock (SCL): The host supplied SCL input to CXP transceivers is used to positive-edge clock data into each CXP device and negative-edge clock data out of each device. The SCL line may be pulled low by a CXP module during clock stretching.

Serial Data (SDA): The SDA signal is bidirectional for serial data transfer. This signal is open-drain or open-collector driven and may be wire-ORed with multiple open-drain or open collector devices, limited by aggregate capacitance vs. clock speed.

Master/Slave: CXP transceivers operate only as slave devices. The host must provide a bus master for SCL and initiate all read/write communication.

Device Address: All CXP modules use the same base addresses, 1010 000x and 1010 100x, where x indicates read (1) or write(0). Each CXP module supports an internal memory map, with one or more 128B lower page and one or more 128B upper pages, depending on module capabilities. See Section 7.6 for memory map structure within each module.

Single CXP device per SCL/SDA: Since all CXP transceivers or modules use the same two base addresses, each CXP port requires its own SCL/SDA bus. Support of multiple ports in a host requires multiple SCL/SDA buses, or multiplexing circuitry such as a multiplexer chip or a switch chip. See Section 2.3 and Table 18 for more information.

Clock and Data Transitions: The SDA signal is normally pulled high in the host. Data on the SDA signal may change only during SCL low time periods. Data changes during SCL high periods indicate a START or STOP condition. All addresses and data words are serially transmitted to and from the CXP in 8-bit words. Every byte on the SDA line must be 8-bits long. Data is transferred with the most significant bit (MSB) first.

START Condition: A high-to-low transition of SDA with SCL high is a START condition, which must precede any other command.

STOP Condition: A low-to-high transition of SDA with SCL high is a STOP condition.

Acknowledge: After sending each 8-bit word, the transmitter releases the SDA line for one bit time, during which the receiver is allowed to pull SDA low (zero) to acknowledge (ACK) that it has received each word. Device address bytes and write data bytes initiated by the host shall be acknowledged by CXP transceivers. Read data bytes transmitted by CXP transceivers shall be acknowledged by the host for all but the final byte read, for which the host shall respond with a STOP instead of an ACK.

Memory (Management Interface) Reset: After an interruption in protocol, power loss or system reset the CXP management interface can be reset. Memory reset is intended only to reset the CXP transceiver management interface (to correct a hung bus). No other transceiver functionality is implied.

1) Clock up to 9 cycles.
2) Look for SDA high in each cycle while SCL is high.
3) Create a START condition as SDA is high

Device Addressing: CXP devices require an 8-bit device address word following a start condition to enable a read or write operation. The device address word consists of a mandatory sequence for the first seven most significant bits, as shown in Figure 30. This is common to all CXP devices.

Transmitter Functions (0xA0)	1	0	1	0	0	0	0	R(1) / W(0)
Receiver Functions (0xA8)	1	0	1	0	1	0	0	R(1) / W(0)
	Most Significant Bit							Least Significant Bit
Standard Two-wire Serial Device Address	1	0	1	0	A2	A1	A0	R/W

Figure 30 CXP Device Addresses

The eighth bit of the device address is the read/write operating select bit. A read operation is initiated if this bit is set high and a write operation is initiated if this bit is set low. Upon compare of the device address the CXP transceiver shall output a zero (ACK) on the SDA line to acknowledge the address.

Nomenclature for all registers more than 1 bit long is MSB-LSB.

7.5 READ/WRITE FUNCTIONALITY

7.5.1 CXP MEMORY ADDRESS COUNTER (READ AND WRITE OPERATIONS)

CXP devices maintain an internal data word address counter containing the last address accessed during the latest read or write operation, incremented by one. The address counter is incremented whenever a data word is received or sent by the transceiver. This address stays valid between operations as long as CXP power is maintained. The address “roll over” during read and writes operations is from the last byte of the 128-byte memory page to the first byte of the same page.

7.5.2 READ OPERATIONS (CURRENT ADDRESS READ)

A current address read operation requires only the device address read word (10100001-Tx base address or 10101001-Rx base address) be sent, see Figure 31 on page 66. Once acknowledged by the CXP, the current address data word is serially clocked out. The host does not respond with an acknowledge, but does generate a STOP condition once the data word is read.

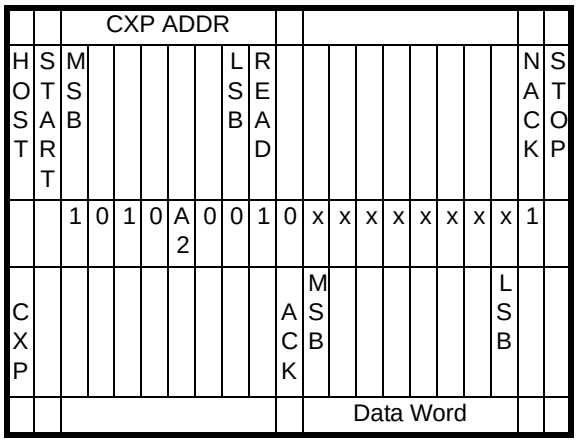


Figure 31 Read Operation on Current Address

7.5.3 READ OPERATIONS (RANDOM READ)

A random read operation requires a “dummy” write operation to load in the target byte address as shown in Figure 32 on page 67. This is accomplished by the following sequence: The target 8-bit data word address is sent following the device address write word (1010 0000 or 1010 1000) and acknowledged by the CXP module. The host then generates another START condition (aborting the dummy write without incrementing the counter) and a current address read by sending a device read base address (1010 0001 for Tx or 1010 1001 for Rx). The CXP acknowledges the device address and serially clocks out the requested data word. The

host does not respond with an acknowledge, but does generate a STOP condition once the data word is read.

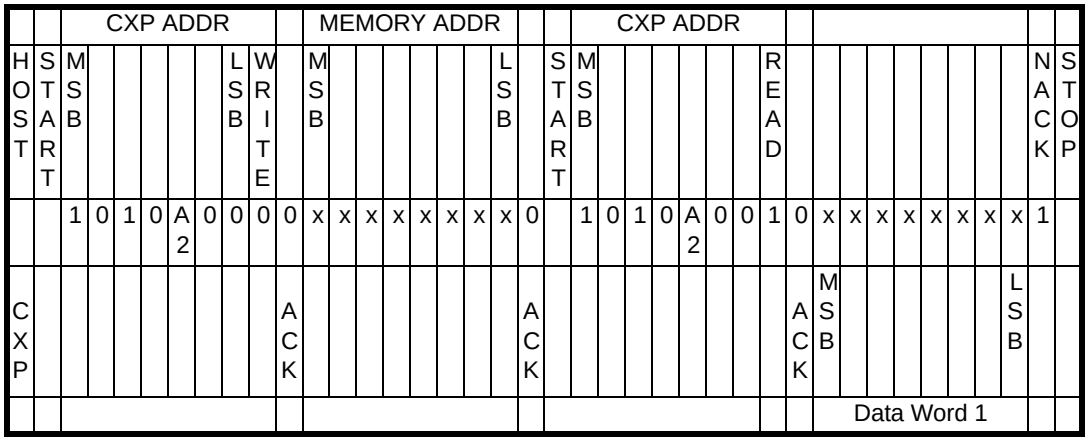


Figure 32 Random Read

7.5.4 READ OPERATIONS (SEQUENTIAL READ)

Sequential reads are initiated by either a current address read Figure 33 on page 68 or a random address read Figure 34 on page 68.To specify a sequential read, the host responds with an acknowledge (instead of a STOP) after each data word. As long as the CXP device receives an acknowledge, it shall serially clock out sequential data words. The sequence

is terminated when the host responds with a NACK and a STOP instead of an acknowledge.

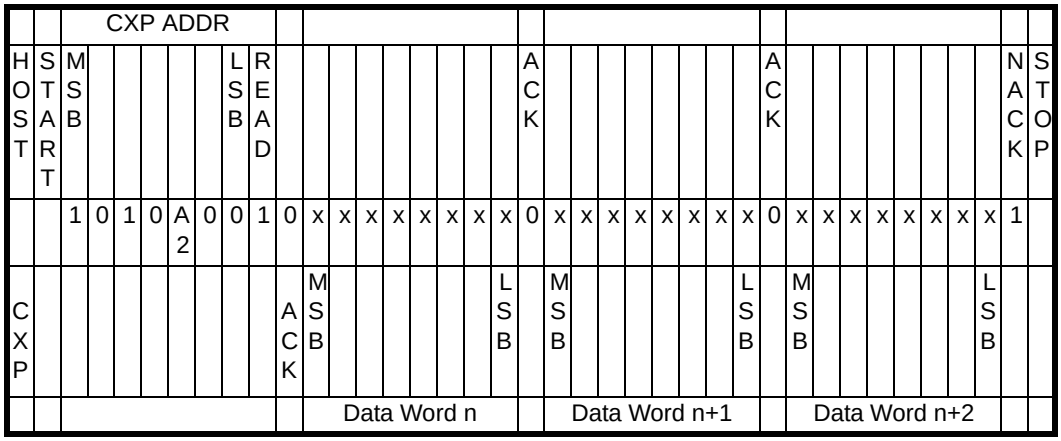


Figure 33 Sequential Address Read Starting at Current Address

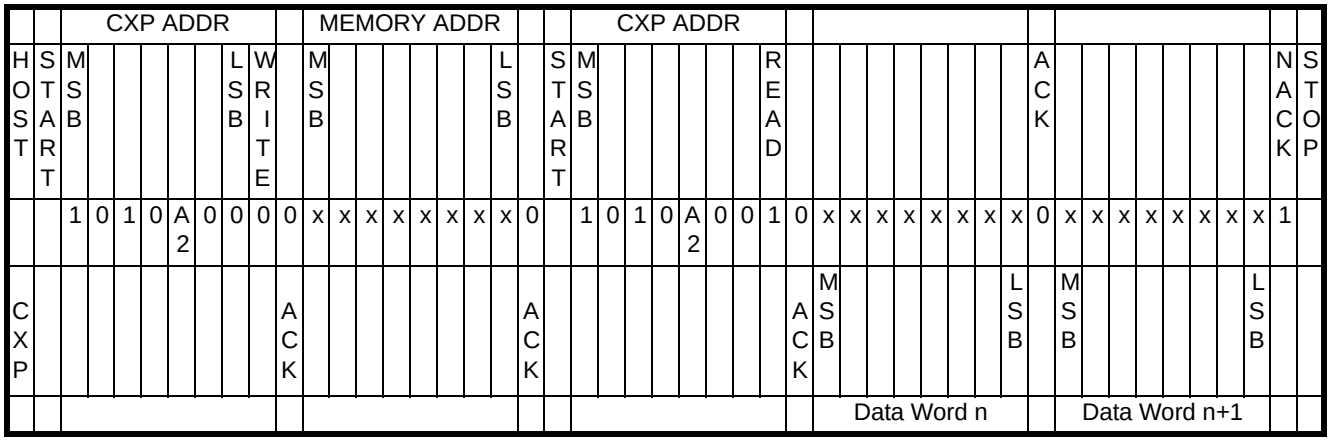


Figure 34 Sequential Address Read Starting with Random CXP Read

7.5.5 WRITE OPERATIONS (BYTE WRITE)

A write operation requires an 8-bit data word address following the device address write word (0101 efg0) and acknowledgement, see Figure 35 on page 69. Upon receipt of this address, the CXP shall again respond with a zero (ACK) to acknowledge and then clock in the first 8-bit data word. Following the receipt of the 8-bit data word, the CXP shall output a zero (ACK) and the host master must terminate the write sequence with a STOP condition for the write cycle to begin. If a START condition is sent

in place of a STOP condition (i.e. a repeated START per the 2-wire interface specification) the write is aborted and the data received during that operation is discarded. Upon receipt of the proper STOP condition, the CXP enters an internally timed write cycle, t_{WR}, to internal memory. The CXP disables it's management interface input during this write cycle and shall not respond or acknowledge subsequent commands until the write is complete. Note that 2-wire interface "Combined Format" using repeated START conditions is not supported on CXP write commands.

		CXP ADDR									MEMORY ADDR									Data Word										
HOST	START	MSB						LSB	WRITE		MSB							LSB		MSB						LSB		STOP
		1	0	1	0	A2	0	0	0	0	x	x	x	x	x	x	x	x	0	x	x	x	x	x	x	x	x	0	
CXP										ACK									ACK									ACK	

Figure 35 Write Byte Operation

7.5.6 WRITE OPERATIONS (SEQUENTIAL WRITE)

A CXP device shall support up to a 4 sequential byte write without repeatedly sending CXP address and memory address information as shown in Figure 36 on page 70. A "sequential" write is initiated the same way as a single byte write, but the host master does not send a stop condition after the first word is clocked in. Instead, after the CXP acknowledges receipt of the first data word, the host can transmit up to three more data words. The CXP shall send an acknowledge after each data word received. The host must terminate the sequential write sequence with a STOP condition or the write operation shall be aborted and data discarded. Note that 2-

wire interface “combined format” using repeated START conditions is not supported on CXP write.

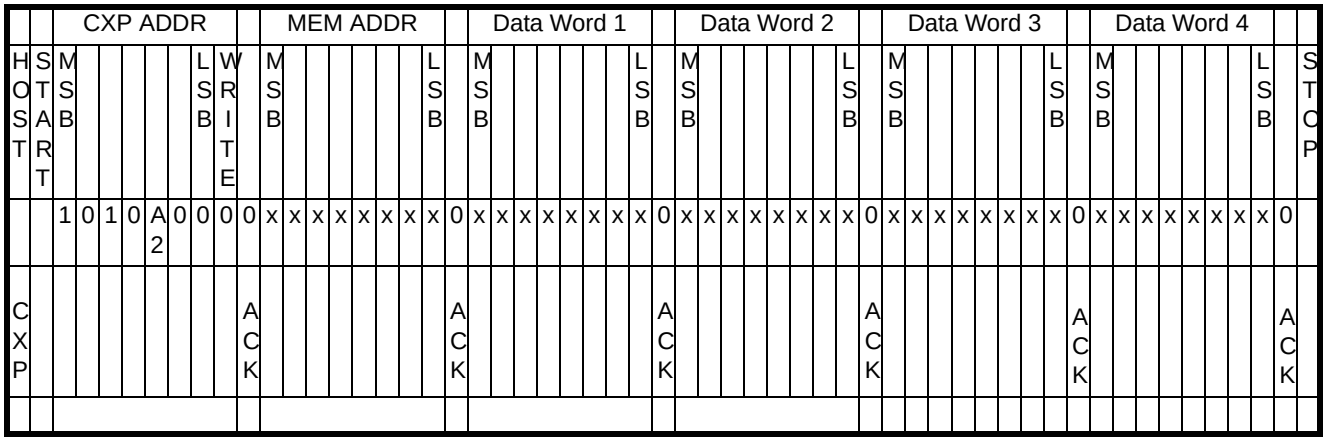


Figure 36 Sequential Write Operation

7.5.7 WRITE OPERATIONS (ACKNOWLEDGE POLLING)

Once the CXP internally timed write cycle has begun (and inputs are being ignored on the bus) acknowledge polling can be used to determine when the write operation is complete. This involves sending a START condition followed by the device address word. Only if the internal write cycle is complete shall the CXP respond with an acknowledge to subsequent commands, indicating read or write operations can continue.

7.6 CXP MEMORY MAP

This section defines the Memory Map for CXP transceiver used for serial ID, digital monitoring and certain control functions. The interface is mandatory for all CXP devices. The interface has been designed largely after the XFP MSA as defined in INF-8077i Rev.4.0. The memory map has been modified to accommodate 12 lanes per direction and to limit the required memory space. Paging on upper pages is used to allow slower access to less time-critical information.

The memory map has also been configured to support a range of device types, from simple passive cables with only EEPROM chips with two-wire serial interfaces for identification, to, for example, optical transceivers with tunable equalization and per-lane optical power monitoring. All devices conforming to this interface are required to implement a basic memory map, including various fields such as fields to identify the device type and manufacturer.

The structure of the memory map is shown in Figure 37 on page 72. It includes two ranges of serial addresses, at 0xA0 (for Tx and basic required functions), and 0xA8 (for optional extensions, including Rx functions). Each address (0xA0 and 0xA8) contains one lower page and at least one upper page (00h), with one optional other upper page (01h) per address range. Each page contains 128 bytes of address space. The lower page or pages contain Read-Only information, and may contain Read-Write fields as well, for more sophisticated devices. The upper pages contain only Read-Only (RO) information. Only the first upper page (00h) is required. Other(s) are optional, to allow devices without pageable memory.

This structure permits timely access to fields in the lower page, which contain time-critical information, such interrupt flags, alarms, critical monitors (temperature, voltage,...) and per-lane control. Read-only device information such as serial ID information, vendor information, is available in Upper Page 00, which is identical for both 0xA0 and 0xA8 device addresses. Less time-critical Read-Only information on more complex devices, such as threshold settings or per-channel monitors, are available with the optional Upper Page Select function.

The structure also allows for address expansion by adding additional upper pages as needed. This expansion is vendor-specific, and is not described in this document.

Tx Lower Page (1010 000x) - Required		
Byte	**Type**	**Functions**
0-6	RO	Tx Status: 0xA8 presence, Flat/Paging memory presence, Interrupt, Data not Ready, Loss of Signal, Fault, Summary of Alarms
7-18	RO	Latched Tx Alarms: Loss of Signal, Fault, Per-channel Alarms (Power or Current high/low), Device alarms (temp, Vcc3.3 or Vcc12)
24-31	RO	Module Monitors: Temp, Voltage
40-41	RO	Module Monitor: Elapsed Operating Time
42-43	RW	Module Control: Rate / Application Select
53	RW	Module Control: Tx Reset
54-69	RW	Tx Channel Control: Disables, Squelch, Polarity Flip, Margin, Equalization control
97-108	RW	Masks for Alarms: Channel (LOS, Fault), Channel Internal (Power or Current high/low) and Module (Temp, Voltage)
109-118	RW	Vendor-Specific Area - Read/Write
119-126	RW	Password
127	RW	Upper Page Select Byte (00h or 01h)

Tx Upper Page 01h (Optional)		
Byte	**Type**	**Functions**
128-167	RO	Module Alarm Threshold Settings
168-179	RO	Channel Alarm Threshold Settings
180-181	RO	Checksum
182-229	RO	Per-Channel Monitors: Tx Bias current and light output
230-255		Reserved - Vendor-Specific Tx Functions

Upper Page 00h (Identical for Tx & Rx) Required		
Bytes	**Type**	**Functions**
128-129	RO	Identifiers
130-144	RO	Device Description: Cable & Connector, Power supplies, Max Case Temp, Min/Max Signal Rate, Laser wavelength or copper attenuation, and supported functions
147	RO	Description: Device Technology
152-222	RO	Vendor Information: Name & OUI, PN & PN rev, Serial number, Data code, & Customer-specific information
223	RO	Checksum on 128-222
224-255	RO	Vendor Specific Area - Read-only

Rx Lower Page (1010 100x) - Optional		
Byte	**Type**	**Functions**
0-6	RO	Rx Status: Flat/Paging memory, Interrupt, Data not Ready, Loss of Signal, Fault, Summary of Alarms
7-18	RO	Latched Rx Alarms: Loss of Signal, Fault, Per-channel Alarms (Power or Current high/low), Device alarms (temp, Vcc3.3 or Vcc12)
24-31	RO	Module Monitors: Temp, Voltage
40-41	RO	Module Monitor: Elapsed Operating Time
42-43	RW	Module Control: Rate / Application Select
53	RW	Module Control: Rx Reset
54-75	RW	Rx Channel Control: Disables, Squelch, Polarity Flip, Margin, Amplitude, Pre-emphasis control
97-108	RW	Masks for Alarms: Channel (LOS, Fault), Channel Internal (Power high/low) and Module (Temp, Voltage)
109-118	RW	Vendor Specific Area - Read/Write
119-126	RW	Password
127	RW	Upper Page Select Byte (00h or 01h)

Rx Upper Page 01h (Optional)		
Byte	**Type**	**Functions**
128-167	RO	Module Alarm Threshold Settings
168-179	RO	Channel Alarm Threshold Settings
180-181	RO	Checksum
182-253	RO	Per-Channel Monitors: Rx Input power
254-255		Reserved - Vendor-Specific Rx Functions

Figure 37 Memory Map 2-Wire Serial Addresses 1010 000x (Tx) & 1010 100x (Rx)

7.6.1 TX LOWER PAGE

Table 23 on page 73 describes the memory map for the Tx lower page.

Table 23 Tx Lower Page Memory Map

Byte	Bit	Name	Description	Type	Required/Optional/ - (Not Applicable)		
					Passive	Active copper	Active Optical
0 00h	All	Reserved - 1B	Coded 00h (unspecified)	RO			
1 01h	All	Reserved: Extended Status	00h	RO			
2 02h	7-4	Reserved	0000b	RO			
	3	Rx 0xA8 Device Address Presence	0 = Rx Device Address fields (0xA8) are present. 1 = Rx Device Address fields (0xA8) are not present		R	R	R
	2	Flat/Paging Memory Presence	0 = Paging is present. 1 = Upper Page 00h only, no other Tx Upper pages		R	R	R
	1	Int_L Status	Coded 1 for asserted Int_L. Clears to 0 when all flags including LOS and Fault are cleared.		R	R	R
	0	Data_Not_Ready	Indicates transceiver has not yet achieved power up and monitor data is not ready. Bit remains high until data is ready to be read at which time the device sets the bit low.		R	R	R
3-5	All	Reserved - 3B	Reserved for Status info	RO			
6 06h	7	LOS Tx Status Summary	Coded 1 when a LOS Tx flag (bytes 7-8) is asserted for any channel, else 0. Clears when LOS flags are cleared.	RO	-	O	O
	6	Reserved	Coded 0b. Reserved for Rx LOS Status Summary in Rx Lower Page				
	5	Fault Tx Status Summary	Coded 1 when a Fault Tx flag (bytes 9-10) is asserted for any channel, else 0. Clears when Fault flags are cleared.		-	O	O
	4	Bias Tx Status Summary	Coded 1 when a Tx Bias Hi-Lo Alarm (bytes 11-13) is asserted, else 0. Clears when alarm is cleared.		-	-	O
	3	Power Tx Status Summary	Coded 1 when a Tx Optical Power Hi-Lo Alarm (bytes 14-16) is asserted, else 0. Clears when alarm is cleared.		-	-	O
	2	Reserved	Coded 0b. Reserved for Rx Optical Power Hi-Lo Alarm in Rx Lower Page				
	1	Module Tx Status Summary	Coded 1 when any Tx Temperature or Voltage alarm (bytes 17-18) or reserved Module Tx monitor alarm (reserved in bytes 19-23) is asserted, else 0. Clears when Tx alarm is cleared.		-	O	O
	0	Reserved	Reserved for other Module Monitor alarm				

Table 23 Tx Lower Page Memory Map

Byte	Bit	Name	Description	Type	Required/Optional/ - (Not Applicable)		
					Passive	Active copper	Active Optical
7 07h	7-4	Reserved	Loss of Signal Tx Channel: Coded 1 when asserted, Latched, Clears on Read. Byte 7, bit 3 encodes for channel Tx11 Byte 7, bit 2 encodes for channel Tx10 Byte 7, bit 1 encodes for channel TX09 Byte 7, bit 0 encodes for channel Tx08 Byte 8, bits 7-0 encode for channels Tx07-Tx00 respectively. Following registers follow the same pattern	RO	-	O	O
	3-0	L-LOS Tx11 - Tx08					
8	7-0	L-LOS Tx07 - Tx00					
9 09h	7-4	Reserved	Fault Tx Channel: Coded 1 when asserted, Latched, Clears on Read.	RO	-	O	O
	3-0	L-Fault Tx11 - Tx08					
10	7-0	L-Fault Tx07 - Tx00					
11 0Bh	7-0	L-Bias Hi-Lo Alarm Tx11 - Tx08	Tx Optical Bias Hi-Lo Alarm Latched: 2 bits / channel Coded 10b when High Bias current alarm is asserted Coded 01b when Low Bias current alarm is asserted Coded 00b for no alarm. Latched, Clears on Read.	RO	-	-	O
12	7-0	L-Bias Hi-Lo Alarm Tx07 - Tx04					
13	7-0	L-Bias Hi-Lo Alarm Tx03 - Tx00					
14 0Eh	7-0	L-Power Hi-Lo Alarm Tx11 - Tx08	Tx Optical Power Hi-Lo Alarm Latched, 2 bits per channel Coded 10b when High Optical output power alarm is asserted Coded 01b when Low Optical output power alarm is asserted Coded 00b for no alarm. Latched, Clears on Read.	RO	-	-	O
15	7-0	L-Power Hi-Lo Alarm Tx07 - Tx04					
16 10h	7-0	L-Power Hi-Lo Alarm Tx03 - Tx00					
17 11h	7	L-Temp High Alarm - Tx	High Internal Temperature Alarm Latched: Coded 1 when asserted, Latched, Clears on Read.	RO	O	O	R
	6	L-Temp Low Alarm - Tx	Low Internal Temperature Alarm Latched: Coded 1 when asserted, Latched, Clears on Read.				
	5-0	Reserved					
18 12h	7	L-Vcc3.3 High Alarm - Tx	High Internal Vcc3.3 Alarm Latched: Coded 1 when asserted, Latched, Clears on Read.	RO	-	O	O
	6	L-Vcc3.3 Low Alarm - Tx	Low Internal Vcc3.3 Alarm Latched: Coded 1 when asserted, Latched, Clears on Read.				
	5-4	Reserved					
	3	L-Vcc12 High Alarm - Tx	High Internal Vcc12 Alarm Latched: Coded 1 when asserted, Latched, Clears on Read.		-	O	O
	2	L-Vcc12 Low Alarm - Tx	Low Internal Vcc12 Alarm Latched: Coded 1 when asserted, Latched, Clears on Read.				
	1-0	Reserved					
19-21	All	Reserved - 3B	Reserved - Module Alarms	RO			

Table 23 Tx Lower Page Memory Map

Byte	Bit	Name	Description	Type	Required/Optional/ - (Not Applicable)		
					Passive	Active copper	Active Optical
22 16h	All	1st Tx Temp Monitor MSB	1st Internal Temperature Monitor for Tx MSB: Integer part coded in signed 2's complement. Tolerance is ± 3°C.	RO	O	O	R
23 17h	All	1st Tx Temp Monitor LSB	1st Internal Temperature Monitor for Tx LSB: Fractional part in units of 1°/256 coded in binary.				
24-25	All	2nd Tx Temp Monitor	2nd Internal Temperature Monitor for Tx. Same 2 Byte format as 1st	RO	O	O	O
26-27 1A-1Bh	All	Tx Vcc3.3 Monitor MSB Tx Vcc3.3 Monitor LSB	Internal Vcc3.3 Monitor for Tx: Voltage in 100 μV units coded as 16 bit unsigned integer, Low byte is MSB. Tolerance is ± 0.10V.	RO	O	O	O
28-29 1C-1Dh	All	Tx Vcc12 Monitor MSB Tx Vcc12 Monitor LSB	Internal Vcc12 Monitor for Tx: Voltage in 100 μV units coded as 16 bit unsigned integer, Low byte is MSB. Tolerance is ± 0.1V.	RO	O	O	O
30-37	All	Reserved - 8B	Reserved - Module Monitors	RO			
38-39 26-27h	All	Elapsed Operating Time	Elapsed (Power-on) Operating Time: Elapsed time in 2 hour units coded as 16 bit unsigned integer, Low byte is MSB, Tolerance is ± 10%	RO	O	O	O
40 28h	All	Tx Module application select	Format to be determined as other applications besides InfiniBand arise	RW	-	O	O
41 29h	7-3	Reserved	Reserved - Rate Select	RW			
	2-0	Tx Rate Select	Tx Rate Select / optimization 000: no Info 001: SDR 010: DDR 011: DDR / SDR 100: QDR 101: QDR / SDR 110: QDR / DDR 111: QDR / DDR / SDR	RW	-	O	O
42 2Ah	7-1	Reserved		RW	O	O	O
	0	High-Power Mode	0: Device or cable may not draw more than 6 Watts of power. 1: Device or cable may draw more than 6.0 W, up to limit denoted in Upper Page 00, Byte 148(94h)				
43-50	All	Reserved - 8B	Reserved - Module Control	RW			
51 33h	7-1	Reserved		RW			
	0	Reset	Reset: Writing 1 return all registers on Tx pages (non-volatile RW, if present in vendor-specific area) to factory default values. Reads 0 after operation.		R	R	R

Table 23 Tx Lower Page Memory Map

Byte	Bit	Name	Description	Type	Required/Optional/ - (Not Applicable)		
					Passive	Active copper	Active Optical
52	7-4	Reserved	Tx Channel Disable: Writing 1 disables the whole channel, Default is 0.	RW	-	O	O
34h	3-0	Channel Disable Tx11 - Tx08					
53	7-0	Channel Disable Tx07 - Tx00					
54	7-4	Reserved	Tx Output Disable: Writing 1 disables just the output for the channel. Default is 0 (Squelch enabled).	RW	-	O	O
36h	3-0	Output Disable Tx11 - Tx08					
55	7-0	Output Disable Tx07 - Tx00					
56	7-4	Reserved	Tx Squelch Disable: Writing 1 disables squelch for the channel. Default is 0 (Squelch enabled).	RW	-	O	O
38h	3-0	Squelch Disable Tx11-Tx08					
57	7-0	Squelch Disable Tx07 - Tx00					
58	7-4	Reserved	Tx Channel input polarity flip: Writing 1 inverts the polarity of outputs relative to the inputs. Default is 0 (No polarity flip)	RW	-	O	O
3Ah	3-0	Polarity flip Tx11 - Tx08					
59	7-0	Polarity flip Tx07 - Tx00					
60	7-4	Reserved	Tx Channel Margin Activation: Writing 1 places Tx in "Margin Mode" - reduces signal integrity (electrical) or OMA (optical) by equivalent of ~1 dB. Default is 0.	RW	-	O	O
3Ch	3-0	Margin Select Tx11 - Tx08					
61	7-0	Margin Select Tx07 - Tx00					
62	7-4	Input Equalization Tx11	Tx Input Equalization Control: Four bit code blocks (bits 7-4 or 3-0) are assigned to each channel. Codes 1xxxb are reserved. Writing 0111b calls for full-scale equalization. Writing 0000b calls for no equalization. Intermediate code values call for intermediate levels of equalization. Exact equalization parameters (e.g., crossover frequency, equalization levels, slopes vs. frequency, etc.) are vendor-specific, and shall be appropriate to the intended use of the module or device.	RW	-	O	O
3Eh	3-0	Input Equalization Tx10					
63	7-4	Input Equalization Tx09					
3Fh	3-0	Input Equalization Tx08					
64	7-4	Input Equalization Tx07					
40h	3-0	Input Equalization Tx06					
65	7-4	Input Equalization Tx05					
41h	3-0	Input Equalization Tx04					
66	7-4	Input Equalization Tx03					
42h	3-0	Input Equalization Tx02					
67	7-4	Input Equalization Tx01					
43h	3-0	Input Equalization Tx00					

Table 23 Tx Lower Page Memory Map

Byte	Bit	Name	Description	Type	Required/Optional/ - (Not Applicable)		
					Passive	Active copper	Active Optical
68-94	All	Reserved - 27B	Reserved - Per-Channel Control	RW			
95 5Fh	7-4	Reserved	Mask Tx LOS Flag: Writing 1 prevents Int_L on Tx LOS. Default = 0	RW	-	O	O
	3-0	Mask LOS Flag Tx11 - Tx08					
96	7-0	Mask LOS Flag Tx07 - Tx00					
97 61h	7-4	Reserved	Mask Tx Fault Flag: Writing 1 prevents Int_L on Tx Fault. Default = 0	RW	-	O	O
	3-0	Mask Tx Fault Flag Tx11 - Tx08					
98	7-0	Mask Tx Fault Flag Tx07 - Tx00					
99 63h	7-0	Mask Bias Hi-Lo Alarm Tx11 - Tx08	Mask Tx Bias Current Hi-Lo Alarm: Writing 10b prevents Int_L on Tx High Bias Current Writing 01b prevents Int_L on Tx Low Bias Current Writing 11b prevents Int_L on both High and Low Bias Current Alarms. Default = 00b	RW	-	-	O
100 64h	7-0	Mask Bias Hi-Lo Alarm Tx07 - Tx04					
101 65h	7-0	Mask Bias Hi-Lo Alarm Tx03 - Tx00					
102 66h	7-0	Mask Pwr Hi-Lo Alarm Tx11 - Tx08	Mask Tx Optical Power Hi-Lo Alarm: Writing 10b prevents Int_L on Tx High Optical Power Writing 01b prevents Int_L on Tx Low Optical Power Writing 11b prevents Int_L on both High and Low Optical Power alarms. Default = 00b	RW	-	-	O
103 67h	7-0	Mask Pwr Hi-Lo Alarm Tx07 - Tx04					
104 68h	7-0	Mask Pwr Hi-Lo Alarm Tx03 - Tx00					

Table 23 Tx Lower Page Memory Map

Byte	Bit	Name	Description	Type	Required/Optional/ - (Not Applicable)		
					Passive	Active copper	Active Optical
105 69h	7	Mask Temp High Alarm - Tx	Mask High Internal Temperature Alarm: Writing 1 prevents Int_L on High Tx Internal temperature. Default = 0	RW	O	O	O
	6	Mask-Temp Low Alarm - Tx	Mask Low Internal Temperature Alarm: Writing 1 prevents Int_L on Low Tx internal temperature. Default = 0				
	5-0	Reserved					
106 6Ah	7	Mask Vcc3.3-Tx High Alarm	Mask High Internal 3.3 Vcc Alarm: Writing 1 prevents Int_L on High Vcc3.3-Tx Voltage alarm. Default = 0	RW	O	O	O
	6	Mask Vcc3.3-Tx Low Alarm	Mask Low Internal 3.3 Vcc Alarm: Writing 1 prevents Int_L on Low Vcc3.3-Tx Voltage alarm. Default = 0		O	O	O
	5-4	Reserved					
	3	Mask Vcc12-Tx High Alarm	Mask High Internal Vcc12 Alarm: Writing 1 prevents Int_L on High Vcc12-Tx Voltage alarm. Default = 0.		O	O	O
	2	Mask Vcc12-Tx Low Alarm	Mask Low Internal Vcc12 Alarm: Writing 1 prevents Int_L on Low Vcc12-Tx Voltage alarm. Default = 0		O	O	O
	1-0	Reserved					
107-109		Reserved - 3B	Reserved - Masks for Module Alarms	RW			
110-118 6Eh-76h	All	Vendor Specific - 9B	Vendor Specific Read-Write Registers for Tx	RW			
119-122 77h-7Ah	All	Password Change Entry Area	Password Change Entry Area	RW	O	O	O
123-126 7Bh-7Eh		Password Entry Area	Password Entry Area	RW	O	O	O
127 7Fh	All	Page Select Byte	Selects Upper Page - Required if paging is used on upper page(s). Not required if paging is not used. Writing 00h selects Tx & Rx Upper Page 00h Writing 01h selects Tx Upper Page 01h, etc.	RW	See note at left.		

7.6.2 RX LOWER PAGE

Table 24 on page 79 describes the memory map for the Rx lower page. This page is optional, and may not be implemented on simple modules or devices such as passive cables.

Table 24 Rx Lower Page Memory Map (Optional)

Byte	Bit	Name	Description	Type	Required/Optional/ - (Not Applicable)		
					Passive	Active copper	Active Optical
0 00h	All	Reserved - 1B	Coded 00h (unspecified)	RO			
1 01h	All	Reserved: Extended Status	00h	RO			
2 02h	7-4	Reserved	0000b	RO			
	3	Reserved	0 - used in Tx Lower Page to indicate presence of Rx				
	2	Flat/Paging Memory Presence	0 = Paging is present. 1 = Upper Page 00h only, no other Rx Upper pages		R	R	R
	1	Int_L Status	Coded 1 for asserted Int_L. Clears to 0 when all flags are cleared.		O	R	R
	0	Data_Not_Ready	Indicates transceiver has not yet achieved power up and monitor data is not ready. Bit remains high until data is ready to be read at which time the device sets the bit low.		O	R	R
3-5	All	Reserved - 3B	Reserved for Status info	RO			
6 06h	7	Reserved - 1b	Coded 0b. Reserved for Tx status info	RO			
	6	LOS Rx Status Summary	Coded 1 when a LOS Rx flag (bytes 9-10) is asserted for any channel, else 0. Clears when Fault flags are cleared.		-	O	O
	5-3	Reserved	Coded 000b. Reserved for Tx status info				
	2	Power Rx Status Summary	Coded 1 when a Rx Optical Power Hi-Lo Alarm (bytes 19-21) is asserted, else 0. Clears when alarm is cleared.		-	-	O
	1	Module Rx Status Summary	Coded 1 when any Rx Temperature or Voltage alarm (bytes 17-18) or reserved Module Rx monitor alarm (reserved in bytes 19-23) is asserted, else 0. Clears when Rx alarm is cleared.		-	O	O
	0	Reserved	Reserved for other Module Monitor alarm				

Table 24 Rx Lower Page Memory Map (Optional)

Byte	Bit	Name	Description	Type	Required/Optional/ - (Not Applicable)		
					Passive	Active copper	Active Optical
7 07h	7-4	Reserved	Loss of Signal Rx Channel: Coded 1 when asserted, Latched, Clears on Read.	RO	-	O	O
	3-0	L-LOS Rx11 - Rx08					
8	7-0	L-LOS Rx07 - Rx00					
9 09h	7-4	Reserved	Fault Rx Channel: Coded 1 when asserted, Latched, Clears on Read.	RO	-	O	O
	3-0	L-Fault Rx11 - Rx08					
10	7-0	L-Fault Rx07 - Rx00					
11-13	All	Reserved - 3B	Reserved - Module Alarms - used in Tx Lower Page for Optical Bias Current Hi-Lo alarms	RO			
14 0Eh	7-0	L-Power Hi-Lo Alarm Rx11 - Rx08	Rx Optical Power Hi-Lo Alarm Latched: Coded 10 when asserted for High Rx Optical power alarm, Coded 01 when asserted for Low Rx optical power alarm. Latched, Clears on Read.	RO	-	-	O
15	7-0	L-Power Hi-Lo Alarm Rx07 - Rx04					
16 10h	7-0	L-Power Hi-Lo Alarm Rx03 - Rx00					
17 11h	7	L-Temp High Alarm - Rx	High Internal Temperature Alarm Latched: Coded 1 when asserted, Latched, Clears on Read.	RO	-	-	O
	6	L-Temp Low Alarm - Rx	Low Internal Temperature Alarm Latched: Coded 1 when asserted, Latched, Clears on Read.		-	-	O
	5-0	Reserved					
18 12h	7	L-Vcc3.3 High Alarm - Rx	High Internal Vcc3.3 Alarm Latched: Coded 1 when asserted, Latched, Clears on Read.	RO	O	O	O
	6	L-Vcc3.3 Low Alarm - Rx	Low Internal Vcc3.3 Alarm Latched: Coded 1 when asserted, Latched, Clears on Read.				
	5-4	Reserved					
	3	L-Vcc12 High Alarm - Rx	High Internal Vcc12 Alarm Latched: Coded 1 when asserted, Latched, Clears on Read.		O	O	O
	2	L-Vcc12 Low Alarm - Rx	Low Internal Vcc12 Alarm Latched: Coded 1 when asserted, Latched, Clears on Read.				
	1-0	Reserved					
19-21	All	Reserved - 3B	Reserved - Module Alarms	RO			

Table 24 Rx Lower Page Memory Map (Optional)

Byte	Bit	Name	Description	Type	Required/Optional/ - (Not Applicable)		
					Passive	Active copper	Active Optical
22 16h	All	1st Rx Temp Monitor MSB	1st Internal Temperature Monitor for Rx MSB: Integer part coded in signed 2's complement. Tolerance is ± 3°C.	RO	O	O	O
23 17h	All	1st Rx Temp Monitor LSB	1st Internal Temperature Monitor for Rx LSB: Fractional part in units of 1°/256 coded in binary.				
24-25	All	2nd Rx Temp Monitor	2nd Internal Temperature Monitor for Rx. Same 2 Byte format as 1st	RO	O	O	O
26-27 1A-1Bh	All	Rx Vcc3.3 Monitor MSB Rx Vcc3.3 Monitor LSB	Internal Vcc3.3 Monitor for Rx: Voltage in 100 μV units coded as 16 bit unsigned integer, Low byte is MSB. Tolerance is ± 0.10V.	RO	O	O	O
28-29 1C-1Dh	All	Rx Vcc12 Monitor MSB Rx Vcc12 Monitor LSB	Internal Vcc12 Monitor for Rx: Voltage in 100 μV units coded as 16 bit unsigned integer, Low byte is MSB. Tolerance is ± 0.1V.	RO	O	O	O
30-37	All	Reserved - 8B	Reserved - Module Monitors	RO			
38-39 26h-27h	All	Elapsed Operating Time	Elapsed (Power-on) Operating Time: Elapsed time in 2 hour units coded as 16 bit unsigned integer, Low byte is MSB, Tolerance is ± 10%	RO	O	O	O
40 28h	All	Rx module application select	Format to be determined as other applications besides InfiniBand arise	RW	-	O	O
41 29h	7-3	Reserved	Reserved - Rate Select	RW			
	2-0	Rx Rate Select	Rx Rate Select / optimization 000: no Info 001: SDR 010: DDR 011: DDR / SDR 100: QDR 101: QDR / SDR 110: QDR / DDR 111: QDR / DDR / SDR	RW	-	O	O
42 2Ah	All	Reserved	Used in Tx Lower Page to manage devices with >6.0 Watt power utilization	RW			
43-50	All	Reserved - 8B	Reserved - Module Control	RW			
51 33h	7-1	Reserved		RW			
	0	Reset - Rx	Reset: Writing 1 return all registers on Rx pages (except any vendor-specific non-volatile RW areas) to factory default values. Reads 0 after operation.		R	R	R

Table 24 Rx Lower Page Memory Map (Optional)

Byte	Bit	Name	Description	Type	Required/Optional/ - (Not Applicable)		
					Passive	Active copper	Active Optical
52	7-4	Reserved	Rx Channel Disable: Writing 1 disables the whole channel. Default is 0.	RW	-	O	O
34h	3-0	Channel Disable Rx11 - Rx08					
53	7-0	Channel Disable Rx07 - Rx00					
54	7-4	Reserved	Rx Output Disable: Writing 1 disables only the output for the channel. Default is 0 (Output enabled).	RW	-	O	O
36h	3-0	Output Disable Rx11 - Rx08					
55	7-0	Output Disable Rx07 - Rx00					
56	7-4	Reserved	Rx Squelch Disable: Writing 1 disables squelch for the channel. Default is 0 (Squelch enabled).	RW	-	O	O
38h	3-0	Squelch Disable Rx11 - Rx08					
57	7-0	Squelch Disable Rx07 - Rx00					
58	7-4	Reserved	Rx Channel Polarity Flip: Writing 1 inverts the polarity of outputs relative to inputs. Default is 0 (No polarity flip)	RW	-	O	O
3Ah	3-0	Polarity flip Rx11 - Rx08					
59	7-0	Polarity flip Rx07 - Rx00					
60	7-4	Reserved	Rx Channel Margin Activation: Writing 1 places Rx in “Margin Mode” - reduces receiver sensitivity by equivalent of ~1 dB. Default is 0.	RW	-	O	O
3Ch	3-0	Margin Select Rx11 - Rx08					
61	7-0	Margin Select Rx07 - Rx00					
62	7-4	Output Amplitude Rx11	Rx Output Amplitude Control: Four bit code blocks (bits 7-4 or 3-0) are assigned to each channel. Codes 1xxxb are reserved. Writing 0111b calls for full-scale signal amplitude. Writing 0000b calls for minimum signal amplitude. Writing intermediate code values calls for intermediate levels of signal amplitude.	RW	-	O	O
3Eh	3-0	Output Amplitude Rx10					
63	7-4	Output Amplitude Rx09					
3Fh	3-0	Output Amplitude Rx08					
64	7-4	Output Amplitude Rx07					
40h	3-0	Output Amplitude Rx06					
65	7-4	Output Amplitude Rx05					
41h	3-0	Output Amplitude Rx04					
66	7-4	Output Amplitude Rx03					
42h	3-0	Output Amplitude Rx02					
67	7-4	Output Amplitude Rx01					
43h	3-0	Output Amplitude Rx00					

Table 24 Rx Lower Page Memory Map (Optional)

Byte	Bit	Name	Description	Type	Required/Optional/ - (Not Applicable)		
					Passive	Active copper	Active Optical
68 44h	7-4	Output Pre-Emphasis Rx11	Rx Output Pre-Emphasis Control: Four bit code blocks (bits 7-4 or 3-0) are assigned to each channel. Codes 1xxxb are reserved. Writing 0111b calls for full-scale pre-emphasis. Writing 0000b calls for minimum pre-emphasis. Writing intermediate code values calls for intermediate levels of pre-emphasis.	RW	-	O	O
	3-0	Output Pre-Emphasis Rx10					
69 45h	7-4	Output Pre-Emphasis Rx09					
	3-0	Output Pre-Emphasis Rx08					
70 46h	7-4	Output Pre-Emphasis Rx07					
	3-0	Output Pre-Emphasis Rx06					
71 47h	7-4	Output Pre-Emphasis Rx05					
	3-0	Output Pre-Emphasis Rx04					
72 48h	7-4	Output Pre-Emphasis Rx03					
	3-0	Output Pre-Emphasis Rx02					
73 49h	7-4	Output Pre-Emphasis Rx01					
	3-0	Output Pre-Emphasis Rx00					
74-94	All	Reserved - 21B	Reserved - Per-Channel Control	RW			
95 5Fh	7-4	Reserved	Mask Rx LOS Alarm: Writing 1 prevents Int_L on Loss of Signal, Default = 0	RW	-	O	O
	3-0	Mask LOS Rx11 - Rx08					
96	7-0	Mask LOS Rx07 - Rx00					
97-98	All	Reserved - 2B	Reserved - Per Module Mask	RW			
99-101	All	Reserved - 3B	Reserved - Per Channel Mask	RW			
102 66h	7-0	Mask Pwr Hi-Lo Alarm Rx11 - Rx08	Mask Rx Optical Power Hi-Lo Alarm Writing 10b prevents Int_L on High Rx Optical Power Writing 01b prevents Int_L on Low Rx optical Power Writing 11b prevents Int_L for both High and Low Rx Optical Power alarms. Default = 00b	RW	-	-	O
103 67h	7-0	Mask Pwr Hi-Lo Alarm Rx07 - Rx04					
104 68h	7-0	Mask Pwr Hi-Lo Alarm Rx03 - Rx00					

Table 24 Rx Lower Page Memory Map (Optional)

Byte	Bit	Name	Description	Type	Required/Optional/ - (Not Applicable)		
					Passive	Active copper	Active Optical
105 69h	7	Mask Temp High Alarm	Mask High Internal Temperature Alarm: Writing 1 prevents Int_L on High Module Temperature alarm. Default = 0	RW	O	O	O
	6	Mask-Temp Low Alarm	Mask Low Internal Temperature Alarm: Writing 1 prevents Int_L on Low Module Temperature alarm. Default = 0				
	5-0	Reserved					
106 6Ah	7	Mask Vcc3.3-Rx High Alarm	Mask High Internal 3.3 Vcc Alarm: Writing 1 prevents Int_L on High Vcc3.3-Rx alarm. Default = 0	RW	O	O	O
	6	Mask Vcc3.3-Rx Low Alarm	Mask Low Internal 3.3 Vcc Alarm: Writing 1 prevents Int_L on Low Vcc3.3-Rx alarm. Default = 0		O	O	O
	5-4	Reserved					
	3	Mask Vcc12-Rx High Alarm	Mask High Internal Vcc12 Alarm: Writing 1 prevents Int_L on High Vcc12-Rx alarm. Default = 0.		O	O	O
	2	Mask Vcc12-Rx Low Alarm	Mask Low Internal Vcc12 Alarm: Writing 1 prevents Int_L on Low Vcc12-Rx alarm. Default = 0		O	O	O
	1-0	Reserved					
107-109		Reserved - 3B	Reserved - Masks for Module Alarms	RW			
110-118 6Eh-76h	All	Vendor Specific - 9B	Vendor Specific Read-Write Registers for Rx	RW			
119-126 77h-7Eh	All	Reserved - 8B	Reserved - compatibility with Tx page Password field	RW			
127 7Fh	All	Page Select Byte	Selects Upper Page - Required if paging is used on upper page(s). Not required if paging is not used. Writing 00h selects Tx & Rx Upper Page 00h Writing 01h selects Rx Upper Page 01h, etc.	RW	See note at left.		

7.6.3 TX & RX COMMON UPPER PAGE 00H

Table 25 on page 85 shows the memory map for the first upper page, page 00h, for both Tx and Rx addresses.

Table 25 Tx & Rx Upper Page 00h Memory Map

Byte	Bit	Name	Description	Type	Required/Optional/ - (Not Applicable)		
					Passive	Active copper	Active Optical
128 80h	All	Reserved - Type Identifier	Reserved for SFF-style Type Identifier code for CXP - probably either 0Eh or 0Fh, TBD	RO			
129 81h	7-5	Power Class	000: 0.25W max - Class 0 001: 1.0W max - Class 1 010: 1.5W max - Class 2 011: 2.5W max - Class 3 100: 4.0W max - Class 4 101: 6.0W max - Class 5 110: >6.0W - Class 6 111: Reserved	RO	R	R	R
	4	Tx CDR Presence	Coded 1 for Tx CDR (clock & data recovery) provided; else coded 0		R	R	R
	3	Rx CDR Presence	Coded 1 for Rx CDR provided; else coded 0		R	R	R
	2-0	Reserved					
130 82h	All	Connector / Cable	00h-0Ch: Not compatible w/CXP, Rsvd.-compatibility 0Dh-1Fh: Reserved 20h-23h: Rsvd.-compatibility 24h-2Fh: Reserved 30h: Passive Copper Cable Assembly 31h: Active Copper Cable Assembly (ref. Byte 147) 32h: Active Optical Cable Assembly 33h: Optical Transceiver w/ optical connector 34h-7Fh: Reserved 80h-FFh: Vendor Specific	RO	-	R	R
131 83h	7	1	3.3V - Vcc3.3 - Coded 1 if required for the module	RO	R	R	R
	6-4	000b - Reserved	2.5V, 1.8V, Vo supplies - not available in receptacle				
	3	1	12V - Vcc12 - Coded 1 if required for the module		R	R	R
	2-0	000b - Reserved					
132 84h	All	Max Temperature	Maximum Recommended Operating Case Temperature for the module, in Degrees C	RO	R	R	R
133 85h	All	Min per-channel bit rate	Min signal rate = binary value x 100 Mb/s (e.g., 25 (00011001b) = 2500 Mb/s, & 100 (01100100b) = 10,000 Mb/s)	RO	-	R	R
134 86h	All	Max per-channel bit rate	Max signal rate = binary value x 100 Mb/s	RO	-	R	R

Table 25 Tx & Rx Upper Page 00h Memory Map

Byte	Bit	Name	Description	Type	Required/Optional/ - (Not Applicable)		
					Passive	Active copper	Active Optical
135-136 87h-88h	All	Optical: Laser Wavelength Copper: Attenuation	**Optical**: Nominal Laser Wavelength -- Wavelength in nm = value / 20): e.g.,42h 04h = 16,900, 16,900/20 = 845 nm **Copper**: Nominal attenuation of cable either to the other end (passive) or to equalizer (active) Byte 135: Attenuation at 2.5 GHz in dB - 00h=no info Byte 136: Attenuation at 5 GHz in dB - 00h=no info	RO	R	R	R
137-138 89-8Ah	All	Optical: Max Wavelength Deviation Copper: Attenuation Extended	**Optical**: Wavelength tolerance (max deviation from nominal) Wavelength tolerance in nm = +/- value / 200): e.g., 0Bh BBh = 3003, 3003/200= 15 nm **Copper**: Nominal attenuation- extended Byte 137: Attenuation at 10 GHz in dB - 00h=no info Byte 138: Tolerance of nominal attenuation at Max per-channel bit rate (Byte 134)	RO	R	R	R
139 8Bh	7	Support for Tx Fault	Coded 1 if Tx Fault Flag supported, else coded 0	RO	R	R	R
	6	Support for Rx Fault	Coded 1 if Rx Fault Flag supported, else coded 0		R	R	R
	5	Support for Tx LOS	Coded 1 if Tx Loss of Signal Flag supported, else coded 0		R	R	R
	4	Support for Rx LOS	Coded 1 if Rx Loss of Signal Flag supported, else coded 0		R	R	R
	3	Support for Tx Squelch	Coded 1 if Tx Squelch supported, else 0		R	R	R
	2	Support for Rx Squelch	Coded 1 if Rx Squelch supported, else 0		R	R	R
	1	Support for Tx CDR LOS	Coded 1 if Tx CDR Loss of Sync Flag supported, else coded 0		R	R	R
	0	Support for Rx CDR LOS	Coded 1 if Rx CDR Loss of Sync Flag supported, else coded 0		R	R	R
140 8Ch	7	Support for Tx Bias Monitor	Coded 1 if Tx Bias Monitor supported, else coded 0	RO	R	R	R
	6	Support for Tx LOP Monitor	Coded 1 if Tx Light Output Power Monitor supported, else coded 0		R	R	R
	5	Support for Rx Input Power Monitor	Coded 1 if individual Rx Input Power Monitors supported, coded 0 for single-channel or group monitor		R	R	R
	4	Support for Rx Input Power Format	Coded 1 if Rx Input Power reported as Pave, coded 0 for reported as OMA		R	R	R
	3	Support for Case Temp Monitor	Coded 1 if Case Temperature Monitor supported, else coded 0		R	R	R
	2	Support for Internal Temp Monitor	Coded 1 if Internal Temperature Monitor supported, else coded 0		R	R	R
	1	Support for Peak Temp Monitor	Coded 1 if Peak Temperature Monitor supported, else coded 0		R	R	R
	0	Support for Elapsed Time Monitor	Coded 1 if Elapsed PowerOn Operating Time Monitor supported, else coded 0		R	R	R

Table 25 Tx & Rx Upper Page 00h Memory Map

Byte	Bit	Name	Description	Type	Required/Optional/ - (Not Applicable)		
					Passive	Active copper	Active Optical
141 8Dh	7	BER Monitor	Coded 1 for BER Monitor, else coded 0	RO	R	R	R
	6	Vcc3.3-Tx Monitor	Coded 1 for Internal Vcc3.3-Tx Monitor, else coded 0		R	R	R
	5	Vcc3.3-Rx Monitor	Coded 1 for Internal Vcc3.3-Rx Monitor, else coded 0		R	R	R
	4	Vcc12-Tx Monitor	Coded 1 for Internal Vcc12-Tx Monitor, else coded 0		R	R	R
	3	Vcc12-Rx Monitor	Coded 1 for Internal Vcc12-Rx Monitor, else coded 0		R	R	R
	2	TEC Current Monitor	Coded 1 for TEC current Monitor, else coded 0		R	R	R
	1-0	Reserved					
142 8Eh	7-6	Tx Channel Disable Capabilities	00: Not provided, or unspecified 01: Global Tx Channel Disable Control implemented 10: Individual & independent Tx Channel Disable Control implemented 11: Reserved	RO	R	R	R
	5-4	Tx Channel Output Disable Capabilities	00: Not provided, or unspecified 01: Tx Global Channel Output Disable Control implemented 10: Individual & independent Tx Channel Output Disable Control implemented 11: Reserved		R	R	R
	3-2	Tx Squelch Disable Capabilities	00: Not provided, or unspecified 01: Global Tx Squelch Disable Control implemented 10: Individual and independent Tx Channel Disable Control implemented 11: Reserved		R	R	R
	1	Tx Polarity Flip Mode	Coded 1 for Tx Channel Polarity Flip Control provided, else coded 0		R	R	R
	0	Tx Margin Mode	Coded 1 for Tx Margin Mode provided, else coded 0		R	R	R
143 8Fh	7-4	Reserved		RO			
	3-2	Tx Input Equalization Control	00: Not provided, or unspecified 01: Global Tx Input Equalization Control implemented 10: Individual and independent Tx Input Equalization Control implemented 11: Reserved		R	R	R
	1-0	Tx Rate Select Control	00: Not provided, or unspecified 01: Global Tx Rate/Application Select Control implemented 10: Reserved (Individual and independent Tx Rate/Application Select control not available except in vendor-specific manner). 11: Reserved		R	R	R

Table 25 Tx & Rx Upper Page 00h Memory Map

Byte	Bit	Name	Description	Type	Required/Optional/ - (Not Applicable)		
					Passive	Active copper	Active Optical
144 90h	7-6	Rx Channel Disable Capabilities	00: Not provided, or unspecified 01: Global Rx Channel Disable Control implemented 10: Individual & independent Rx Channel Disable Control implemented 11: Reserved	RO	R	R	R
	5-4	Rx Channel Output Disable Capabilities	00: Not provided, or unspecified 01: Rx Global Channel Output Disable Control implemented 10: Individual & independent Rx Channel Output Disable Control implemented 11: Reserved		R	R	R
	3-2	Rx Squelch Disable Capabilities	00: Not provided, or unspecified 01: Global Rx Squelch Disable Control implemented 10: Individual and independent Rx Channel Disable Control implemented 11: Reserved		R	R	R
	1	Rx Polarity Flip Mode	Coded 1 for Rx Channel Polarity Flip Control provided, else coded 0		R	R	R
	0	Rx Margin mode	Coded 1 for Rx Margin Mode provided, else coded 0		R	R	R
145 91h	7-6	Reserved		RO			
	5-4	Rx Output Equalization Control	00: Not provided, or unspecified 01: Global Rx Output Equalization Control implemented 10: Individual and independent Rx Output Equalization Control implemented 11: Reserved		R	R	R
	3-2	Rx Output De-Emphasis Control	00: Not provided, or unspecified 01: Global Rx Output De-Emphasis Control implemented 10: Individual and independent Rx Output De-Emphasis Control implemented 11: Reserved		R	R	R
	1-0	Rx Rate Select Control	00: Not provided, or unspecified 01: Global Rx Rate/Application Select Control implemented 10: Reserved (Individual and independent Rx Rate/Application Select control not available except in vendor-specific manner). 11: Reserved		R	R	R

Table 25 Tx & Rx Upper Page 00h Memory Map

Byte	Bit	Name	Description	Type	Required/Optional/ - (Not Applicable)		
					Passive	Active copper	Active Optical
146 92h	7	FEC Control	Coded 1 for FEC Control, else coded 0	RO	R	R	R
	6	PEC Control	Coded 1 for PEC Control, else coded 0		R	R	R
	5	JTAG Control	Coded 1 for JTAG Control, else coded 0		R	R	R
	4	AC-JTag Control	Coded 1 for AC-JTAG Control, else coded 0		R	R	R
	3	BIST	Coded 1 for BIST, else coded 0		R	R	R
	2	TEC Temperature Control	Coded 1 for TEC Temperature Control, else coded 0		R	R	R
	1	Speed Mode Set Control	Coded 1 for Sleep Mode Set Control provided, else coded 0		R	R	R
	0	CDR Bypass Control	Coded 1 for CDR Bypass Control provided, else coded 0		R	R	R
147 93h	7-4	Device Technology	0000: 850 nm VCSEL 0001:1310 nm VCSEL 0010:1550 nm VCSEL 0011: 1310 nm FP 0100:1310 nm DFB 0101:1550 nm DFB 0110: 1310 nm EML 0111: 1550 nm EML 1000: Copper or others 11001: 1490 nm DFB 1010: Copper cable un-equalized 1011: Copper cable passive equalized 1100: Copper cable near & far end active equalizers 1101: Copper cable, far end active equalizer 1110: copper cable, near end active equalizer 1111: Reserved	RO	R	R	R
	3	Wavelength Control	0: No control 1: Active wavelength control		-	-	R
	2	Transmitter cooling	0: Uncooled transmitter, 1: Cooled transmitter		-	-	R
	1	Optical Detector	0: P-I-N Detector 1: APD detector		-	-	R
	0	Optical Tunability	0: Transmitter not tunable, 1:Transmitter tunable		-	-	R
148 94h	All	Max Power Utilization	Maximum power utilization, in units of 0.1 Watts. Range: 0.1W - 25.5 Watts 00h: No information	RO	R	R	R
149 95h	7-1	Reserved	Coded 1 for 12x to 3-4x Cable, else, for regular cable without fanout, coded 0	RO	R	R	R
	0	12x to 3-4x					
150-151 96h-97h	All	Reserved		RO			

Table 25 Tx & Rx Upper Page 00h Memory Map

Byte	Bit	Name	Description	Type	Required/Optional/ - (Not Applicable)		
					Passive	Active copper	Active Optical
152-167 98h-A7h	All	Vendor Name	Vendor name in ASCII - 16B	RO	R	R	R
168-170 A8-AAh	All	Vendor OUI	Vendor OUI (IEEE ID): Organization-Unique Identifier - 3B	RO	R	R	R
171-186 AB-BAh	All	Vendor Part Number	Vendor Part Number in ASCII - 16B	RO	R	R	R
187-188 BBh-BCh	All	Vendor Rev. Number	Vendor Revision Number in ASCII - 2B	RO	O	O	O
189-204 BDh-CCh	All	Vendor Serial Number	Vendor Serial Number (ASCII): Varies by unit - 16B	RO	O	O	O
205-212 CD-D4h	All	Vendor Date Code	Vendor Date Code YYYYMMDD (ASCII): Spaces (20h) for unused characters	RO	O	O	O
213-222 215-DEh	All	Lot Code	Customer-Specific Code or Vendor-Specific lot code (ASCII). 10B. All spaces (20h) if unused	RO	O	O	O
223 DFh		Checksum	Checksum of addresses 128 through 222 inclusive: 8 low-order bits of sum	RO	R	R	R
224-255 E0-EFh		Vendor Specific - 32B	Vendor Specific Read-Only Registers	RO	O	O	O

7.6.4 TX UPPER PAGE 01H

Table 26 on page 91 shows the memory map for the Tx upper page 01h

Table 26 Tx Upper Page 01h Memory Map

Byte	Bit	Name	Description	Type	Required/Optional/ - (Not Applicable)		
					Passive	Active copper	Active Optical
128 80h	All	Hi Alarm Threshold for 1st Tx Temperature Monitor MSB	Hi Alarm Threshold for 1st Internal Temperature Monitor for Tx MSB: Integer part coded in signed 2's complement. Tolerance is ± 3°C.	RO	O	R	R
129 81h	All	Hi Alarm Threshold for 1st Tx Temperature Monitor LSB	Hi Alarm Threshold for 1st Internal Temperature Monitor for Tx LSB: Fractional part in units of 1°/256 coded in binary.				
130-131 82h-83h	All	Lo Alarm Threshold 1st Tx MonitorTemp	Lo Alarm Threshold for 1st Internal Temperature Monitor for Tx. Same 2 Byte format as 128-129	RO	O	R	R
132-133 84h-85h	All	Hi Alarm Threshold 2nd Tx MonitorTemp	Hi Alarm Threshold for 2nd Internal Temperature Monitor for Tx. Same 2 Byte format	RO	O	O	O
134-135 86h-87h	All	Lo Alarm Threshold 2nd Tx MonitorTemp	Lo Alarm Threshold for 2nd Internal Temperature Monitor for Tx. Same 2 Byte format	RO	O	O	O
136-143 88h-8Fh	All	Reserved - 8B	Reserved - Alarm Thresholds for Module Monitors				
144-145 90h-91h	All	Hi Alarm Threshold Tx Vcc3.3 Monitor	Hi Alarm Threshold for Internal Vcc3.3 Monitor for Tx: Voltage in 100 μV units coded as 16 bit unsigned integer, Low byte is MSB.	RO	-	O	O
146-147 92h-93h	All	Lo Alarm Threshold Tx Vcc3.3 Monitor	Lo Alarm Threshold for Internal Vcc3.3 Monitor for Tx: Voltage in 100 μV units coded as 16 bit unsigned integer, Low byte is MSB.	RO	-	O	O
148-149 94h-95h	All	Hi Alarm Threshold Tx Vcc12-Monitor	Hi Alarm Threshold for Internal Vcc12 Monitor for Tx: Voltage in 100 μV units coded as 16 bit unsigned integer, Low byte is MSB.	RO	-	O	O
150-151 96h-97h	All	Lo Alarm Threshold Tx Vcc12 Monitor	Lo Alarm Threshold for Internal Vcc12 Monitor for Tx: Voltage in 100 μV units coded as 16 bit unsigned integer, Low byte is MSB.	RO	-	O	O
152-167 98h-A7h	All	Reserved - 16B	Reserved - Alarm Thresholds for Module Monitors	RO			
168-169 A8h-A9h	All	Hi Alarm Threshold, Tx Bias Current	High Alarm Threshold on Tx Bias current: in 2 μA units coded as 16 bit unsigned integer, Low byte is MSB.	RO	-	-	R
170-171 AAh-ABh	All	Lo Alarm Threshold, Tx Bias Current	Low Alarm Threshold on Tx Bias current in 2 μA units coded as 16 bit unsigned integer, Low byte is MSB.	RO	-	-	R
172-173 ACh-ADh	All	Hi Alarm Threshold, Tx Optical Power	High Alarm Threshold on Transmitted Optical Power in 0.1 μW units coded as 16 bit unsigned integer, Low byte is MSB.	RO	-	-	R

Table 26 Tx Upper Page 01h Memory Map

Byte	Bit	Name	Description	Type	Required/Optional/ - (Not Applicable)		
					Passive	Active copper	Active Optical
174-175 AEh-AFh	All	Lo Alarm Threshold, Tx Optical Power	Low Alarm Threshold on Transmitter Optical Power in 0.1 µW units coded as 16 bit unsigned integer, Low byte is MSB.	RO	-	-	R
176-179 B0h-B3h	All	Reserved - 4B	Reserved - Alarm Thresholds for Channel Monitors				
180-181 B4h-B5h	All	Checksum	Checksum: Low order 16 bits of the sum of all pairs of bytes from 128 through 175 inclusive, as unsigned integers.	RO	R	R	R
182-205 B5h-CDh	All	Bias Current Monitor Tx11... Bias Current Monitor Tx00	Per-channel Tx Bias current: Monitor. 2B per channel, each measured in 2 µA units coded as 16 bit unsigned integer, Low byte within each byte pair is MSB. Tolerance is ± 0.50 mA.	RO	-	-	O
206-229 CEh-E5h	All	Output Optical Power Monitor Tx11... Output Optical Power Monitor Tx00	Per-channel Tx Light Output Monitor in 0.1µW units coded as 16 bit unsigned integer, Low byte within each pair is MSB. Tolerance is +/- 3 dB	RO	-	-	O
230-255 E6h-FFh	All	Vendor Specific - 26B	Vendor Specific Tx Functions				

7.6.5 RX UPPER PAGE 01H

Table 27 on page 92 shows the memory map for the Rx upper page 01h

Table 27 Rx Upper Page 01h Memory Map

Byte	Bit	Name	Description	Type	Required/Optional/ - (Not Applicable)		
					Passive	Active copper	Active Optical
128 80h	All	Hi Alarm Threshold for 1st Rx Temperature Monitor MSB	Hi Alarm Threshold for 1st Internal Temperature Monitor for Rx MSB: Integer part coded in signed 2's complement. Tolerance is ± 3°C.	RO	O	O	O
129 81h	All	Hi Alarm Threshold for 1st Rx Temperature Monitor LSB	Hi Alarm Threshold for 1st Internal Temperature Monitor for Rx LSB: Fractional part in units of 1°/256 coded in binary.				
130-131 82h-83h	All	Lo Alarm Threshold 1st Rx Temp Monitor	Lo Alarm Threshold for 1st Internal Temperature Monitor for Rx. Same 2 Byte format as 128-129	RO	O	O	O
132-133 84h-85h	All	Hi Alarm Threshold 2nd Rx Temp Monitor	Hi Alarm Threshold for 2nd Internal Temperature Monitor for Rx. Same 2 Byte format	RO	O	O	O
134-135 86h-87h	All	Lo Alarm Threshold 2nd Rx Temp Monitor	Lo Alarm Threshold for 2nd Internal Temperature Monitor for Rx. Same 2 Byte format	RO	O	O	O
136-143 88h-8Fh	All	Reserved - 8B	Reserved - Alarm Thresholds for Module Monitors				

Table 27 Rx Upper Page 01h Memory Map

Byte	Bit	Name	Description	Type	Required/Optional/ - (Not Applicable)		
					Passive	Active copper	Active Optical
144-145 90h-91h	All	Hi Alarm Threshold Rx Vcc3.3 Monitor	Hi Alarm Threshold for Internal Vcc3.3 Monitor for Rx: Voltage in 100 μV units coded as 16 bit unsigned integer, Low byte is MSB.	RO	-	O	O
146-147 92h-93h	All	Lo Alarm Threshold Rx Vcc3.3 Monitor	Lo Alarm Threshold for Internal Vcc3.3 Monitor for Rx: Voltage in 100 μV units coded as 16 bit unsigned integer, Low byte is MSB.	RO	-	O	O
148-149 94h-95h	All	Hi Alarm Threshold Rx Vcc12-Monitor	Hi Alarm Threshold for Internal Vcc12 Monitor for Rx: Voltage in 100 μV units coded as 16 bit unsigned integer, Low byte is MSB.	RO	-	O	O
150-151 96h-97h	All	Lo Alarm Threshold Rx Vcc12 Monitor	Lo Alarm Threshold for Internal Vcc12 Monitor for Rx: Voltage in 100 μV units coded as 16 bit unsigned integer, Low byte is MSB.	RO	-	O	O
152-167 98h-A7h	All	Reserved - 16B	Reserved - Alarm Thresholds for Module Monitors	RO			
168-175 A8h-AFh	All	Reserved - 8B	Reserved Alarm Thresholds for Channel Monitors	RO			
176-177 B0h-B1h	All	Hi Alarm Threshold, Rx Optical Power	High Alarm Threshold on Received Optical Power in 0.1 μW units coded as 16 bit unsigned integer, Low byte is MSB.	RO	-	-	R
178-179 B2h-B3h	All	Lo Alarm Threshold, Rx Optical Power	Low Alarm Threshold on Received Optical Power in 0.1 μW units coded as 16 bit unsigned integer, Low byte is MSB.	RO	-	-	r
180-181 B4h-B5h	All	Checksum	Checksum: Low order 16 bits of the sum of all pairs of bytes from 128 through 175 inclusive, as unsigned integers.	RO	R	R	R
182-205 B5h-CDh	All	Reserved - 24B	Reserved Rx Channel Monitors	RO			
206-229 CEh-E5h	All	Input Optical Power Monitor Tx11... Input Optical Power Monitor Tx00	Per-channel Rx Light Input Monitor in 0.1μW units coded as 16 bit unsigned integer, Low byte within each pair is MSB. Tolerance is +/- 3 dB	RO	-	-	O
230-255 E6h-FFh	All	Vendor Specific - 26B	Vendor Specific Rx Functions				

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