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RF Power Reference Design Library

FM Broadcast Reference Design

High Ruggedness N–Channel Enhancement–Mode Lateral MOSFETs

MRFE6VP61K25H
MRFE6VP61K25HS
FM Broadcast

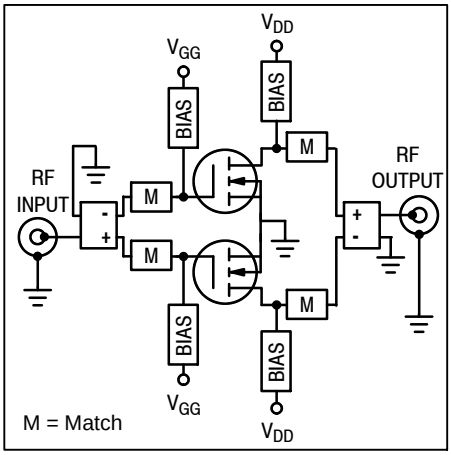
87.5–108 MHz, 1100 W CW, 50 V
FM BROADCAST
REFERENCE DESIGN

Reference Design Characteristics

The MRFE6VP61K25H/HS are versatile devices and are well suited for a wide range of applications. They are capable of delivering 1.2 kW under continuous wave test signaling as a result of their high efficiency and low thermal resistance. This document focuses on FM broadcast radio applications for both analog and complex modulation waveforms.

- Frequency Band: 87.5–108 MHz
- Output Power: 1100 Watts CW
- Supply Voltage: 50 Vdc
- Power Gain (Typ): 25 dB
- Drain Efficiency (Min): 79% (at fundamental frequency)

The MRFE6VP61K25H/HS products are enhanced ruggedness 50 volt LDMOS power transistors that can operate in harsh environments and in highly mismatched applications (within the limit of maximum junction temperature). These parts are designed for high voltage operation and are fabricated using Freescale's very high voltage 6th generation (VHV6E) platform.



FM BROADCAST REFERENCE DESIGN

This reference design is designed to demonstrate the RF performance characteristics of the MRFE6VP61K25H/HS devices when applied to the 87.5–108 MHz FM broadcast frequency band. The reference design is tuned for performance at 1100 watts CW output power, V_{DD} = 50 volts and I_{DQ} = 200 mA.

REFERENCE DESIGN LIBRARY TERMS AND CONDITIONS

Freescale is pleased to make this reference design available for your use in development and testing of your own product or products. The reference design contains an easy–to–copy, fully functional amplifier design. It consists of "no tune" distributed element matching circuits designed to be as small as possible, and is designed to be used as a "building block" by our customers.

HEATSINKING

When operating this fixture it is critical that adequate heat-sinking is provided for the device. Excessive heating of the device may prevent duplication of the included measurements and/or destruction of the device.

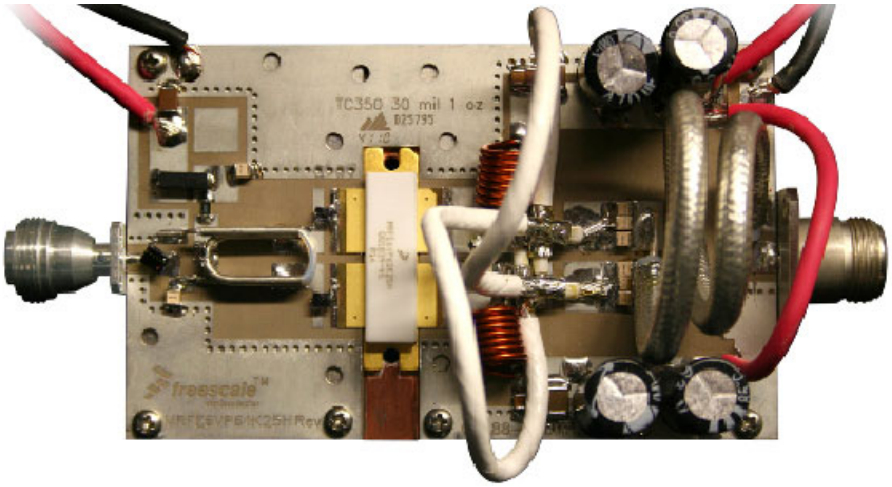


Figure 1. FM Broadcast Reference Design Fixture

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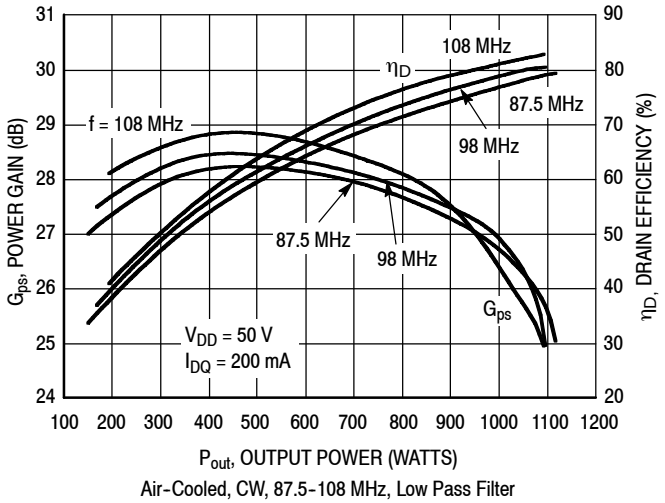
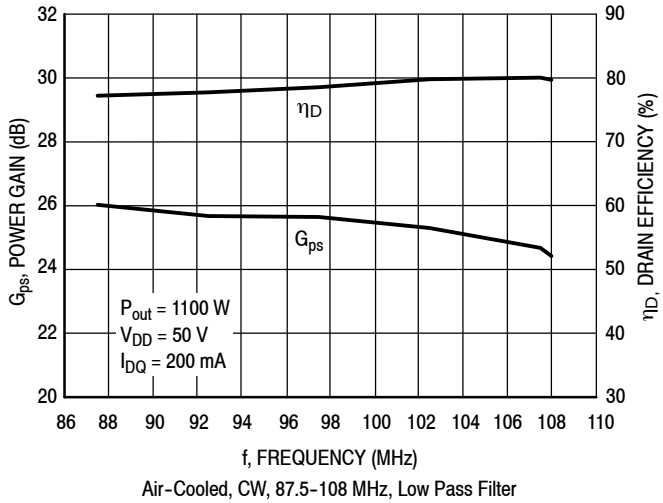
MEASUREMENTS



Air-Cooled, CW, 87.5-108 MHz, Low Pass Filter

Figure 2. Continuous Wave Performance Graph with Low Pass Filter versus Output Power



Air-Cooled, CW, 87.5-108 MHz, Low Pass Filter

Figure 3. Continuous Wave Performance Graph with Low Pass Filter versus Frequency

Table 1. CW Drive-Up at 87.5 MHz

P_{in} (W)	P_{out} (W)	Gain (dB)	IRL (dB)	Eff (%)	V_{DD} (V)	I_{DD} (A)	I_{DQ} (1) (A)
0.3	150	27.0	-6.1	33.6	50	8.9	0.2
0.5	314	28.0	-6.5	48.0	50	13.1	0.2
1.0	639	28.1	-8.1	65.8	50	19.4	0.2
1.5	844	27.5	-10.1	72.6	50	23.2	0.2
2.0	975	26.9	-11.9	76.1	50	25.6	0.2
2.5	1056	26.3	-13.0	78.1	50	27.0	0.2
3.0	1100	25.6	-13.3	79.1	50	27.8	0.2
3.5	1116	25.0	-13.6	79.2	50	28.2	0.2

Table 2. CW Drive-Up at 98 MHz

P_{in} (W)	P_{out} (W)	Gain (dB)	IRL (dB)	Eff (%)	V_{DD} (V)	I_{DD} (A)	I_{DQ} (1) (A)
0.3	168	27.5	-11.0	36.8	50	9.1	0.2
0.5	343	28.4	-11.8	52.0	50	13.2	0.2
1.0	660	28.2	-14.9	68.5	50	19.3	0.2
1.5	864	27.6	-19.4	75.3	50	22.9	0.2
2.0	999	27.0	-22.4	78.7	50	25.4	0.2
2.5	1058	26.3	-22.0	80.1	50	26.4	0.2
3.0	1085	25.6	-22.0	80.2	50	27.0	0.2
3.5	1094	24.9	-22.6	80.4	50	27.2	0.2

Table 3. CW Drive-Up at 108 MHz

P_{in} (W)	P_{out} (W)	Gain (dB)	IRL (dB)	Eff (%)	V_{DD} (V)	I_{DD} (A)	I_{DQ} (1) (A)
0.3	193	28.1	-14.2	40.9	50	9.4	0.2
0.5	377	28.8	-14.9	56.1	50	13.4	0.2
1.0	695	28.4	-15.6	72.9	50	19.1	0.2
1.5	881	27.7	-13.5	78.6	50	22.4	0.2
2.0	980	26.7	-14.1	79.2	50	22.9	0.2
2.5	1018	26.1	-12.2	81.6	50	24.9	0.2
3.0	1066	25.5	-11.8	82.4	50	25.9	0.2
3.5	1092	24.9	-11.8	82.7	50	26.4	0.2

1. I_{DQ} is set by adjusting a variable gate-source voltage while maintaining a constant 50 volts at the drain.

AMPLIFIER DESIGN

MATCHING NETWORK

As a first order approximation, the typical maximum efficiency impedance point corresponds to a 25% power degradation from the maximum P3dB impedance. The maximum output power impedance value on this device corresponds to a 1.25 kW output capability from 87.5–108 MHz. This puts the targeted P1dB compression value at 800 watts of output power total, or 400 watts per side. The initial load impedance is determined using the following equation:

$$R = \frac{(0.85 \times V_{DD})^2}{(2 \times P_{out})} = \frac{(0.85 \times 50\ V)^2}{(2 \times 400\ W)} = 2.25\ \Omega$$

R (drain to drain) = 2.25 Ω x 2 = 4.5 Ω

The coaxial transformer turns ratio was chosen to meet this required impedance level and the length of the coax (series inductance) was tuned to attain maximum efficiency and maximum power transfer between the device and its complex conjugate test fixture load impedance.

FIXTURE IMPEDANCE

V_{DD} = 50 Vdc, I_{DQ} = 200 mA, P_{out} = 1100 W CW

f MHz	Z_{source} Ω	Z_{load} Ω
87.5	2.20 + j6.70	4.90 + j2.90
98	2.30 + j6.90	4.10 + j2.50
108	2.30 + j7.00	4.40 + j3.60

Z_{source} = Test circuit impedance as measured from gate to gate, balanced configuration.

Z_{load} = Test circuit impedance as measured from drain to drain, balanced configuration.

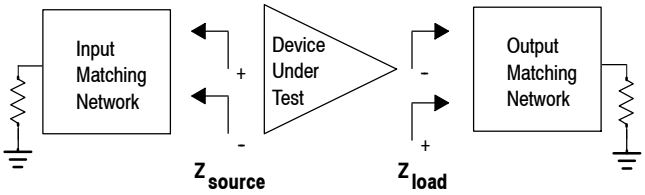


Figure 4. Series Equivalent Source and Load Impedance

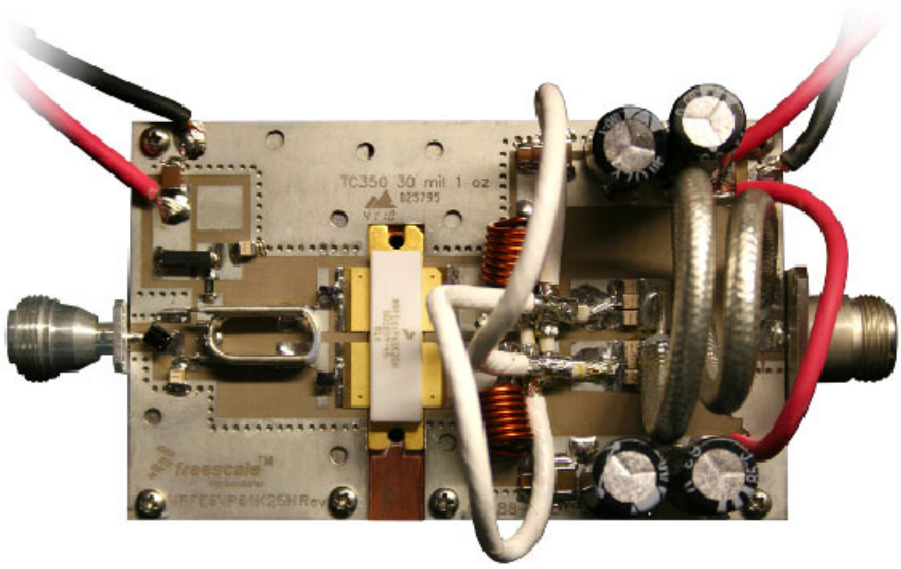


Figure 5. FM Broadcast Reference Design Fixture Impedance

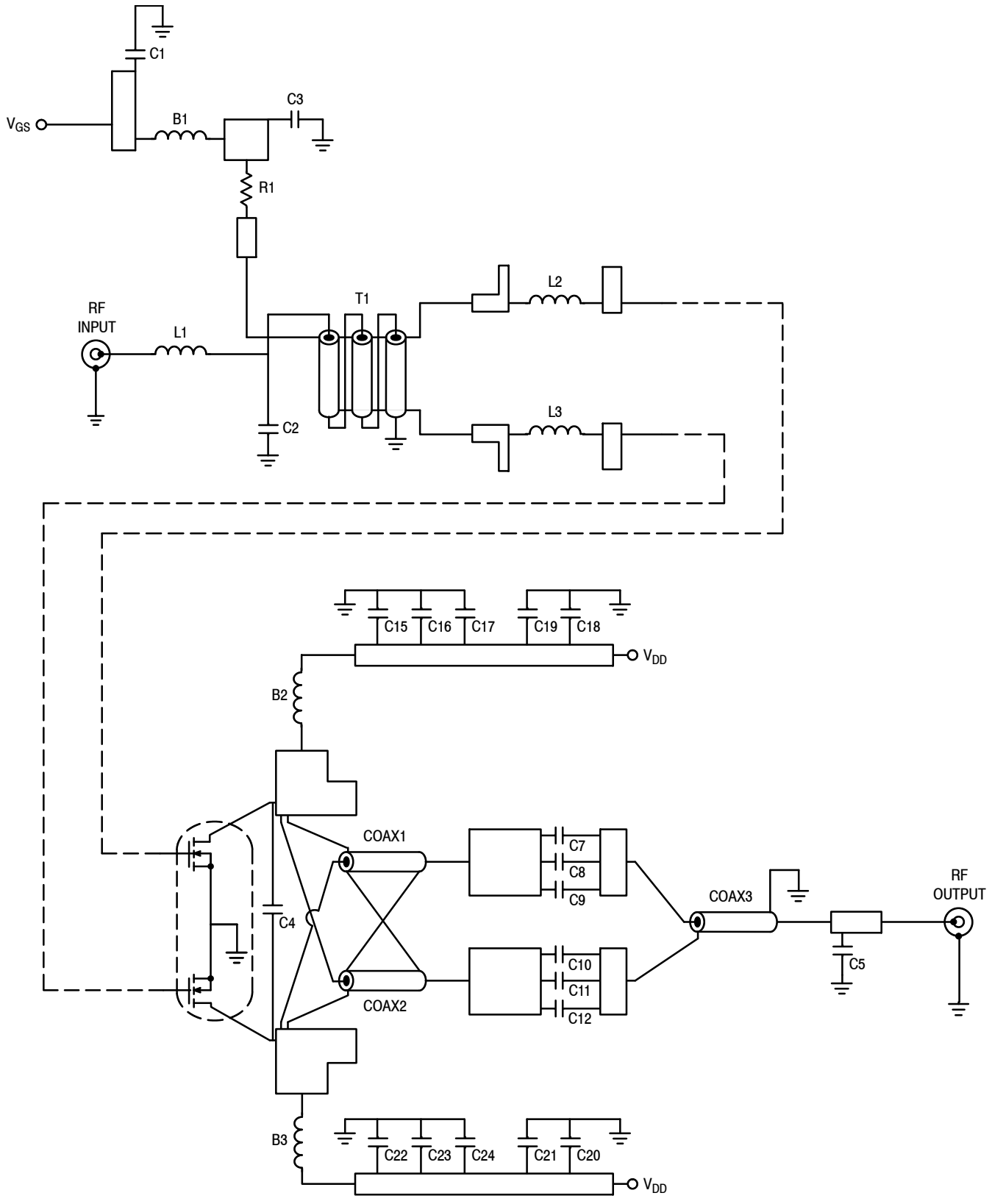
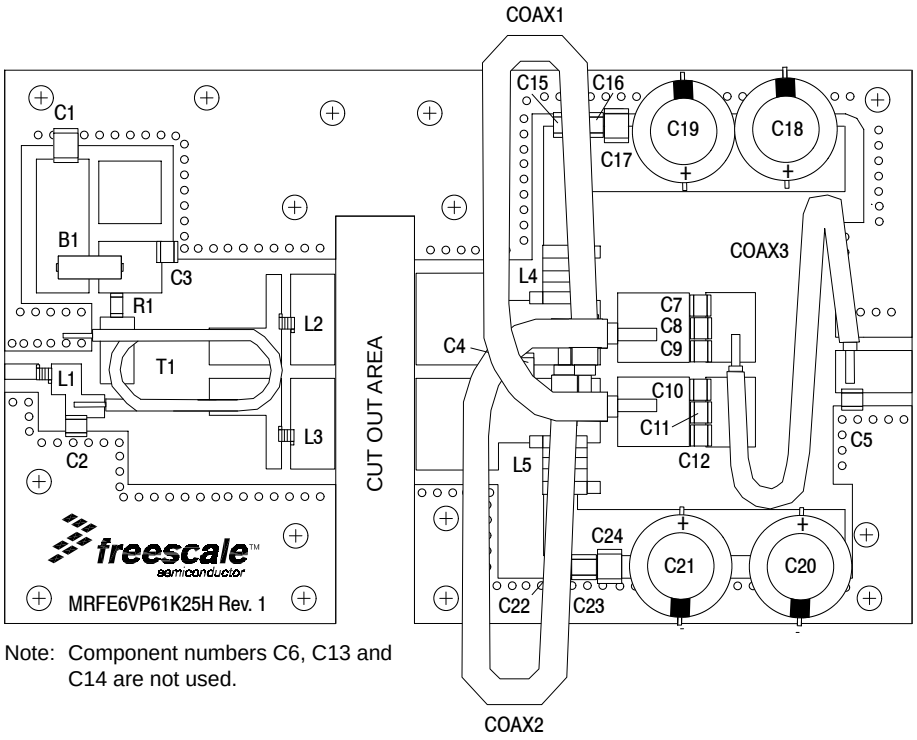


Figure 6. FM Broadcast Reference Design Schematic Diagram



Note: Component numbers C6, C13 and C14 are not used.

Figure 7. FM Broadcast Reference Design Component Layout

Table 4. FM Broadcast Reference Design Component Designations and Values

Part	Description	Part Number	Manufacturer
B1	Long Ferrite Bead	2743021447	Fair−Rite
C1	6.8 μF, 50 V Chip Capacitor	C4532X7R1H685K	TDK
C2	27 pF Chip Capacitor	ATC100B270JT500XT	ATC
C3, C7, C8, C9, C10, C11, C12	1000 pF Chip Capacitors	ATC100B102JT50XT	ATC
C4	39 pF Mica Capacitor	MIN02−002DC390J−F	Cornell Dubilier
C5	3 pF Chip Capacitor	ATC100B3R0CT500XT	ATC
C15, C22	10K pF Chip Capacitors	ATC200B103KT500XT	ATC
C16, C23	1 μF, 100 V Chip Capacitors	C3225JB2A105KT	TDK
C17, C24	10 μF, 100 V Chip Capacitors	C5750X7S2A106MT	TDK
C18, C19, C20, C21	470 μF, 63 V Electrolytic Capacitors	477KXM063M	Illinois Capacitor
L1	39 nH Inductor	1812SMS−39NJLC	Coilcraft
L2, L3	2.5 nH Inductors	A01TKLC	Coilcraft
L4, L5	7 Turn, #16 AWG, ID = 0.3″ Inductors	Copper Wire	
R1	11 Ω, 1/4 W Chip Resistor	CRCW120611R0FKEA	Vishay
T1	Balun	TUI−9	Comm Concepts
Coax1, Coax2	Flex Cables, 12 Ω, 5.9″	TC−12	Comm Concepts
Coax3	Coax Cable, Quickform 50 Ω, 8.7″	SUCOFORM 250−01	Huber+Suhner
PCB*	0.030″, ε_r = 3.5	TC−350	Arlon
Heatsink	NI−1230 Copper Heatsink	C193X280T970	Machine Shop

*PCB artwork for this reference design is available at http://freescale.com/RFbroadcast > Design Support > Reference Designs.

Note: See Appendix A for Tuning Tips.

50 V Drain Voltage

The 87.5–108 MHz FM broadcast reference design fixture was designed to utilize the standard 50 volt power supply commonly used in this market.

Data was collected to characterize the reference design's output power and efficiency vs. drain voltage, as shown in Figure 8. The output power can be adjusted over a 12 dB worth of dynamic range by adjusting the drain voltage, while creating minimal degradation on the efficiency performance.

Refer to Freescale's *50 V RF LDMOS White Paper*. Go to http://freescale.com/RFpower and select Documentation/-White Papers – 50VRFLDMOSWP for more information on 50 V RF LDMOS technology.

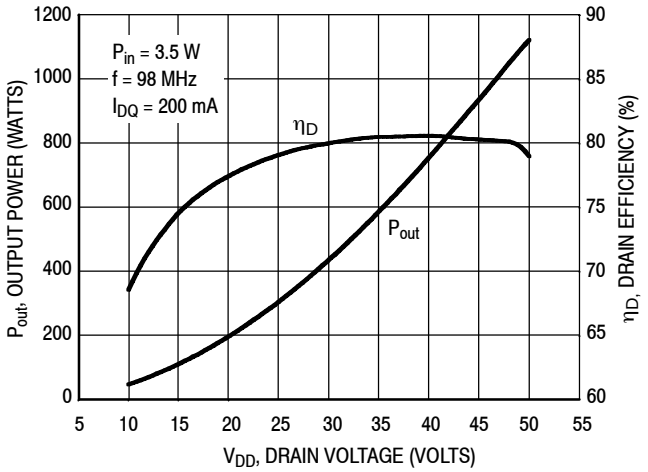


Figure 8. Output Power and Drain Efficiency versus Drain Voltage

Extended Gate Voltage Range

The enhanced electrostatic discharge (ESD) protection structure at the gate of the transistor is a Freescale innovation pioneered in the cellular infrastructure market that is incorporated into the 50 volts RF LDMOS power product portfolios. This ESD structure can tolerate moderate reverse bias conditions, applied to the gate lead, up to –6 volts as shown in Figure 9. This allows these transistors to be used in zero gate voltage, Class C bias applications where the RF voltage swings on the gate can be significantly lower than the ground potential.

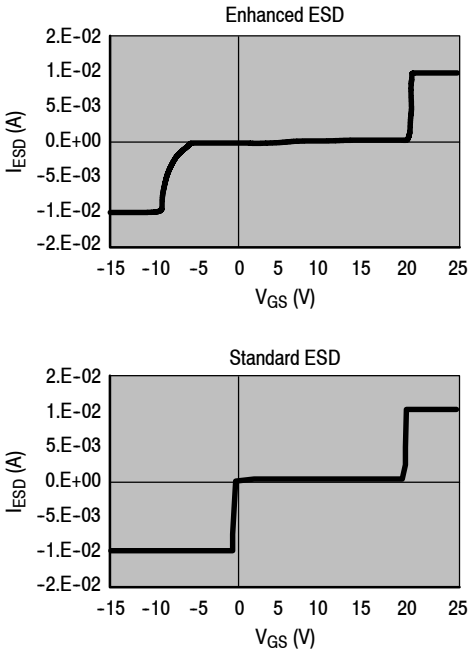


Figure 9. Gate Voltage Breakdown with ESD

High Ruggedness/Energy Absorption

The MRFE6VP61K25H/HS was designed to operate in applications which demand very high ruggedness. The VHV6E technology has proven to be valuable in FM broadcast applications, specifically in high definition (HD) FM transmitters where a high peak–to–average (PAR) digital signal is injected on top of an existing analog FM signal. At the peak of the signal, the voltage waveform could exceed the $V_{(BR)DSS}$ breakdown voltage of the device and thus cause the device to enter into an avalanche condition. However, for the device to fail, the current must be sufficiently high enough during the high voltage period to activate the internal parasitic bipolar transistor buried beneath the active field–effect transistor (FET) structure.

An Integrated Technologies Corporation's Unclamped Inductive Load Tester, model #ITC55100B, was used to measure the maximum energy dissipation capability of the device under these high current and high voltage test conditions.

Figure 10 shows the internal diagram of the ITC55100B tester. The tester controller activates the pulse generator to turn on the device under test (DUT) through the limiting and terminating resistor, R_G, creating a very clean gate pulse waveform. This pulse waveform tests the maximum energy dissipation capability of the DUT by stressing it under various, controlled energy levels. This is accomplished by attaching an unclamped inductive load to the device's drain and source connection and then increasing both the load current and load voltage up until the point that the DUT failure is achieved. Using this test method for power devices ensures proper operation in circuits used to drive inductive loads that may possibly cause an avalanche mode stress on the DUT. The final maximum energy dissipation capability rating, in joules, is calculated by the following equation:

$$E = \frac{1}{2} \times L \times I^2$$

where L is the load inductance value and I is the peak current within the load inductor.

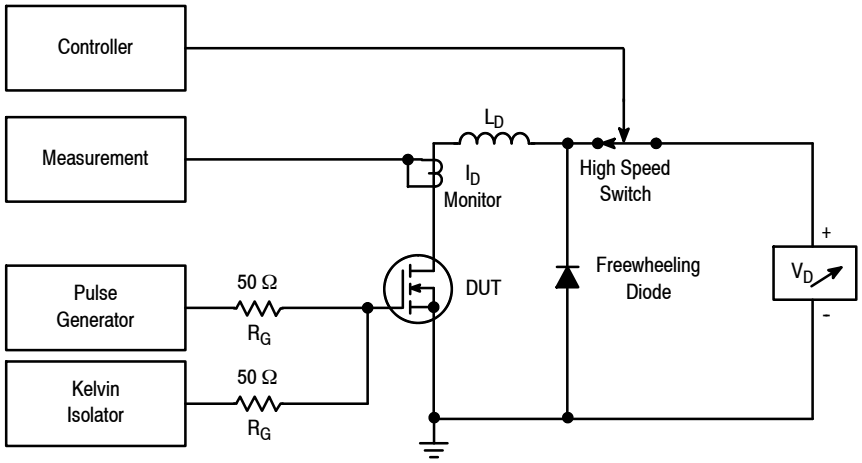
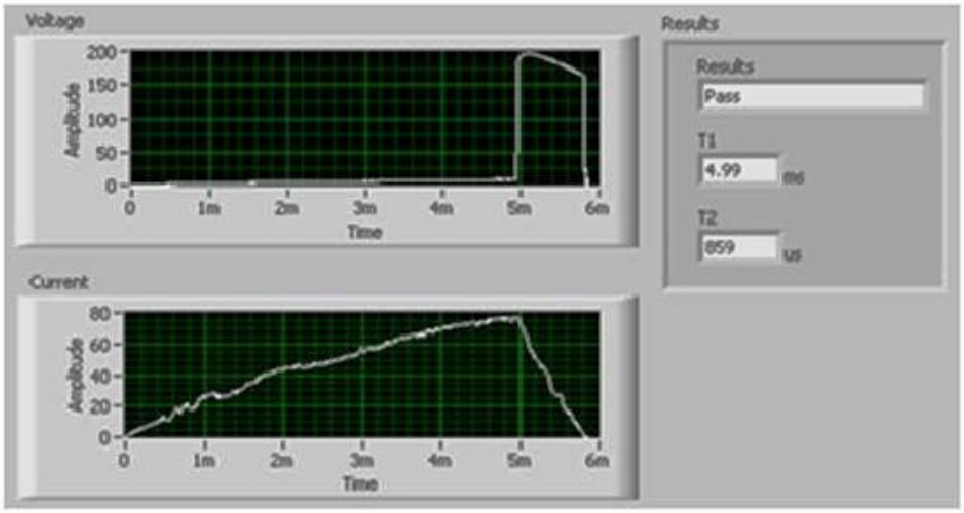


Figure 10. Internal Diagram of the ITC55100B Tester

The highest energy level the MRFE6VP61K25H/HS device passed is shown in Figure 11. During the course of this testing, the device dissipated over 5.77 joules of energy over a discharge time of 859 μsec, while reaching a maximum current of 76 A and a maximum voltage of 197 volts. (These load voltage and current values are taken under short discharge durations to keep the thermal dissipation issues out of the ruggedness equation.)



- Max Voltage = 196.8 Vdc
- End Voltage = 167.5 Vdc
- Energy = 5.766 J (full device)
- ID_{peak} = 76 A

Figure 11. Voltage and Current Curves During Energy Discharge

Reliability

Mean time to failure (MTTF) is defined as a 10% reduction in current handling capability on 50% of the devices within a given sample size. The primary factor in device failure is due to metal electromigration on the die surface. Once the average operating conditions for a given application are determined, then the MTTF can be calculated using the thermal resistance R_{th} value given in the MRFE6VP61K25H product data sheet.

Example: If the desired operating output power is 1100 watts, with 80% drain efficiency:

- I_{Drain} = 1100 W / (80% × 50 V) ~ 27.5 A
- MRFE6VP61K25H R_{th} = 0.15°C/W, case temperature = 80°C
- Dissipated power = P_{dc} – P_{out} + P_{in}
- Dissipated power = 50 V × 27.5 A – 1100 W + 4 W = 279 W
- Temperature rise = 279 W × 0.15°C/W = 42°C
- $T_J = T_{rise} + T_C$ = 42°C + 80°C = 122°C

Utilizing Figure 12 which calculates MTTF versus I_{Drain} and T_J; I_{Drain} = 27.5 A, MTTF for this example is 2700 years.

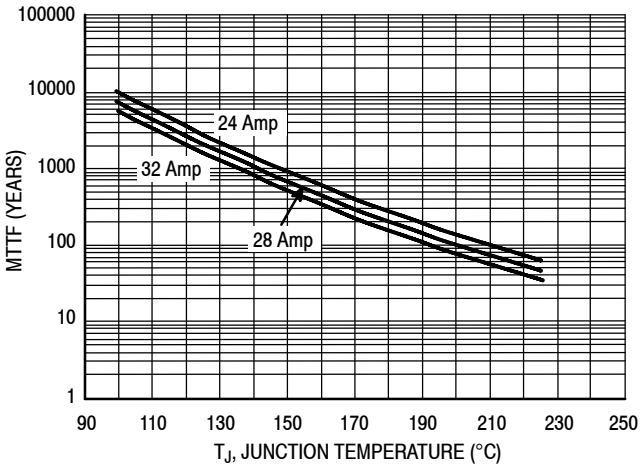
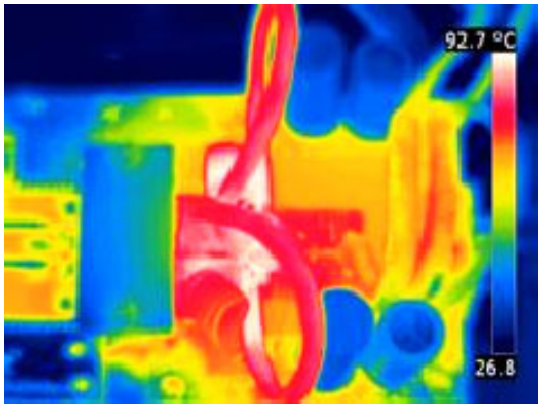


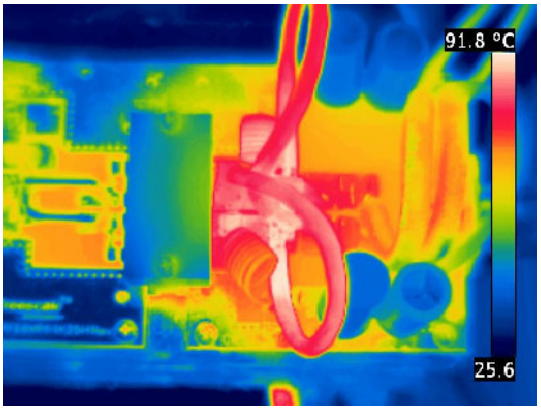
Figure 12. MTTF versus Junction Temperature

THERMAL MEASUREMENTS

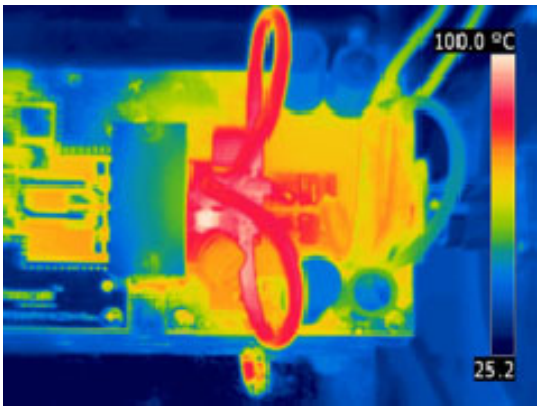
Thermal images of the MRFE6VP61K25H FM broadcast reference circuit were taken using a FLIR Infrared(IR) T360 camera. The hottest point observed was located at the Coax1 and Coax2 junction point with the C4 mica capacitor at 108 MHz. The recorded temperature was 100°C after 10 minutes of operation to reach steady state temperature. Due to the high efficiency achieved by the FM broadcast reference fixture, the overall baseplate temperature remains relatively cool at around 60°C, with forced air cooling at 25°C.



87.5 MHz, 1100 W CW, 79% Drain Efficiency



98 MHz, 1100 W CW, 78% Drain Efficiency



108 MHz, 1100 W CW, 80% Drain Efficiency

Figure 13. IR Images of the Output Matching Network

APPENDIX A

Tuning Tips

- Increasing C4 increases efficiency at the low end of the band (87.5 MHz), but there is a trade−off in power at the high end of the band.
- Increasing the length of Coax3 increases efficiency at the low end of the band (87.5 MHz), but there is a trade off in efficiency and power at the high end of the band.
- Make sure all the coax are measured tip to tip.
- Increasing C5 increases the power, but lowers efficiency.
- Moving C4 closer to the device will improve efficiency across the band, and lowers peak power at the high end of the band.

APPENDIX B

Mounting Tips

The MRFE6VP61K25H/HS is packaged in the industry standard NI−1230 air cavity package which offers outstanding thermal performance.

This package can be assembled into a power amplifier system using several different mounting methods. The popular options include bolting down with screws, clamping and reflow soldering. Freescale recommends the solder reflow method for best thermal and electrical performance.

One of the key advantages to solder mounting includes a superior source contact−to−heatsink interface that provides for lower thermal resistance as well as better electrical grounding, which means that high power RF devices such as the MRFE6VP61K25H/HS parts will have a lower junction temperature and better RF performance when compared to all other mounting options. Lowering the junction temperature of the device also increase the MTTF (Mean Time to Failure), as shown in Figure 8, MTTF versus Junction Temperature.

Refer to AN1908 *Solder Reflow Attach Method for High Power RF Devices in Air Cavity Packages*. Go to http://freescale.com/RFpower and select Documentation/ Application Notes – AN1908 for more information on solder reflow attach method.

APPENDIX C

RF Bench Setup/Continuous Wave Performance (CW)

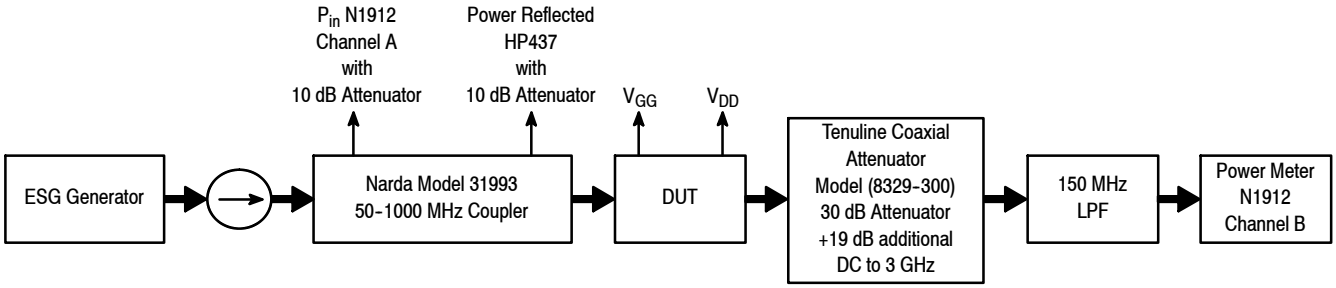
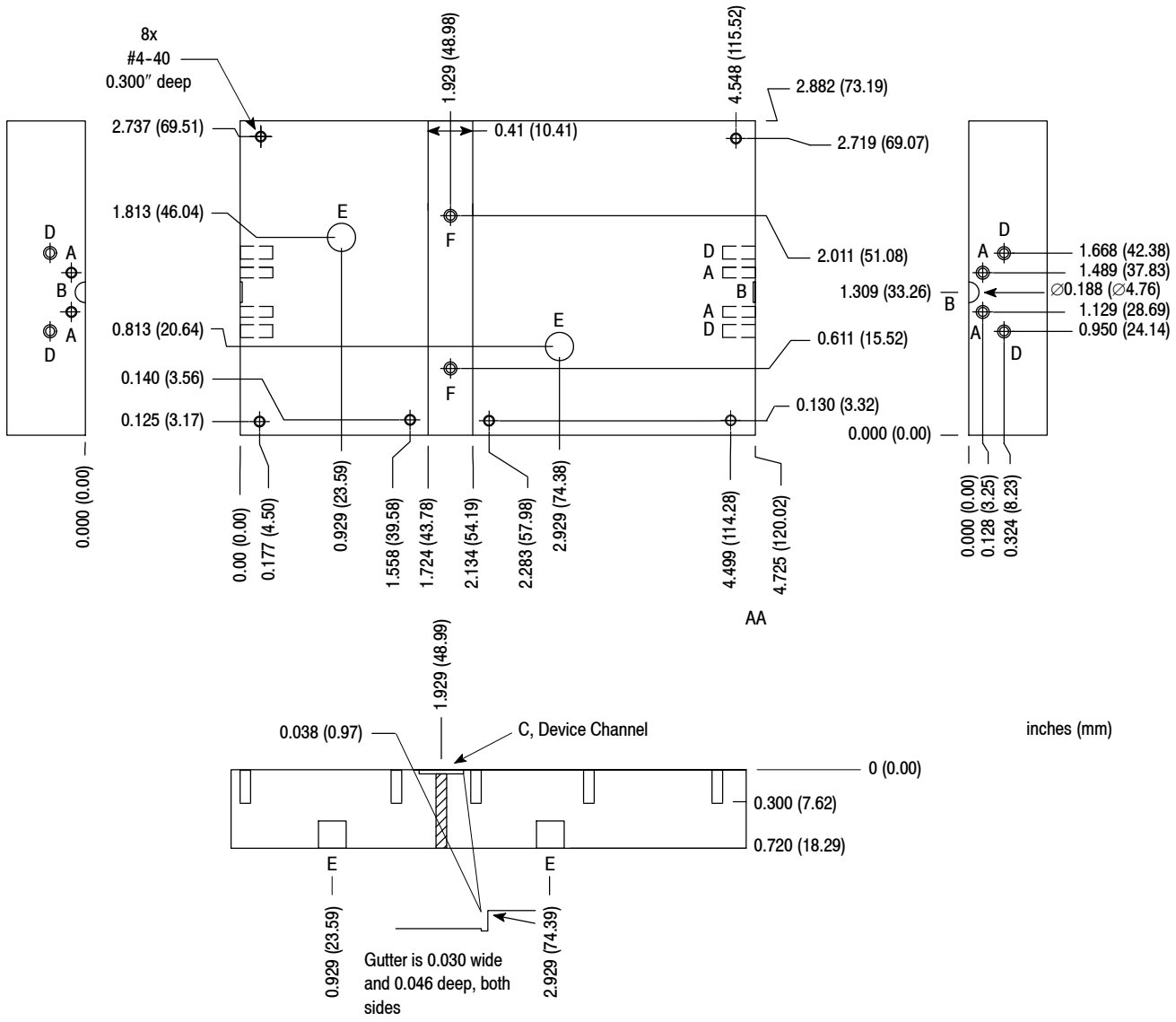


Figure 14. RF Bench Setup

APPENDIX D

Copper Heatsink for FM Broadcast Fixture



0.720″ Copper Heatsink Hole Details

Designators	Details
A	2 places, both sides, drill and tap, #2-56 screw depth 0.300″
B	2 places, both sides, 0.1875″ diameter notch 0.020″ deep
C	NI-1230 channel 0.410″ wide by 0.0380″ deep
D	2 places, both sides, drill depth 0.250″ and tap for #4-40 screw
E	Locator holes from bottom diameter = 0.257″, depth = 0.400″
F	2 places, drill through and tap for #4-40 screw

Figure 15. NI-1230 Heatsink

REVISION HISTORY

The following table summarizes revisions to this document.

Revision	Date	Description
1	May 2011	• Table 4, Component Designations and Values, updated C17, C24 capacitor from “50 V, GRM55DR61H106KA88L, Murata” to “100 V, C5750X7S2A106MT, TDK”, 100 V part provides higher breakdown voltage capability. Corrected R1 part number from “CRCW1206110FKEA” to CRCW120611R0FKEA”. For Coax1, 2, 3, in description changed cm to inches, p. 4.
1.1	June 2011	• Content flow of the reference design document was restructured • Appendix A, Tuning Tips, added additional information, p. 9

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