AN1229
Application note

SD2932 RF MOSFET for 300 W FM amplifier

Introduction

This application note gives a description of a broadband power amplifier operating over the frequency range 88 - 108 MHz using the new STMicroelectronics RF MOSFET transistor SD2932.

Table 1. Typical achievable performances

Parameter	Performance
Device	1 X SD2932
Frequency	88-108 MHz
Vdd	50 V
Idq	200 mA
Pout	300 W
Gain	>19 dB
Input return loss	< -11 dB
Drain efficiency	>70%

1 Amplifier design

1.1 Input matching network

Typical input gate-to-gate impedance of SD2932 at 100 MHz is Zin = Rs + jXs = 2 - 2.6 j, and can also be expressed as the combination of parallel resistance and reactance using the following formulas:

Equation 1

$$Rp = Rs \bullet \left[1 + \left(\frac{Xs}{Rs}\right)^2\right] = 5.38\Omega$$

Equation 2

$$X_P = R_P / \left(\frac{X_S}{R_S}\right) = -4.14j\Omega$$

Therefore, in order to achieve good input matching performances over the frequency range 88-108 MHz the unbalanced 50 Ω is to be transformed into an impedance with a value as close as possible to Rp of 5.38 Ω

From the circuit schematic given in *Figure 6* , we can see that the input matching network is based on a two section balun (1:1 balun in cascade with a 9:1 balun transformer) which transforms the unbalanced 50 Ω to a balanced 5.56 Ω (2 x 2.78 Ω / 9:1 ratio). The first section, a 5" long - 50 Ω coaxial cable and the second section, a two 3.9" long - 25 Ω flexible coaxial cables with ferrite core NEOSIDE, are connected as described: a 10 nH inductor (L1) is connected between the two gates to compensate SD2932 input parallel reactance Xp.

1.2 Input matching network tuning

Figure 1. Input Impedance of 1:1 balun in cascade with 4:1 balun

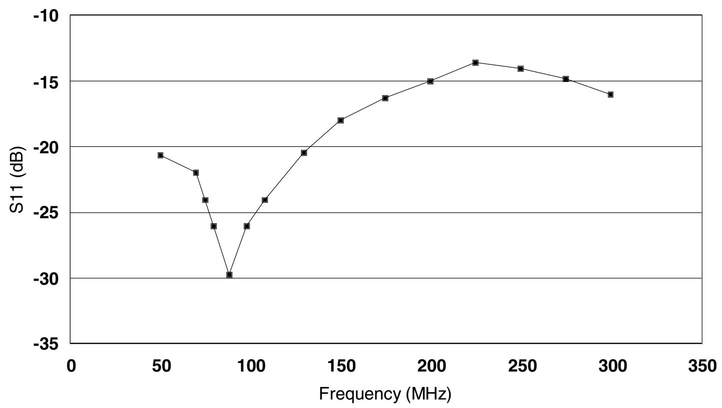
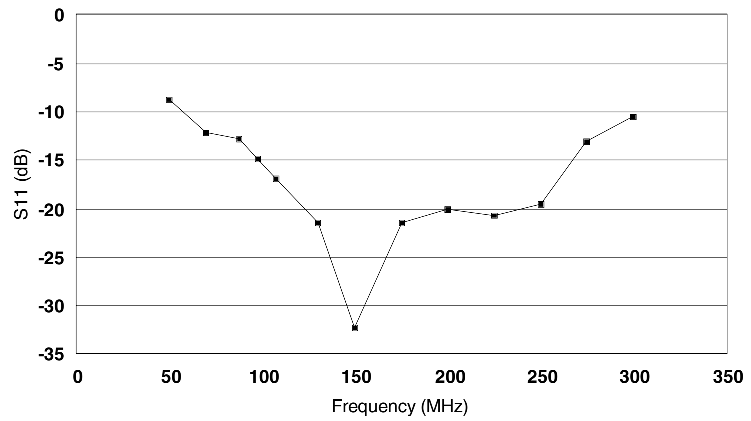


Figure 2. Input Impedance of 1:1 balun in cascade with 9:1 balun



SD2932 input matching network was tuned in order to achieve the best compromise in terms of power gain (Gp) and input return loss (Rtl) over the frequency range 88 - 108 MHz. Best results were achieved by adding a 10 pF chip capacitor (C1) between RFIN and the 1 nF blocking capacitor (C2).

1.3 Output matching network

The output impedance of each side is a combination of the output capacitance Coss (195 pF) and the optimum load resistance which can be determined as follows:

Equation 3

$$Rp = \frac{(0.85 \bullet Vdd)^2}{2 \bullet Pout} = \frac{0.85 \bullet 2500}{2 \bullet 150W} = 6.02\Omega$$

The total optimum load, seen by SD2932 (drain to drain), is 2 x 6.02 = 12.04 Ω Therefore, a simple two section balun (1:1 balun in cascade with a 4:1 balun transformer) is used to transform the unbalanced 50 Ω to a balanced 12.5 Ω (2 x 6.25 Ω) which is very near to the total optimum load resistance.

The first section, a 5" long - 50 Ω flexible coaxial cable, and the second section, two 5" long - 25 Ω flexible coaxial cables, are connected as described in *Figure 6*.

To compensate for the output capacitance Coss of SD2932 , a 40 nH inductor (L2) is connected between the two drains. This LC network (L2 & Coss) is a high pass filter with a resonance frequency calculated at 10 % below the minimum operating frequency:

Equation 4

$$C_{OSS} = \frac{C_{OSS(per\ side)}}{2} = \frac{180pF}{2} = 90pF$$

Equation 5

$$\text{Frequency of resonance} = 0.9 \bullet 88MHz = 80MHz$$

Equation 6

$$L2 \bullet Coss \bullet (2 \bullet pi \bullet F)^2 = 1 \rightarrow L2 = 44nH$$

Figure 3. Power gain vs. frequency

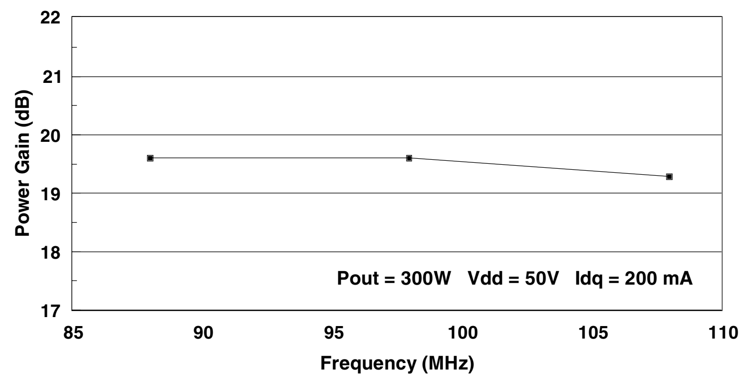


Figure 4. Drain efficiency vs. frequency

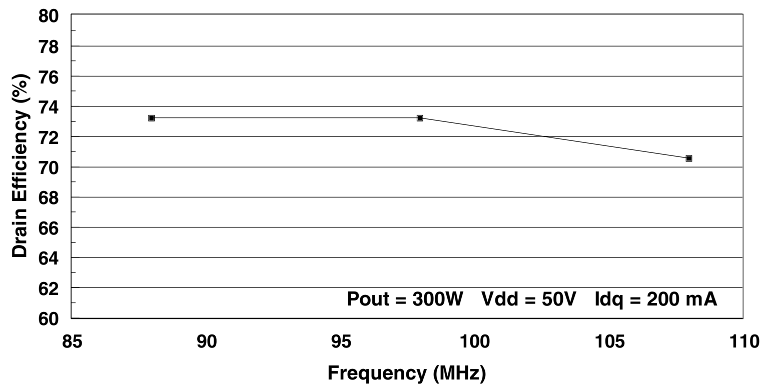
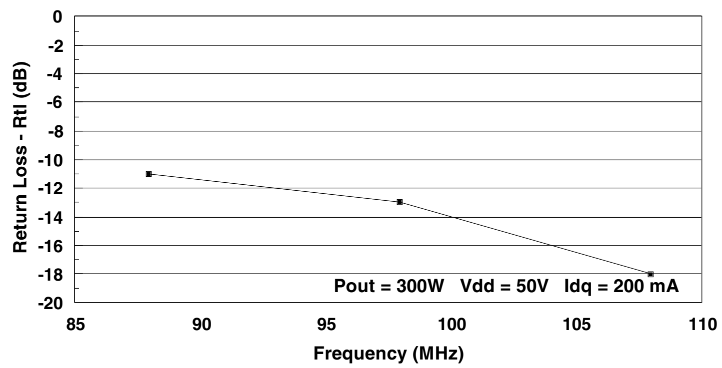


Figure 5. Drain efficiency vs. frequency



2 SD2932 typical performances and conclusion

Figure 3, *Figure 4* and *Figure 5* show power gain, efficiency and input return loss over the frequency range 88 - 108 MHz at a constant output power of 300 W and a drain supply voltage of 50 V and a quiescent current of 200 mA. Typical performances are as follows:

Table 2. Typical performances

Parameters	Min	Max
Gp	19.3 dB	19.6 dB
R_{TL}	-18 dB	-11 dB
Eff	71%	73%

Finally, in this report we have demonstrated ST's SD2932 MOSFET transistor excellent performance as a wideband 300 W - 50 V push-pull amplifier for FM applications.

Figure 6. 88-108 MHz circuit schematic

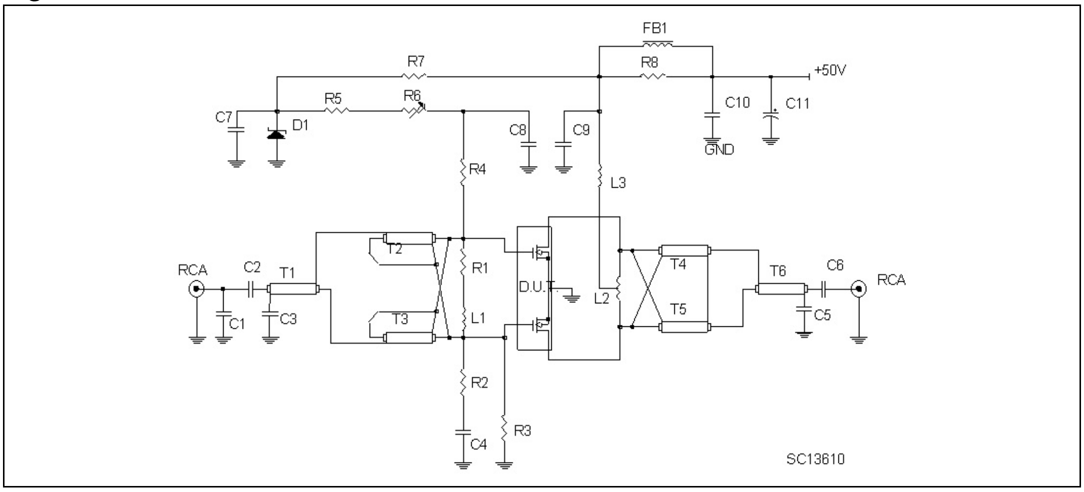


Table 3. 88-108 MHz circuit components list

Symbol	Description
PCB	1/32" Woven fiberglass 0.0030 Cu, 2 side, er
T1	50 Ω Flexible coax cable OD 0.006", 5" long
T2/ T3	9:1 Transformer, 25 Ω flexible coax cable OD 0.1" 3.9". ferrite core NEOSIDE
T4 / T5	4:1 Transformer, 25 Ω flexible coax cable OD 0.1" 5.0" long.
T6	50 Ω flexible coax cable OD 0.1" 5.0" long.
FB1	VK200
C1	10 pf Ceramic capacitor
C2/C3/C4/C7/C8	1 nF Chip capacitor
C5/C6	1 nF ATC chip capacitor

Table 3. 88-108 MHz circuit components list (continued)

Symbol	Description
C9	470 pF ATC chip capacitor
C10	100 nF chip capacitor
R1	56 Ω Resistor
R2/R4	10 Ω Chip resistor
R3	10 K Ω Resistor
R5	5.6 K Ω Resistor
R6	10K Ω 10 Turn trim resistor
R7	3.3 K Ω/ 1 W Resistor
R8	15 Ω/ 1 W Resistor
D1	6.8 V Zener diode
L1	10 nH inductor
L2	40 nH inductor
L3	70 nH inductor

3 Revision history

Table 4. Revision history

Date	Revision	Changes
21-Jun-2006	2	Minor text changes
30-Jul-2007	3	The document has been reformatted