BUILDING PUSH-PULL, MULTIOCTAVE, VHF POWER AMPLIFIERS

Prepared By

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By choosing the right feedback network and wide-band transformers, users will have a powerful amp.

TWIN FET packages are the heart of a unique, push-pull 300-W power amplifier. With a 50-V power supply, this broadband amplifier is easy to implement, and has excellent impedance-matching characteristics and low DC-current levels.

Applications include low-band and VHF communications base stations, FM broadcast, low-band TV, and certain medical uses. For these uses, a frequency coverage of at least 10 to 175 MHz is required. However, for a particular application, the required bandwidth can be narrowed for increased circuit efficiency.

The development of high-power VHF/UHF power FETs make the amplifier possible. These FETs have recently become available in a push-pull package configuration—commonly called the Gemini. A push-pull Gemini package is a flange-mounted transistor header capable of accommodating two individual transistors—either FETs or bipo-

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Transformer characteristics		
Frequency (MHz)	R_p (Ω)	X_p (Ω)
10	12.85	+ J50
30	12.20	+ J58
50	11.90	+ J95
100	10.20	+ J150
175	8.70	+ J9.60

lars. One of the three transistor electrodes is connected to the normally grounded flange.

On first observation, it seems that a push-pull header would not be as advantageous as separate headers for each transistor. Separate headers provide better thermal distribution, improved circuit design and layout versatility, and higher production yields. The result is lower cost per watt of output power.

In addition, operating parameters of the two transistors in a push-pull header must be closely matched before assembly. If there is even the slightest mismatch in any of the several DC parameters, the device must be rejected. Another drawback of the push-pull header is that the adjacent-transistor configuration results in reduced thermal ratings, leading to a decrease in electrical ruggedness.

But there are important advan-

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1. For this high-power VHF amplifier, separate circuit boards are used for the input and output. The magnetic core has been removed from the output transformer for clarity. Note the thermistor (upper middle) attached to one end of the transistor flange.
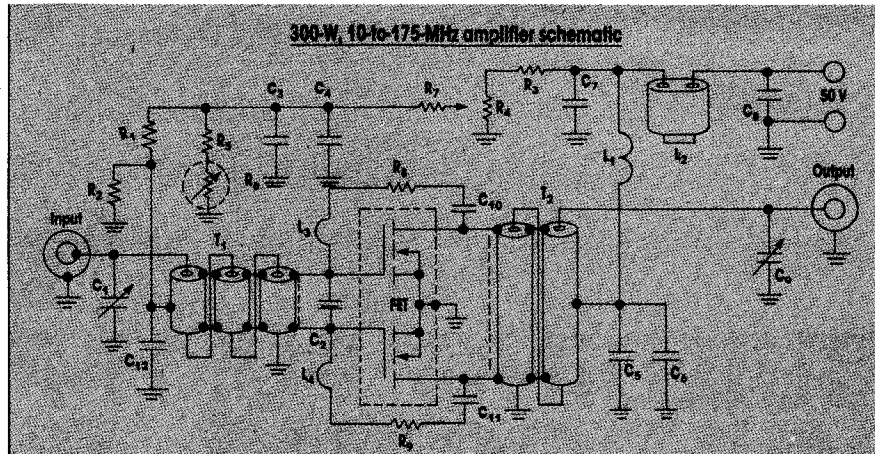
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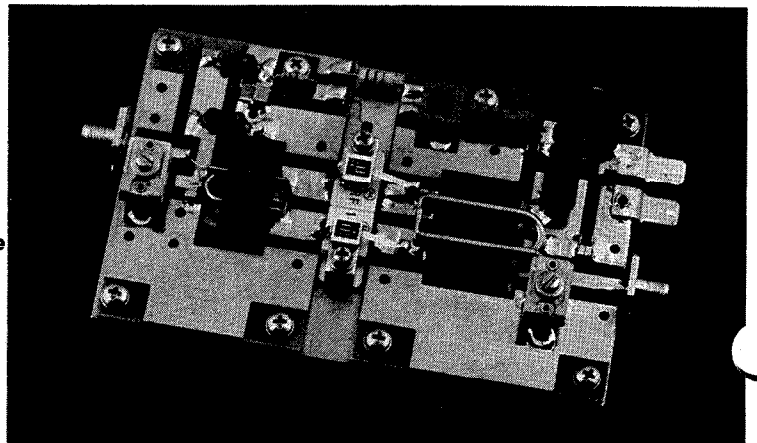
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tages to the push-pull design. For example, the power gain performance of this design is difficult to duplicate in single-ended configurations because power gain is directly related to the emitter- or source-to-ground inductance. Also, in push-pull designs, the common-mode inductance is completely insignificant; mutual inductance between each emitter, or source, becomes the critical factor. This mutual inductance is much easier to control and minimize.

There are several different design approaches that can be used for solid-state power amplifiers. A transformer-based push-pull design is the best approach for multioctave devices, but such circuits are not easily implemented for frequency ranges higher than 50 to 100 MHz. If transformers are used, their locations and connecting points, as well as the locations of any associated capacitances, are extremely critical. These parameters must be tightly controlled.

Control of input and output impedances to the matching networks is also required. These impedances must be kept constant over the entire operating range. Internal impedances—which are directly proportional to the frequency—cannot be easily adjusted. However, some designs mitigate the effect of this frequency-dependent internal impedance. These practices include inserting special correcting elements between the matching network and the device, designing the matching networks for the proper impedance-versus-frequency slope, and introducing negative-feedback series resistor-inductor-capacitor (RLC) net-

works for controlling the feedback over the desired frequency band. Often, the negative-feedback technique is used with special, correcting-element techniques.

Negative feedback is the output voltage returned to the input at 180 deg. out of phase. In series RLC networks, the series resistor limits the overall amount of feedback voltage and also lowers the Q of the inductor. The capacitance is mostly used for DC blocking.
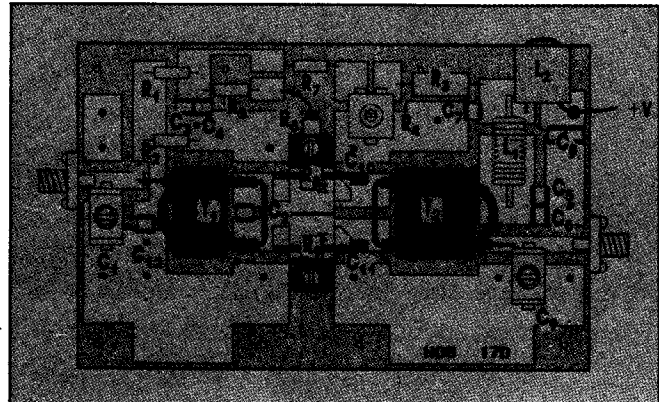
With these networks, the series inductive reactance results in phase lag. This phase lag is maximum at high frequencies, where the effect of the negative feedback is the least. As a result, the out-of-phase voltage must be obtained from either side of the push-pull circuit—or through a specially designed network—which allows the impedance of the voltage source to be optimized.

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3. Building the amplifier is easy using this component layout.

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A resistive network eliminates the reduced efficiency of the feedback power. This power is dissipated in the series resistor. Power loss can be considerable—up to 15 percent at the low end of the spectrum—where the feedback is highest.
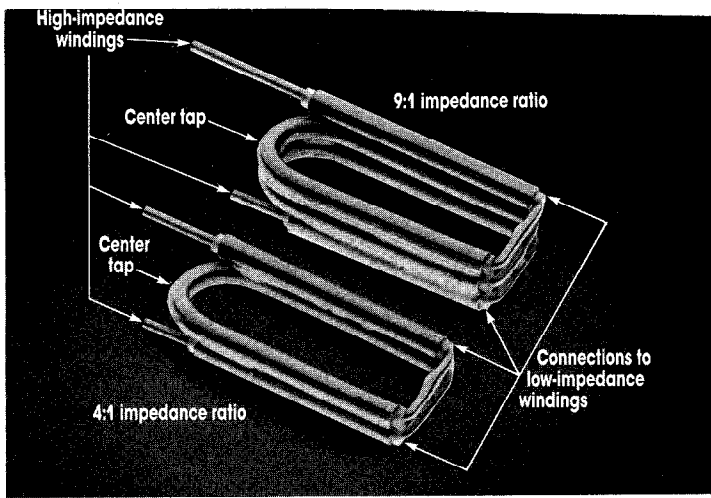
Another factor in negative-feedback system design is that the out-of-phase feedback voltage must be injected after the input-matching network. This will not affect the device input impedance, but will lower the load impedance to the input-matching network. Also, there will be an additional load to the device output at low frequencies, where the output impedance is higher and less reactive.

In addition to the correct use of negative feedback, the basis for good, multioctave, RF power-amplifier design is well-designed wideband transformers and correct matching elements. With proper design, this combination yields a low-input circuit VSWR over many octaves and results in a system with level power output.

Proper push-pull design requires a noncritical, source-to-ground inductance that provides a DC current path. This allows the circuit board to be split into two sections: an input

300-W, 10-to-175-MHz amplifier schematic

R_1 = 1 kΩ—1/2 W
R_2 = 1.5 kΩ—1/2 W
R_3 = 1.5 kΩ—2 W
R_4 = 1-kΩ trimpot
R_5 = 6.8 - 8.2 kΩ—1/4 W (depends on FET g_{fs})
R_6 = Thermistor—10 kΩ at 25°C; 2.5 kΩ at 75°C
R_7 = 2 kΩ—1/2 W
R_8, R_9 = 50-Ω power resistor—EMC Technology type 5310, or KDI Pyrofilm type PPR 515-20-3
C_1, C_9 = 8 - 60 pF, ARCO 404 or the equivalent
C_2 = 130-pF ceramic chip
C_3, C_{10}, C_{11} = 0.1-µF ceramic chip
C_4, C_8, C_{12} = 1000-pF ceramic chip
C_6, C_7 = 5000-pF ceramic chip
C_5 = 0.47-µF ceramic chip, or lower values in parallel to

reach the value indicated
L_1 = 10 turn, AWG #16 gage enameled wire, 5-mm inside diameter
L_2 = Ferrite beads, 1.3-µH total
L_3, L_4 = Lead lengths of R_8 and R_9, 20-mm total
T_1 = 9:1 RF transformer—25 Ω, 0.062-in. outside diameter, semirigid coax
T_2 = 1:4 RF transformer—25 Ω, 0.090-in. outside diameter, semirigid coax
FET = MRF151G
Notes: For T_1, two type 75-26 Ω and 1 Micrometals powdered iron cores are required.
For T_2, three type 100-8 Ω and 1 Micrometals powdered iron cores are required.
All chip capacitors of 5000 pF or less are ATC type 100 or equivalent.

2. At the heart of the 300-W amplifier is the Gemini push-pull transistor configuration. This broadband amplifier operates in the 10-to-175-MHz range.

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4. Correct construction of the wideband transformers makes the amplifier work properly.

and an output board (Fig. 1). The input section carries the input-matching network and part of the gate-bias circuit.

The first parts of the bias circuit—the output matching network and the drain-source voltage (V_{DS}) filtering and bypassing components—are mounted on the output board. This configuration allows each board to be changed independently for matching-network modifications or for other purposes. Furthermore, the input matching is almost identical for a 28-V power-supply counterpart, requiring the change of only one chip capacitor and the output board (Fig. 2).

Component locations can be seen in Fig. 3. The board material is G10, which is adequate for frequency ranges as high as 200 to 250 MHz, especially since no high-Q elements are incorporated. For a two-sided board, the lower side is a continuous ground plane, although not necessarily in all locations. This means that no through-holes are provided for components such as resistors, trimpots, and inductors. These components—as well as chip capacitors and wideband transformers—must be surface-mountable. The total number of feedthroughs to the bottom ground plane is 16.

Gate-bias voltage is obtained from the main DC supply voltage through two voltage dividers. The first divider includes a trimpot for the bias adjustment. The second divider accommodates a thermistor-resistor combination (R_5, R_6) for temperature stabilization of FET biases. Without this stabilization, the drain idle current would have an approximate temperature coefficient of +15 mA/°C. With this temperature coefficient, idle current would increase by a factor of three if the case temperature was doubled.

The FET and circuit boards are mounted on a milled copper plate, measuring $115 \times 75 \times 6$ mm. Input/output SMA-type connectors are mounted at the end of this plate. The result is a self-contained, single structure that can be fastened to a properly cooled heatsink. In laboratory tests, the copper plate—called the heat spreader—was pressed against an air-cooled heatsink by its own weight with a thermal compound interface. The V_{DS} feed circuitry consists of standard high- and low-frequency filtering and bypassing. In Fig. 2, it is clear that components L_1 and C_7 handle the high-frequency end; the low-frequency end is handled by the L_2, C_8 components.

Normally it is desirable to filter down to very low frequencies to prevent any RF energy from feeding back to the power supply, in case of load mismatches and instabilities. But this type of filtering applies primarily to single-ended circuits. In push-pull circuits, the DC feed is usually at a balanced point, with no RF potential. In this push-pull circuit, such an elaborate filtering network is not necessary, except when partially damaged devices cause excessive unbalances between the two sides.

IMPEDANCE MATCHING

Input- and output-impedance matching is done with unique wideband transformers (Figs. 4 and 5).[1] Advantages of using these transformers include DC isolation between the primary and secondary turns, automatic balanced-to-unbalanced functions, and compact size vis-a-vis the power-handling capability. The principle is the same as in ordinary low-frequency transformers. However, the tight coupling coefficient is achieved between the transformers' windings by the use of a low-impedance transmission line, in this case, semirigid coaxial cable.

The low-impedance side always has one turn, and consists of parallel, connected segments of the coax outer conductor. The high-impedance side has inner conductor segments that are connected in series. This arrangement permits only integer impedance ratios that are perfect squares, such as 1, 4, 9, and 16. The coupling coefficient between the primary and secondary turns can be controlled by varying the coax impedance. The optimum line impedance formula, Eq. 1, also applies to the transmission-line transformers:

$$Z_0 = \sqrt{R_L(R)}^{1/2} \qquad (1)$$

High line impedance results in loss of high frequency response, whereas a very low impedance would further lower the R_P at the middle frequencies (see table).

There is a trade-off between the cable diameter and the length of the board. Depending on where the lines
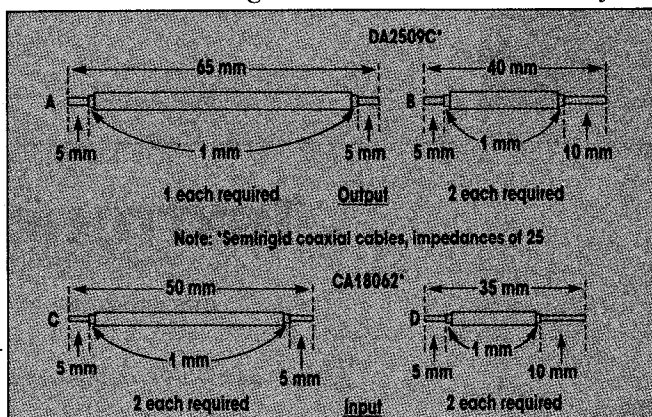
5. Semirigid coaxial cables are bent and formed to produce the wideband transformers. The outer conductors are soldered together. The inner conductor of all segments are sharply bent inwards against each other.

are stacked, using large-diameter cable results in less-definable connection points to the low-impedance winding. This results in an increased leakage inductance. The areas of the coax inner conductor—where the winding series connections are made—are uncontrollable and contribute to the leakage inductance.

In an optimum configuration, the low-impedance winding connection points should be brought together as close as possible. This minimizes the lengths of the uncovered inner-conductor segments, but the physical format would be difficult to accomplish.

The optimum value for the R_P would be exactly 12.5 Ω, with a high value for the X_P. In fact, if X_P is equal to, or greater than, the high-impedance termination, it can be omitted. Then, only the R_P becomes the determining factor. The worst case is at 100 MHz, at which the R_P is low and the X_P is high (see table).

This means the transformer ratio is greater than 1:4 at that frequency, resulting in a dip in the drain efficiency. It is the result of the leakage inductance and can be observed at frequencies as low as 50 MHz. The compensation capacitor, C_9, is optimized at 175 MHz, but its influence diminishes at 130 to 150 MHz. Despite all of this, the overall performance of the transformer was considered satisfactory.

Variations of the output impedance with frequency, compared to those of the input, are usually several times smaller. Therefore, impedance-sloping networks are rarely seen. Such networks should be able to handle high RF currents and voltages and would be difficult to design with low losses. Negative feedback, however, tends to present an artificial load to the device output and it can be designed to decrease with frequency.

The parallel, equivalent gate-to-gate input impedance of the push-pull network is 1.28 – J 3.12 Ω at 175 MHz, making the normalized impedance value equal to 3.37 Ω. At 10 MHz, the normalized impedance would be 15.7 Ω. At 175 MHz, a 16:1 impedance ratio would result in a closer input-impedance match, but it was decided that a 9:1 ratio would provide a closer match at lower frequencies. The high end can be corrected with an adjustment of C_1 and C_2. At 10 MHz, the input transformer would see a 15.7 Ω load, which represents a VSWR of almost 5:1.

Therefore, if no correction network or feedback is employed, negative feedback will level the power gain as well. But, with simple RLC networks, only the high- and low-frequency ends can be equalized, leaving a "hump" at the middle frequencies. In most cases, this hump is only 2 to 3 dB—tolerable for most applications. The series resistor should lower the Q of the inductor. But real optimization requires a variable source for the feedback voltage.[1] The feedback resistor values can also be calculated.[2]

A simplified model of the feedback network can be seen in Fig. 6. Only the series inductor, which is used to

shape the gain slope, is omitted. This inductor can be treated as an additional variable. Its value for the spectrum in question would be lower than the minimum limit achievable with the physical layout, regarding the minimum lead lengths. In other words, the model only allows the calculation of the feedback resistor values at a single frequency. In most instances, the minimum series inductor is limited by the physical size of the circuitry. Ideally, its reactance should be infinite at the high end of the band and should be zero at 10 MHz. From the data sheet and by simple calculations, it is possible to obtain the following values:

- G_{PS} at 10 MHz = 26 dB.
- G_{PS} at 175 MHz = 16 dB (lowered to 15 dB with feedback).
- P_{in} 1 (f = 10 MHz, P_{out} = 300 W) = 0.75 W, V_{in} (RMS) = 2.03V (V_2).
- P_{in} 2 (f = 175 MHz, P_{out} = 300 W) = 9.50 W, V_{in} (RMS) = 7.23V (V_1).
- V_3 = RMS output voltage (drain to drain) = –61.25 V.
- R_1, R_2 (transformer source and gate-to-gate impedances) = 5.5 Ω.
- R_3 = feedback resistor.
- R_4 (output load) = 12.5 Ω.

The value of the feedback resistor is given by:

$$R_3 = \frac{V_2 + V_3}{\left[\left(\dfrac{V_1 - V_2}{R_1}\right) - \left(\dfrac{V_2}{R_2}\right)\right]} - R_4$$
$$= 48.3 \ \Omega \text{ (each resistor)} \qquad (2)$$

Total power dissipated (R_8 and R_9) = 63.28 $\times$ 0.58 = 36.70 W, or 18.35 W per resistor. The values can be rounded to 50 Ω, allowing the use of stock resistors. The resistors used here are rated for 25 W. They have a one-sided flange for heatsinking purposes, which is mounted on 6.35-$\times$-6.35-$\times$-4-mm-high copper blocks in each end of the FET. Holes are provided through the blocks, and common screws are used to mount the resistors and the FET.

The purpose of the copper blocks is to conduct the heat away from the resistors to the heatsink through the ends of the FET flange and to raise their height to more than the top surface of the ceramic lids of the FET, allowing the resistors to be mounted directly on top of each lid. This design provides the shortest path between the drain and the gate, still leaving about 20 mm of lead length, which is the practical minimum for the series inductance.

On the top of one of the resistor flanges, fastened with the common resistor-FET mounting screw, is a solder lug into which one end of a thermistor (R_6) has been attached. Together with R_5, it tracks the FET gate-threshold voltage variations with the FET flange and heatsink temperature. Similar thermistors come in pill or cylinder forms, and are 3 to 4 mm in diameter and 4 to

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7. Input VSWR is effectively constant. However, the choice of transformer core material can change VSWR performance.

5 mm long. Normally they have wires soldered to each end, of which one was removed and replaced with the solder lug. The lug is the electrical contact to the ground and the thermal contact to the heatsink. Thermistors with similar mounting may be commercially available.

Since the output-load impedance is fixed and set for a nominal 12.5 Ω, the optimum supply voltage would be approximately 45 V for the best combination of drain efficiency and saturated power. If good linearity is required, higher voltage will give better results. In most applications, such as single sideband (where the duty cycle is low), the efficiency is less important. Other factors that affect efficiency are the amount and type of magnetic material in the output transformer, the amount of negative feedback introduced, and the magnitude of drain idle current.

It would be difficult to design an amplifier covering the 1-to-175-MHz range in one segment, since highly permeable magnetic material is excessively lossy at VHF. Transmission-line transformers would allow multiturn windings and the use of material with lower permeability, but could easily lead to excessive physical line length. For extremely broadband designs, a low overall efficiency must be accepted, as well as reduced power output from the specified device values. In such cases, efficiencies of 40 to 45 percent are typical.

However, if the band is split into segments such as 1 to 75 MHz and 75 to 175 MHz, magnetic material in the output transformer is not required for the high segment, resulting in 10-to-15-percent higher efficiency. Amplifiers, for even narrower bandwidths such as the 88-to-108-MHz FM broadcast band, have been designed with efficiencies up to 70 percent using the same devices and design technique.

Some power is absorbed by the feedback networks at the high end of the band as a result of the finite reactance of the series inductances.
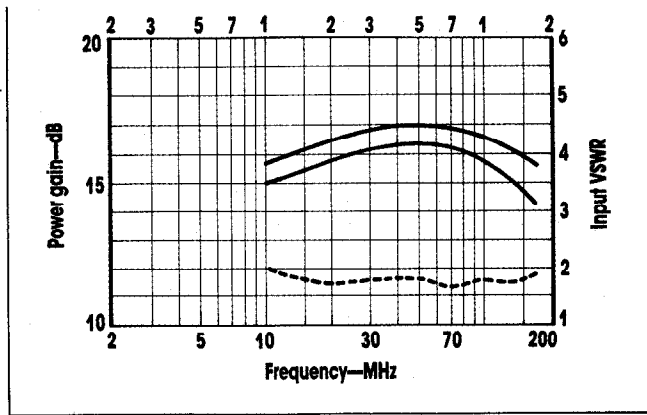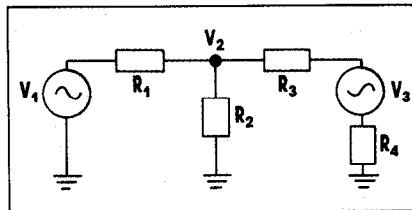
6. A negative-feedback network plays an important role in the amplifier's operation. Design of this DC model is based on a series RLC circuit.

The reactance decreases in proportion with the frequency and reaches its minimum value at the lowest frequency of operation, which is where maximum power loss due to feedback occurs. The numbers previously determined from the feedback resistor calculations permits a determination: The power loss is P_{in} 2 – P_{in} 1 + 36.7 W = 45.45 W, which converts to 7.5 percent, assuming 50-percent initial efficiency.

Linear amplifiers usually operate at a lower efficiency than amplifiers designed for CW or FM service. For good linearity, the output-matching network is designed for a higher transform ratio than that which is optimum for efficiency, which also results in higher saturated power output. Linearity is affected by the amount of quiescent idle current as well, of which a certain amount is always required. In a FET amplifier, going from class B to class C has a larger effect on efficiency than in a bipolar design, since the gate-threshold voltage is usually higher than the base-emitter forward voltage. Zero gate voltage would lower the amplifier's power gain, but would also increase its efficiency by more than that accounted for by the idle current, and could actually be thought of as setting the operating point closer to class D.

Stability is a concern with all solid-state amplifiers. It is easier to achieve with FETs than bipolar

transistors, mainly due to a higher ratio of feedback capacitance to input impedance. The "half f_0 oscillation" phenomenon is unknown with FETs, since the nonlinear diode junctions are not present. However, at low frequencies the FET input impedance is almost a pure capacitance with high reactance, resulting in extremely high power gain. If the FET gate is not properly terminated due to input mismatches, low-frequency instabilities may take place—especially if the frequency response of the input circuit is low enough to sustain the activity.

For push-pull RF FET amplifiers, the two gates must have sufficient isolation between each other at the frequency at which the device internal capacitances, wirebond inductances, and external inductances resonate. If the gate inductance is low compared to the device's internal inductances, oscillations at the resonant frequency will occur.[3-5]

Depending on the exact conditions and device type, relatively low-level parasitic oscillations can occur; in worst-case scenarios, a latching-type condition will destroy the FET instantly. This can be prevented by lowering the Q of the resonant circuit with series resistance or inductance at the gates. Unfortunately, this seriously affects the high frequency performance of the amplifier. A more practical solution is simply to load the input transformer itself with magnetic material, which in this design is required to extend the frequency response down to 10 MHz in any case, and would be required for any amplifier of this type regardless of the frequency range.

The input VSWR can be optimized for lower frequencies by increasing the value of C_2 and adjusting C_1 (Fig. 2). The optimum value for C_2 at 150 MHz is approximately 180 pF.

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Its location, which is critical, should be inside T_1 (Fig. 3). The C_2 capacitor should be soldered in place before the mounting of T_1. Some designers allow a fair amount of input reflected power at low frequencies to compensate for excessive power gain. However, this may result in instabilities with the driver, unless biased into class A.

In this design, the input and output magnetic cores are heatsunk to the copper heat spreader. In the case of E- and I-type cores, the I section is pressed flat against the heat spreader, and the E section is cemented to it through a rectangular opening in the circuit board. Since the cemented joints have high thermal resistance, this is not a perfect way to remove the heat from the core, but it lowers the temperature by 20 to 30°C from no cooling at all. Cooling is only necessary for certain types of ferrites with low Curie points. The powdered iron transformer core does not have a Curie point in that sense and can be operated at high temperatures without changes in its magnetic properties.

The efficiency is lowest with full bandwidth and high supply voltage. Although the data was taken under CW conditions, continuous operation of the unit is not recommended, except with reduced duty cycle such as SSB or linear pulse. For applications above 50 to 70 MHz, it is recommended that no magnetic material is inserted in T_2 (Fig. 6). This applies especially to FM and other CW modes, at which the unit should be run at reduced power levels and voltages. At full power output (Fig. 7) and worst-case efficiency, power dissipation gets dangerously close to the derated limit, assuming a 60-to-70°C flange temperature.

Overtightening the device mounting screws will bow the relatively thin and long flange. Split lockwashers should be used, with enough mounting torque to fully compress the washer. Silicone thermal compound must be applied to the flange/heat-spreader interface. A thin layer wiped only to the flange bottom is sufficient and will spread evenly under the pressure. This interface, the mounting torque, and the flatness and type of mounting surface are some of the most important aspects in high-power transistor amplifier design because heat is the number one enemy of any solid-state device. ••

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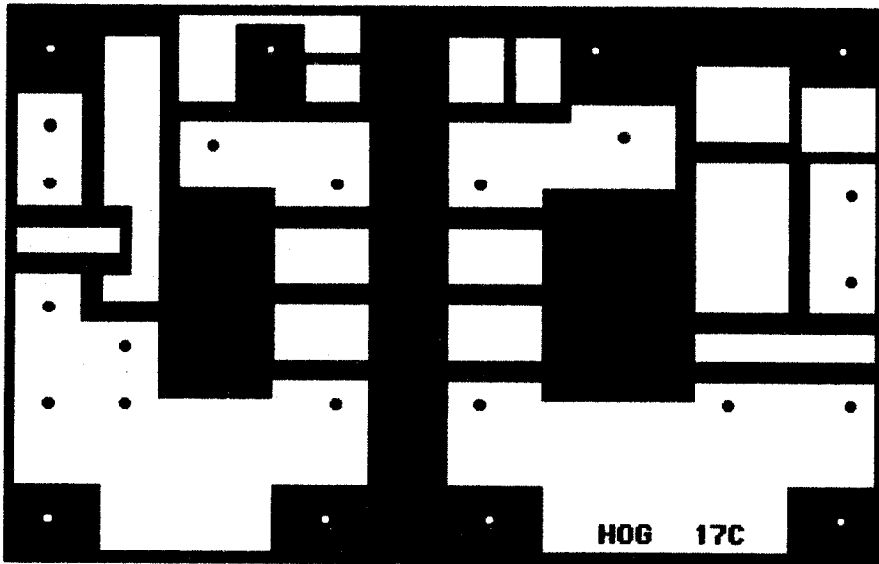
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