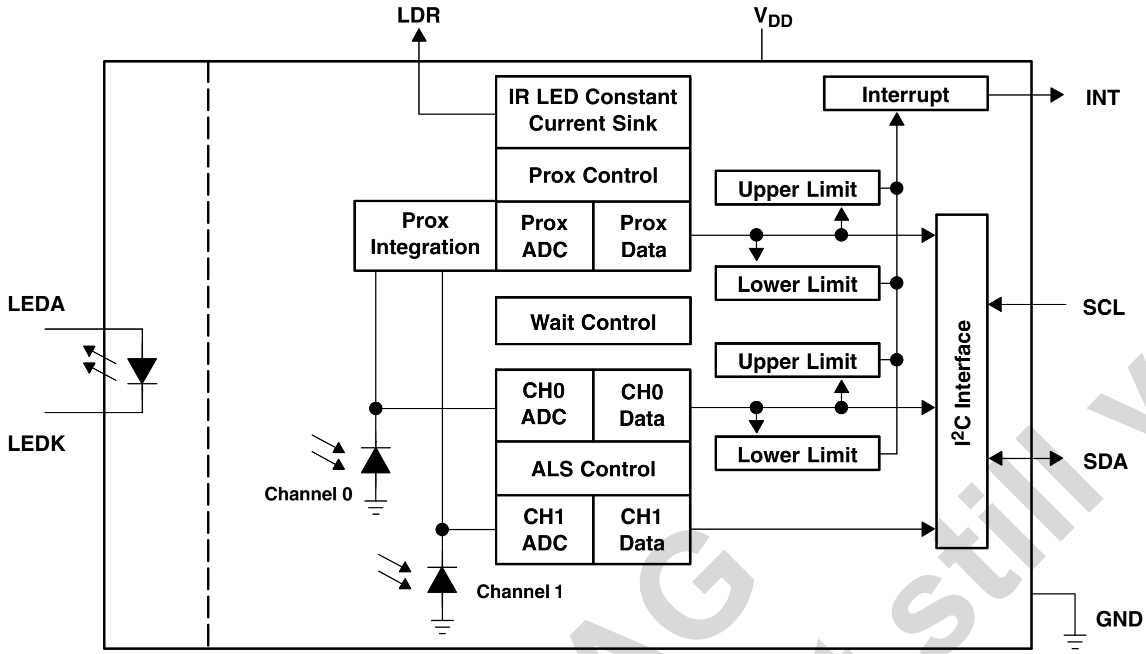
Functional Block Diagram



Detailed Description

The light-to-digital device provides on-chip photodiodes, integrating amplifiers, ADCs, accumulators, clocks, buffers, comparators, a state machine, and an I^2C interface. Each device combines one photodiode (CH0), which is responsive to both visible and infrared light, and a second photodiode (CH1), which is responsive primarily to infrared light. Two integrating ADCs simultaneously convert the amplified photodiode currents to a digital value providing up to 16-bits of resolution. Upon completion of the conversion cycle, the conversion result is transferred to the Ch0 and Ch1 data registers. This digital output can be read by a microprocessor where the luminance (ambient light level in lux) is derived using an empirical formula to approximate the human eye response.

A fully integrated proximity detection solution is provided with an 850-nm IR LED, LED driver circuit, and proximity detection engine. An internal LED driver pin (LDR) is externally connected to the LED cathode (LEDK) to provide a controlled LED sink current. This is accomplished with a proprietary current calibration technique that accounts for all variances in silicon, optics, package, and most important, IR LED output power. This eliminates or greatly reduces the need for factory calibration that is required for most discrete proximity sensor solutions. The *device* is factory calibrated to achieve a proximity count reading at a specified distance with a specific number of pulses. In use, the number of proximity LED pulses can be programmed from 1 to 255 pulses, which allows different proximity distances to be achieved. Each pulse has a 16 μs period with a 7.2 μs on time.

Communication with the device is accomplished through a fast (up to 400 kHz), two-wire I^2C serial bus for easy connection to a microcontroller or embedded controller. The digital output of the device is inherently more immune to noise when compared to an analog photodiode interface.

The device provides a separate pin for level-style interrupts. When interrupts are enabled and a pre-set value is exceeded, the interrupt pin is asserted and remains asserted until cleared by the controlling firmware. The interrupt feature simplifies and improves system efficiency by eliminating the need to poll a sensor for a light intensity or proximity value. An interrupt is generated when the value of an ALS or proximity conversion exceeds either an upper or lower threshold. In addition, a programmable interrupt persistence feature allows the user to determine how many consecutive exceeded thresholds are necessary to trigger an interrupt. Interrupt thresholds and persistence settings are configured independently for both ALS and proximity.

Terminal Functions

TERMINAL NAME	NO.	TYPE	DESCRIPTION
GND	3		Power supply ground. All voltages are referenced to GND.
INT	7	O	Interrupt — open drain (active low).
LDR	6	O	LED driver input for proximity IR LED, constant current source LED driver.
LEDA	4		LED anode.
LEDK	5		LED cathode. Connect to LDR pin when using internal LED driver circuit.
SCL	2	I	I^2C serial clock input terminal — clock signal for I^2C serial data.
SDA	8	I/O	I^2C serial data I/O terminal — serial data I/O for I^2C .
V_{DD}	1		Supply voltage.

Available Options

DEVICE	ADDRESS	PACKAGE – LEADS	INTERFACE DESCRIPTION	ORDERING NUMBER
TMD27721	0x39	Module−8	I^2C Vbus = V_{DD} Interface	TMD27721
TMD27723	0x39	Module−8	I^2C Vbus = 1.8 V Interface	TMD27723
TMD27725†	0x29	Module−8	I^2C Vbus = V_{DD} Interface	TMD27725
TMD27727†	0x29	Module−8	I^2C Vbus = 1.8 V Interface	TMD27727

† Contact TAOS for availability.

Absolute Maximum Ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{DD} (Note 1) . . . . . 3.8 V
Digital I/O Voltage (except LDR) . . . . . −0.5 V to 3.8 V
Max LEDA Voltage (T_A=0 to 70C, 4.4V otherwise. Note 2) . . . . . 4.8 V
Max LDR Voltage (T_A=0 to 70C, 4.4V otherwise. Note 3) . . . . . 4.8 V
Output terminal current (except LDR) . . . . . −1 mA to 20 mA
Storage temperature range, T_{stg} . . . . . −40°C to 85°C
ESD tolerance, human body model . . . . . 2000 V

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltages are with respect to GND.

2. Maximum 4.8V DC over 7 years lifetime.
Maximum 5.0V spikes with up to 250s cumulative duration over 7 years lifetime.
Maximum 5.5V spikes with up to 10s (=1000* 10ms) cumulative duration over 7 years lifetime.

3. Maximum voltage with LDR = off.

Recommended Operating Conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}	2.2	3	3.6	V
Supply voltage accuracy, V_{DD} total error including transients	−3		3	%
LED Supply Voltage (Max shown for T_A=0 to 70C, 4.4V otherwise)	2.5		4.8	V
Operating free-air temperature, T_A (Note 2)	−30		85	°C

NOTE 2: While the device is operational across the temperature range, functionality will vary with temperature. Specifications are stated only at 25°C unless otherwise noted.

Operating Characteristics, V_{DD} = 3 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{DD}	Supply current	Active — LDR pulse off		195	250	μA
		Wait state		90		
		Sleep state — no I^{2}C activity		2.2	4	
V_{OL}	INT, SDA output low voltage	3 mA sink current	0		0.4	V
		6 mA sink current	0		0.6	
I_{LEAK}	Leakage current, SDA, SCL, INT pins		−5		5	μA
I_{LEAK}	Leakage current, LDR pin		−5		5	μA
V_{IH}	SCL, SDA input high voltage	TMD27721	0.7 V_{DD}			V
		TMD27723	1.25			
V_{IL}	SCL, SDA input low voltage	TMD27721			0.3 V_{DD}	V
		TMD27723			0.54	

ALS Characteristics, V_{DD} = 3 V, T_A = 25°C, AGAIN = 16×, AEN = 1 (unless otherwise noted) (Notes 1 ,2, 3)

PARAMETER		TEST CONDITIONS	CHANNEL	MIN	TYP	MAX	UNIT
	Dark ADC count value	E_e = 0, AGAIN = 120×, ATIME = 0xDB (100 ms)	CH0	0	1	5	counts
			CH1	0	1	5	
	ADC integration time step size	ATIME = 0xFF		2.58	2.73	2.9	ms
	ADC number of integration steps			1		256	steps
	ADC counts per step	ATIME = 0xFF		0		1024	counts
	ADC count value	ATIME = 0xC0		0		65535	counts
	ADC count value	λ_p = 625 nm, E_e = 46.8 μW/cm^2, ATIME = 0xF6 (27 ms) (Note 2)	CH0	4000	5000	6000	counts
			CH1		950		
		λ_p = 850 nm, E_e = 61.7 μW/cm^2, ATIME = 0xF6 (27 ms) (Note 3)	CH0	4000	5000	6000	
			CH1		2900		
	ADC count value ratio: CH1/CH0	λ_p = 625 nm, ATIME = 0xF6 (27 ms) (Note 2)		0.152	0.19	0.228	
		λ_p = 850 nm, ATIME = 0xF6 (27 ms) (Note 3)		0.43	0.58	0.73	
R_e	Irradiance responsivity	λ_p = 625 nm, ATIME = 0xF6 (27 ms) (Note 2)	CH0		107.2		counts/ (μW/ cm^2)
			CH1		20.4		
		λ_p = 850 nm, ATIME = 0xF6 (27 ms) (Note 3)	CH0		81.5		
			CH1		47.3		
	Gain scaling, relative to 1× gain setting	AGAIN = 1× and AGL = 1			0.16		×
		AGAIN = 8× and AGL = 0		7.2	8.0	8.8	
		AGAIN = 16× and AGL = 0		14.4	16.0	17.6	
		AGAIN = 120× and AGL = 0		108	120	132	

NOTES: 1. Optical measurements are made using small-angle incident radiation from light-emitting diode optical sources. Red 625 nm and infrared 850 nm LEDs are used for final product testing for compatibility with high-volume production.

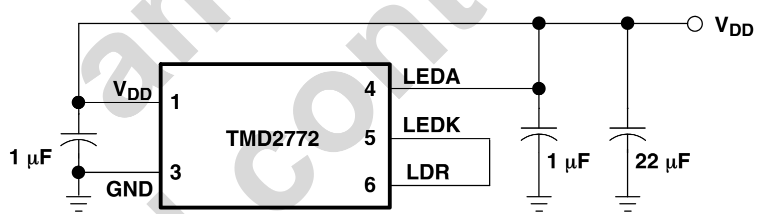
2. The 625 nm irradiance E_e is supplied by an AlInGaP light-emitting diode with the following typical characteristics: peak wavelength λp = 625 nm and spectral halfwidth Δλ½ = 20 nm.

3. The 850 nm irradiance E_e is supplied by a GaAs light-emitting diode with the following typical characteristics: peak wavelength λp = 850 nm and spectral halfwidth Δλ½ = 42 nm.

Proximity Characteristics, $V_{DD} = V_{LEDA}$ = 3 V, T_A = 25°C, PEN = 1 (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{DD}	Supply current	LED On		3		mA
I_{LEDA}	LEDA current (Note 1)	LED On, PDRIVE = 0		100		mA
		LED On, PDRIVE = 1		50		
		LED On, PDRIVE = 2		25		
		LED On, PDRIVE = 3		12.5		
PTIME	ADC conversion steps		1		256	steps
PTIME	ADC conversion time	PTIME = 0xFF (= 1 conversion step)	2.58	2.73	2.9	ms
PTIME	ADC counts per step	PTIME = 0xFF (= 1 conversion step)	0		1023	counts
PPULSE	LED pulses (Note 5)		0		255	pulses
LED On	LED pulse width	PPULSE = 1, PDRIVE = 0		7.3		μs
	LED pulse period	PPULSE = 2, PDRIVE = 0		16.0		μs
	Proximity response, no target (offset)	PPULSE = 8, PDRIVE = 0, PGAIN = 4×, (Note 2)		100		counts
	Prox count, 100-mm target (Note 3)	73 mm × 83 mm, 90% reflective Kodak Gray Card, PGAIN = 4×, PPULSE = 8, PDRIVE = 0, PTIME = 0xFF (Note 4)	450	520	590	counts

NOTES:
1. Value is factory-adjusted to meet the Prox count specification. Considerable variation (relative to the typical value) is possible after adjustment.
2. Proximity offset varies with power supply characteristics and noise.
3. I_{LEDA} is factory calibrated to achieve this specification. Offset and crosstalk directly sum with this value and is system dependent.
4. No glass or aperture above the module. Tested value is the average of 5 consecutive readings.
5. These parameters are ensured by design and characterization and are not 100% tested.
6. Proximity test was done using the following circuit. See the **Application Information: Hardware** section for recommended application circuit.



IR LED Characteristics, V_{DD} = 3 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_F	Forward Voltage	I_F = 20 mA		1.4	1.5	V
V_R	Reverse Voltage	I_R = 10 μA	5			V
P_O	Radiant Power	I_F = 20 mA	4.5			mW
λ_p	Peak Wavelength	I_F = 20 mA		850		nm
Δ_λ	Spectral Radiation Bandwidth	I_F = 20 mA		40		nm
T_R	Optical Rise Time	I_F = 100 mA, T_W = 125 ns, duty cycle = 25%		20	40	ns
T_F	Optical Fall Time	I_F = 100 mA, T_W = 125 ns, duty cycle = 25%		20	40	ns

Persistence Filter Register (0x0C)

The persistence filter register controls the interrupt capabilities of the device. Configurable filtering is provided to allow interrupts to be generated after every ADC cycle or if the ADC cycle has produced a result that is outside of the values specified by threshold register for some specified amount of time. Separate filtering is provided for proximity and ALS functions. ALS interrupts are generated using C0DATA.

Table 11. Persistence Filter Register

	7	6	5	4	3	2	1	0	
PERS	PPERS				APERS				Reset 0x00

FIELD	BITS	DESCRIPTION		
PPERS	7:4	Proximity interrupt persistence filter. Controls rate of proximity interrupt to the host processor.		
		FIELD VALUE	**MEANING**	**INTERRUPT PERSISTENCE FUNCTION**
		0000	–––	Every proximity cycle generates an interrupt
		0001	1	1 proximity value out of range
		0010	2	2 consecutive proximity values out of range
		...	...	...
		1111	15	15 consecutive proximity values out of range
APERS	3:0	ALS Interrupt persistence filter. Controls rate of ALS interrupt to the host processor.		
		FIELD VALUE	**MEANING**	**INTERRUPT PERSISTENCE FUNCTION**
		0000	Every	Every ALS cycle generates an interrupt
		0001	1	1 value outside of threshold range
		0010	2	2 consecutive values out of range
		0011	3	3 consecutive values out of range
		0100	5	5 consecutive values out of range
		0101	10	10 consecutive values out of range
		0110	15	15 consecutive values out of range
		0111	20	20 consecutive values out of range
		1000	25	25 consecutive values out of range
		1001	30	30 consecutive values out of range
		1010	35	35 consecutive values out of range
		1011	40	40 consecutive values out of range
		1100	45	45 consecutive values out of range
		1101	50	50 consecutive values out of range
		1110	55	55 consecutive values out of range
		1111	60	60 consecutive values out of range

Configuration Register (0x0D)

The configuration register sets the proximity LED drive level, wait long time, and ALS gain level.

Table 12. Configuration Register

	7	6	5	4	3	2	1	0	
CONFIG	**Reserved**					**AGL**	**WLONG**	**PDL**	**Reset 0x00**

FIELD	BITS	DESCRIPTION
Reserved	7:3	Reserved. Write as 0.
AGL	2	ALS gain level. When asserted, the 1× and 8× ALS gain (AGAIN) modes are scaled by 0.16. Otherwise, AGAIN is scaled by 1. Do not use with AGAIN greater than 8×.
WLONG	1	Wait Long. When asserted, the wait cycles are increased by a factor 12× from that programmed in the WTIME register.
PDL	0	Proximity drive level. When asserted, the proximity LDR drive current is reduced by 9.

Proximity Pulse Count Register (0x0E)

The proximity pulse count register sets the number of proximity pulses that the LDR pin will generate during the Prox Accum state. The pulses are generated at a 62.5-kHz rate.

Table 13. Proximity Pulse Count Register

	7	6	5	4	3	2	1	0	
PPULSE	**PPULSE**								**Reset 0x00**

FIELD	BITS	DESCRIPTION
PPULSE	7:0	Proximity Pulse Count. Specifies the number of proximity pulses to be generated.

Control Register (0x0F)

The Control register provides eight bits of miscellaneous control to the analog block. These bits typically control functions such as gain settings and/or diode selection.

Table 14. Control Register

	7	6	5	4	3	2	1	0	
CONTROL	PDRIVE		PDIODE		PGAIN		AGAIN		Reset 0x00

FIELD	BITS	DESCRIPTION		
PDRIVE (Note 1)	7:6	Proximity LED Drive Strength.		
		FIELD VALUE	**LED STRENGTH — PDL = 0**	**LED STRENGTH — PDL = 1**
		00	*100 mA*	*11.1 mA*
		01	*50 mA*	*5.6 mA*
		10	*25 mA*	*2.8 mA*
		11	*12.5 mA*	*1.4 mA*
PDIODE	5:4	Proximity Diode Selector.		
		FIELD VALUE	**DIODE SELECTION**	
		00	Proximity uses neither diode	
		01	Proximity uses the CH0 diode	
		10	Proximity uses the CH1 diode	
		11	Reserved — Do not write	
PGAIN	3:2	Proximity Gain.		
		FIELD VALUE	**PROXIMITY GAIN VALUE**	
		00	1× gain	
		01	2× gain	
		10	4× gain	
		11	8× gain	
AGAIN	1:0	ALS Gain.		
		FIELD VALUE	**ALS GAIN VALUE**	
		00	1× gain	
		01	8× gain	
		10	16× gain	
		11	120× gain	

NOTE 1: LED STRENGTH values (italic) are nominal operating values. Specifications can be found in the Proximity Characteristics table.

Revision Register (0x11)

The Revision register shows the silicon revision number. It is a read-only register and shows the revision level of the silicon used internally.

Table 15. Revision Register

	7	6	5	4	3	2	1	0	
REVISION	Reserved				DIE_REV				Reset Rev Num

FIELD	BITS	DESCRIPTION	
Reserved	7:4	Reserved	Bits read as 0
DIE_REV	3:0	Die revision number	Die revision number

ID Register (0x12)

The ID Register provides the value for the part number. The ID register is a read-only register.

Table 16. ID Register

	7	6	5	4	3	2	1	0	
ID	ID								Reset ID

FIELD	BITS	DESCRIPTION	
ID	7:0	Part number identification	0x30 = TMD27721
			0x39 = TMD27723

Status Register (0x13)

The Status Register provides the internal status of the device. This register is read only.

Table 17. Status Register

	7	6	5	4	3	2	1	0	
STATUS	Reserved	PSAT	PINT	AINT	Reserved		PVALID	AVALID	Reset 0x00

FIELD	BIT	DESCRIPTION
Reserved	7	Reserved. Bit reads as 0.
PSAT	6	Proximity Saturation. Indicates that the proximity measurement saturated.
PINT	5	Proximity Interrupt. Indicates that the device is asserting a proximity interrupt.
AINT	4	ALS Interrupt. Indicates that the device is asserting an ALS interrupt.
Reserved	3:2	Reserved. Bits read as 0.
PVALID	1	Proximity Valid. Indicates that the proximity channel has completed an integration cycle after PEN has been asserted.
AVALID	0	ALS Valid. Indicates that the ALS channels have completed an integration cycle after AEN has been asserted.

ADC Channel Data Registers (0x14 – 0x17)

ALS data is stored as two 16-bit values. To ensure the data is read correctly, a two-byte read I^2C transaction should be used with auto increment protocol bits set in the command register. With this operation, when the lower byte register is read, the upper eight bits are stored in a shadow register, which is read by a subsequent read to the upper byte. The upper register will read the correct value even if additional ADC integration cycles end between the reading of the lower and upper registers.

Table 18. ADC Channel Data Registers

REGISTER	ADDRESS	BITS	DESCRIPTION
C0DATA	0x14	7:0	ALS CH0 data low byte
C0DATAH	0x15	7:0	ALS CH0 data high byte
C1DATA	0x16	7:0	ALS CH1 data low byte
C1DATAH	0x17	7:0	ALS CH1 data high byte

Proximity Data Registers (0x18 – 0x19)

Proximity data is stored as a 16-bit value. To ensure the data is read correctly, a two-byte read I^2C transaction should be utilized with auto increment protocol bits set in the command register. With this operation, when the lower byte register is read, the upper eight bits are stored into a shadow register, which is read by a subsequent read to the upper byte. The upper register will read the correct value even if the next ADC cycle ends between the reading of the lower and upper registers.

Table 19. Proximity Data Registers

REGISTER	ADDRESS	BITS	DESCRIPTION
PDATAL	0x18	7:0	Proximity data low byte
PDATAH	0x19	7:0	Proximity data high byte

Proximity Offset Register (0x1E)

The 8-bit proximity offset register provides compensation for proximity offsets caused by device variations, optical crosstalk, and other environmental factors. Proximity offset is a sign-magnitude value where the sign bit, bit 7, determines if the offset is negative (bit 7 = 0) or positive (bit 7 = 1). At power up, the register is set to 0x00. The magnitude of the offset compensation depends on the proximity gain (PGAIN), proximity LED drive strength (PDRIVE), and the number of proximity pulses (PPULSE). Because a number of environmental factors contribute to proximity offset, this register is best suited for use in an adaptive closed-loop control system. See available TAOS application notes for proximity offset register application information.

Table 20. Proximity Offset Register

	7	6	5	4	3	2	1	0	
POFFSET	SIGN	MAGNITUDE							Reset 0x00

FIELD	BIT	DESCRIPTION
SIGN	7	Proximity Offset Sign. The offset sign shifts the proximity data negative when equal to 0 and positive when equal to 1.
MAGNITUDE	6:0	Proximity Offset Magnitude. The offset magnitude shifts the proximity data positive or negative, depending on the proximity offset sign. The actual amount of the shift depends on the proximity gain (PGAIN), proximity LED drive strength (PDRIVE), and the number of proximity pulses (PPULSE).

APPLICATION INFORMATION: HARDWARE

LED Driver Pin with Proximity Detection

In a proximity sensing system, the included IR LED can be pulsed with more than 100 mA of rapidly switching current, therefore, a few design considerations must be kept in mind to get the best performance. The key goal is to reduce the power supply noise coupled back into the device during the LED pulses. Averaging of multiple proximity samples is recommended to reduce the proximity noise.

The first recommendation is to use two power supplies; one for the device V_{DD} and the other for the IR LED. In many systems, there is a quiet analog supply and a noisy digital supply. By connecting the quiet supply to the V_{DD} pin and the noisy supply to the LEDA pin, the key goal can be met. Place a 1-µF low-ESR decoupling capacitor as close as possible to the V_{DD} pin and another at the LEDA pin, and at least 10-µF of bulk capacitance to supply the 100-mA current surge. This may be distributed as two 4.7 µF capacitors.

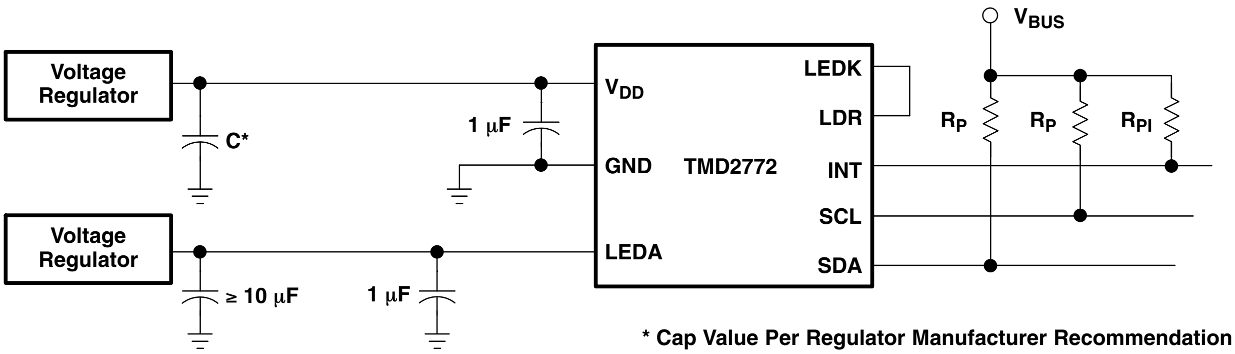


Figure 13. Proximity Sensing Using Separate Power Supplies

If it is not possible to provide two separate power supplies, the device can be operated from a single supply. A 22-Ω resistor in series with the V_{DD} supply line and a 1-µF low ESR capacitor effectively filter any power supply noise. The previous capacitor placement considerations apply.

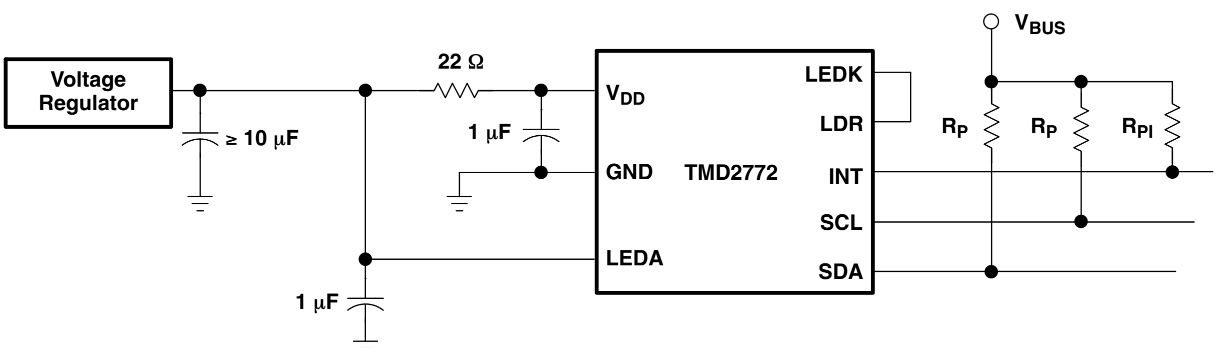


Figure 14. Proximity Sensing Using Single Power Supply

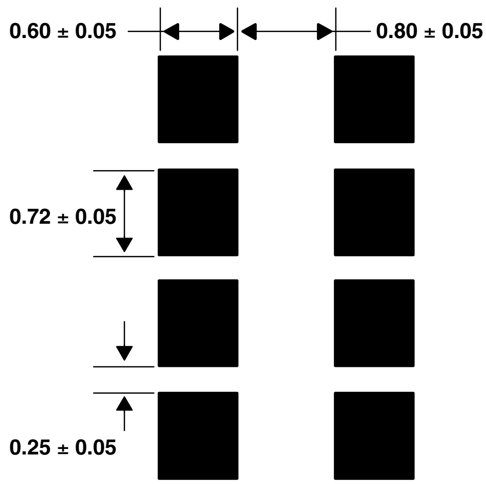
V_{BUS} in the above figures refers to the I^2C bus voltage which is either V_{DD} or 1.8 V. Be sure to apply the specified I^2C bus voltage shown in the Available Options table for the specific device being used.

The I^2C signals and the Interrupt are open-drain outputs and require pull−up resistors. The pull-up resistor (R_P) value is a function of the I^2C bus speed, the I^2C bus voltage, and the capacitive load. The TAOS EVM running at 400 kbps, uses 1.5-kΩ resistors. A 10-kΩ pull-up resistor (R_{PI}) can be used for the interrupt line.

APPLICATION INFORMATION: HARDWARE

PCB Pad Layout

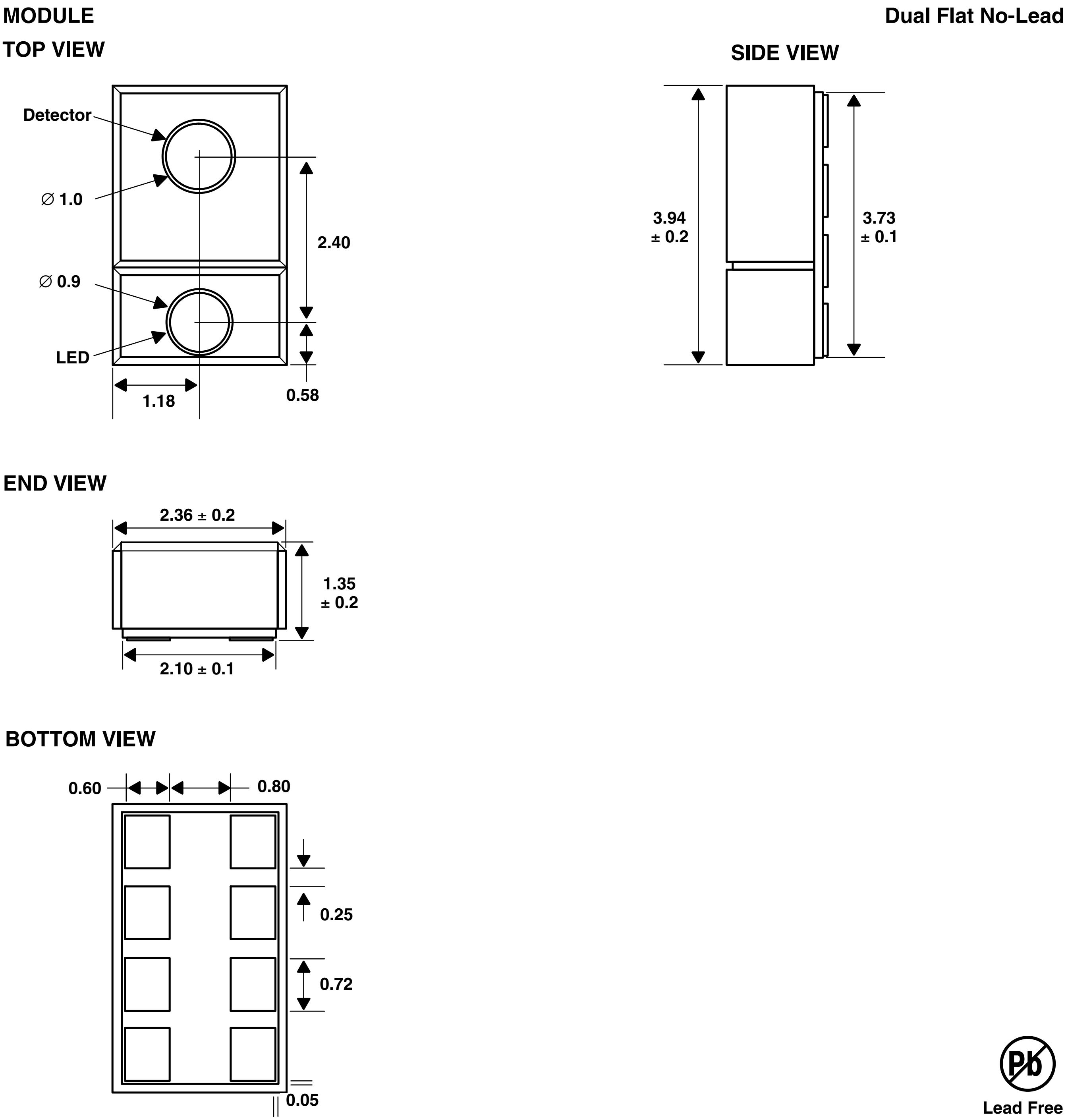
Suggested PCB pad layout guidelines for the surface mount module are shown in Figure 15. Flash Gold is recommended surface finish for the landing pads.



NOTES: A. All linear dimensions are in mm.
B. This drawing is subject to change without notice.

Figure 15. Suggested Module PCB Layout

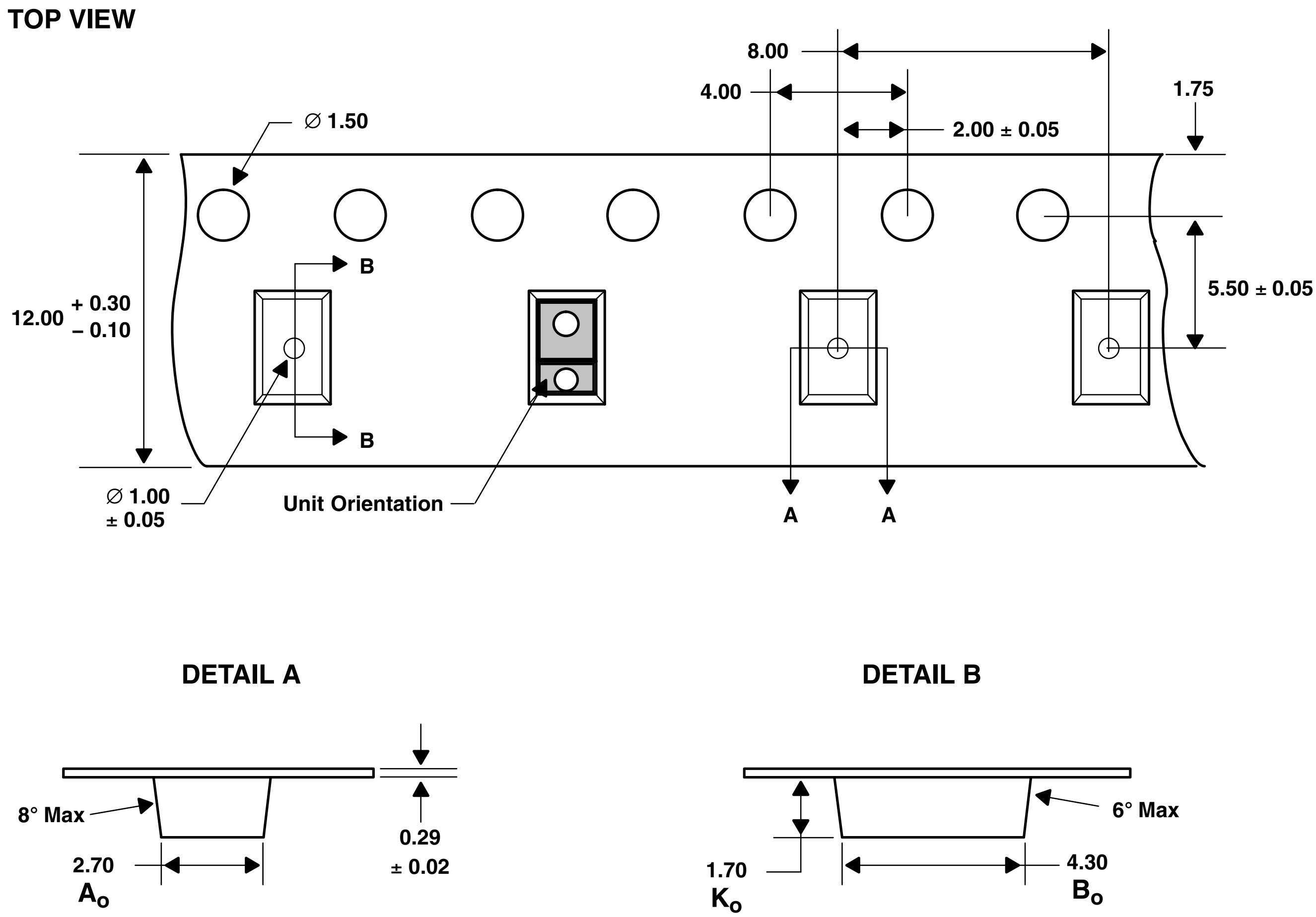
PACKAGE INFORMATION



NOTES: A. All linear dimensions are in millimeters. Dimension tolerance is ± 0.05 mm unless otherwise noted.
B. Contacts are copper with NiPdAu plating.
C. This package contains no lead (Pb).
D. This drawing is subject to change without notice.

Figure 16. Module Packaging Configuration

CARRIER TAPE AND REEL INFORMATION



NOTES:
- A. All linear dimensions are in millimeters. Dimension tolerance is ± 0.10 mm unless otherwise noted.
- B. The dimensions on this drawing are for illustrative purposes only. Dimensions of an actual carrier may vary slightly.
- C. Symbols on drawing A_o, B_o, and K_o are defined in ANSI EIA Standard 481−B 2001.
- D. Each reel is 330 millimeters in diameter and contains 2500 parts.
- E. TAOS packaging tape and reel conform to the requirements of EIA Standard 481−B.
- F. In accordance with EIA standard, device pin 1 is located next to the sprocket holes in the tape.
- G. This drawing is subject to change without notice.

Figure 17. Module Carrier Tape

SOLDERING INFORMATION

The module has been tested and has demonstrated an ability to be reflow soldered to a PCB substrate.

The solder reflow profile describes the expected maximum heat exposure of components during the solder reflow process of product on a PCB. Temperature is measured on top of component. The components should be limited to a maximum of three passes through this solder reflow profile.

Table 21. Solder Reflow Profile

PARAMETER	REFERENCE	DEVICE
Average temperature gradient in preheating		2.5°C/sec
Soak time	t_{soak}	2 to 3 minutes
Time above 217°C (T_1)	t_1	Max 60 sec
Time above 230°C (T_2)	t_2	Max 50 sec
Time above T_{peak} –10°C (T_3)	t_3	Max 10 sec
Peak temperature in reflow	T_{peak}	260°C
Temperature gradient in cooling		Max –5°C/sec

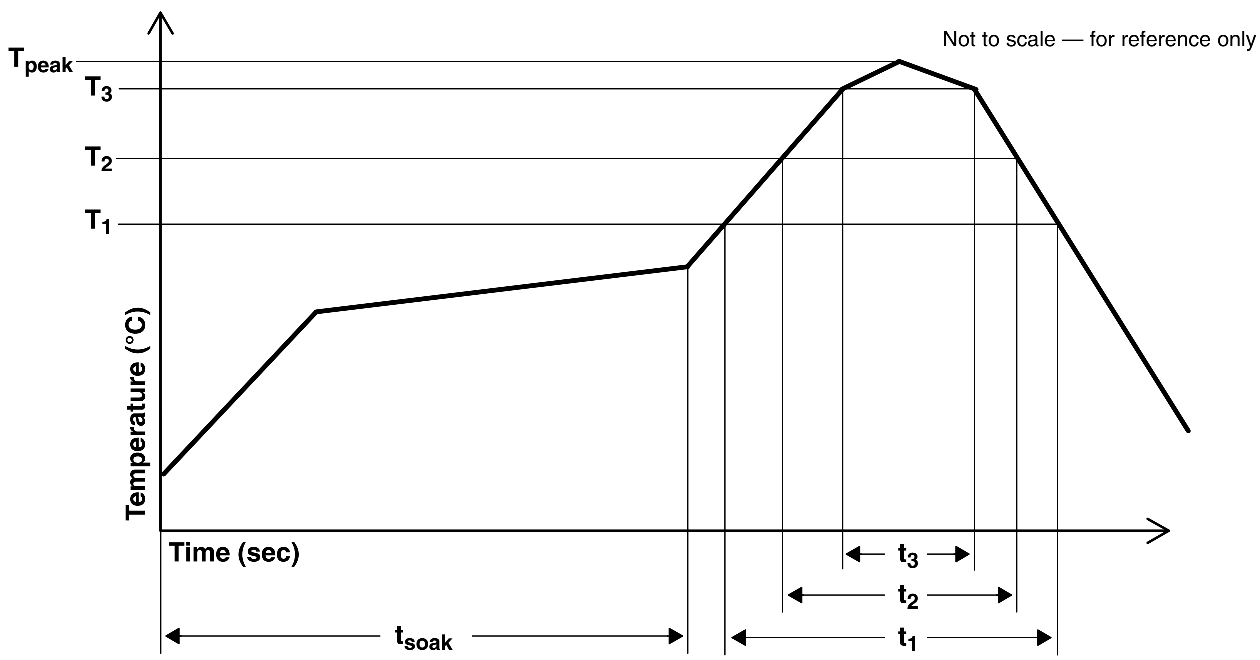


Figure 18. Solder Reflow Profile Graph

STORAGE INFORMATION

Moisture Sensitivity

Optical characteristics of the device can be adversely affected during the soldering process by the release and vaporization of moisture that has been previously absorbed into the package. To ensure the package contains the smallest amount of absorbed moisture possible, each device is baked prior to being dry packed for shipping. Devices are dry packed in a sealed aluminized envelope called a moisture-barrier bag with silica gel to protect them from ambient moisture during shipping, handling, and storage before use.

Shelf Life

The calculated shelf life of the device in an unopened moisture barrier bag is 12 months from the date code on the bag when stored under the following conditions:

Shelf Life: 12 months
Ambient Temperature: < 40°C
Relative Humidity: < 90%

Rebaking of the devices will be required if the devices exceed the 12 month shelf life or the Humidity Indicator Card shows that the devices were exposed to conditions beyond the allowable moisture region.

Floor Life

The module has been assigned a moisture sensitivity level of MSL 3. As a result, the floor life of devices removed from the moisture barrier bag is 168 hours from the time the bag was opened, provided that the devices are stored under the following conditions:

Floor Life: 168 hours
Ambient Temperature: < 30°C
Relative Humidity: < 60%

If the floor life or the temperature/humidity conditions have been exceeded, the devices must be rebaked prior to solder reflow or dry packing.

Rebaking Instructions

When the shelf life or floor life limits have been exceeded, rebake at 50°C for 12 hours.

PRODUCTION DATA — information in this document is current at publication date. Products conform to specifications in accordance with the terms of Texas Advanced Optoelectronic Solutions, Inc. standard warranty. Production processing does not necessarily include testing of all parameters.

LEAD-FREE (Pb-FREE) and GREEN STATEMENT

Pb-Free (RoHS) TAOS' terms *Lead-Free* or *Pb-Free* mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TAOS Pb-Free products are suitable for use in specified lead-free processes.

Green (RoHS & no Sb/Br) TAOS defines *Green* to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material).

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