200 kSPS, 8-Channel, Simultaneous Sampling, Bipolar 16-Bit ADC

Preliminary Technical Data

AD7606

FEATURES

Eight Simultaneously Sampled Inputs
True bipolar analog input ranges: ±10 V, ±5 V
Single 5V Analog Supply, 1.8V to +5V V_{DRIVE}
1MΩ Analog Input Impedance
Analog Input Clamp Protection
2nd Order Anti-alias Analog Filter
Fast throughput rate: 200 kSPS for all 8 channels
90dB typ SNR at 200ksps
Over-sampling capability with digital filter, e.g. 93dB typ SNR at 50ksps
Low power: 100 mW typ at 200 kSPS
On-chip accurate reference and reference buffer
Flexible Parallel/Serial interface:
SPI®-/QSPI™-/MICROWIRE™-/DSP-compatible
Standby Mode: 6 mW typ
64-lead LQFP Package

APPLICATIONS

Power line monitoring and protection systems
Multiphase Motor Control
Instrumentation and control systems
Multi-axis positioning systems
Data Acquisition Systems

GENERAL DESCRIPTION

The AD7606[1] is an eight channel simultaneously sampled 16-bit ADC. The AD7606 is capable of achieving a sampling rate of 200 ksps per channel. The input signals are sampled simultaneously thus preserving the relative phase information of the signals on the input channels. The part operates from a 5V supply and can accommodate ± 10V and ±5V true bipolar input signals. The part contains on-chip LDOs, reference and reference buffer, track and hold circuitry, supply conditioning circuitry, on-chip conversion clock, oversampling capability and high speed parallel and serial interfaces.

The AD7606 features throughput rates up to 200 kSPS per channel. The part contains low noise, high input impedance signal scaling amplifiers that can handle input frequencies in the region of 5 to10 Khz. The AD7606 features a front-end anti-alias filter with attenuation of approximately 40dB while sampling at 200kSPS. The conversion process and data acquisition are controlled using CONVST signals and an internal oscillator. Two CONVST pins allow the simultaneous sampling of all eight analog inputs or two groups of four analog input channels. The AD7606 provides over sampling capability. Over sampling is optional to achieve improved noise performance and reduced output code spread for lower throughput rates.

FUNCTIONAL BLOCK DIAGRAM

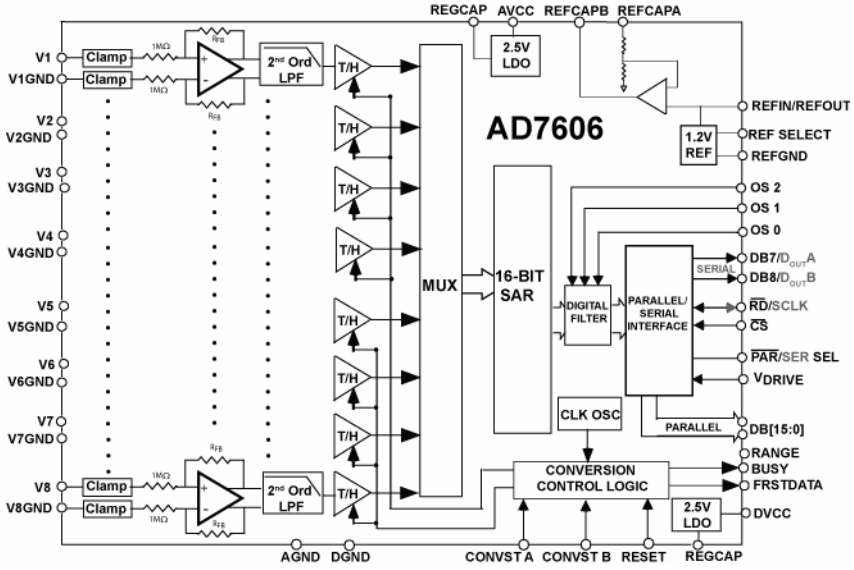

Figure 1.

[1] Patent Pending

Rev. PrG

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SPECIFICATIONS

V_{REF} = 1.2V external/ 4.5 V internal, AV_{CC} = 4.75 V to 5.25 V, DV_{CC} = 4.75 V to 5.25 V, V_{DRIVE} = 1.8 V to 5.25 V; f_{SAMPLE} = 200 kSPS, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.[1]

Table 1.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE	f_{IN} = 1 kHz sine wave				
Signal-to-Noise + Distortion (SINAD)[2]		87			dB
			90		dB
Signal-to-Noise Ratio (SNR)[2]		88			dB
			90		dB
Total Harmonic Distortion (THD)[2]				−90	dB
			−100		dB
Peak Harmonic or Spurious Noise (SFDR)[2]			−100		dB
Intermodulation Distortion (IMD)[2]	fa = 4 kHz, fb = 4.1 kHz				
Second-Order Terms			−112		dB
Third-Order Terms			−107		dB
Channel-to-Channel Isolation[2]	f_{IN} on unselected channels up to 2 kHz		−100		dB
Full Power Bandwidth	@ −3 dB		10		kHz
	@ −0.1 dB		1		kHz
DC ACCURACY					
Resolution	No Missing Codes	16			Bits
Integral Nonlinearity[2]			±1	±2.5	LSB
Positive Full-Scale Error[2]			±1		% FS
Positive Full-Scale Error Matching[2]			±0.5		% FS
Bipolar Zero-Scale Error[2]			±0.01		% FS
Bipolar Zero-Scale Error Matching[2]			±0.01		% FS
Negative Full-Scale Error[2]			±1		% FS
Negative Full-Scale Error Matching[2]			±0.5		% FS
ANALOG INPUT					
Input Voltage Ranges	RANGE = 1			±10	V
	RANGE = 0			±5	V
DC Leakage Current				±1	µA
Input Capacitance[3]			20		pF
Input Impedance	See Analog input section		1		MΩ
REFERENCE INPUT/OUTPUT					
Reference Input Voltage Range			1.2		V
DC Leakage Current				±1	µA
Input Capacitance[3]	REF SELECT= 1		18.5		pF
Reference Output Voltage			1.2		V
Reference Temperature Coefficient			±10		ppm/°C
LOGIC INPUTS					
Input High Voltage (V_{INH})		0.7×V_{DRIVE}			V
Input Low Voltage (V_{INL})				0.3 ×V_{DRIVE}	V
Input Current (I_{IN})	Typically 10 nA, V_{IN} = 0 V or V_{DRIVE}			±1	µA
Input Capacitance (C_{IN})[3]				5	pF
LOGIC OUTPUTS					
Output High Voltage (V_{OH})	I_{SOURCE} = 200 µA	V_{DRIVE} − 0.2			V
Output Low Voltage (V_{OL})	I_{SINK} = 200 µA			0.2	V
Floating-State Leakage Current				±1	µA
Floating-State Output Capacitance[3]				10	pF

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
Output Coding	2's Complement				
CONVERSION RATE					
Conversion Time	All 8 channels included			4	µs
Track-and-Hold Acquisition Time[2, 3]				1	µs
Throughput Rate	Per channel, all 8 channels included			200	kSPS
POWER REQUIREMENTS					
AV_{CC}		4.75		5.25	V
DV_{CC}		4.75		5.25	V
V_{DRIVE}		1.8		5.25	V
I_{TOTAL}	Digital I/P_S = 0 V or V_{DRIVE}				
Normal Mode (Static)	AV_{CC} = DV_{CC} = V_{DRIVE} = 5.25 V		18	22	mA
Normal Mode (Operational)	f_{SAMPLE} = 200 kSPS, AV_{CC} = DV_{CC} = V_{DRIVE} = 5.25 V		19.5	24	mA
Standby Mode	AV_{CC} = DV_{CC} = V_{DRIVE} = 5.25 V		1.2	1.4	mA
Power Dissipation	AV_{CC} = DV_{CC} = V_{DRIVE} = 5.25 V				
Normal Mode (Static)			94.5	115	mW
Normal Mode (Operational)	f_{SAMPLE} = 200 kSPS		102	126	mW
Standby Mode			6.3	7.35	mW

[1] Temperature range for B version is −40°C to +85°C.
[2] See the Terminology section.
[3] Sample tested during initial release to ensure compliance.

TIMING SPECIFICATIONS

AV_{CC}/DV_{CC} = 4.75 V to 5.25 V, V_{DRIVE} = 1.8V to 5.25 V, V_{REF} = 1.2V external reference/ internal reference, $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted.[1]

Table 2.

Parameter	Limit at T_{MIN}, T_{MAX}		Unit	Description
	V_{DRIVE} < 4.75 V	V_{DRIVE} = 4.75 V to 5.25 V		
PARALLEL/ SERIAL MODE				
t_{CONV}	4	4	µs max	Conversion time, internal clock. Oversampling Off.
	(4×OSR) + (t_{ACQ} × (OSR-1))			Conversion time, internal clock. Oversampling On. OSR = Oversampling Rate.
t_{QUIET}	150	150	ns min	Minimum quiet time required between bus relinquish and start of next conversion
t_{ACQ}	1	1	µs max	
$t_{WAKE-UP}$	500	500	µs max	$\overline{STBY}$ rising edge to CONVST rising edge
	550	550	µs max	Power up time from when supplies first applied.
t_1	60	60	ns min	CONVST high to BUSY high
t_2	25	25	ns min	Minimum CONVST low pulse
t_3	15	15	ns min	BUSY falling edge to CS falling edge set-up time
PARALLEL READ OPERATION				
t_4	0	0	ns min	$\overline{CS}$ to $\overline{RD}$ setup time
t_5	0	0	ns min	$\overline{CS}$ to $\overline{RD}$ hold time
t_6	20	20	ns min	$\overline{RD}$ pulse width
t_7	20	20	ns max	Data access time after $\overline{RD}$ falling edge
t_8	7	7	ns min	Data hold time after $\overline{RD}$ rising edge
t_9	12	12	ns max	Bus relinquish time after $\overline{CS}$ rising edge
t_{10}	10	10	ns min	Minimum time between reads
t_{11}	12	12	ns min	Minimum time between rising and falling edge of $\overline{CS}$
t_{12}	9.5	9.5	ns max	Delay from $\overline{CS}$ until DB[15:0] three-state disabled
SERIAL READ OPERATION				
f_{SCLK}	40	40	MHz max	Frequency of serial read clock
t_{13}	9.5	9.5	ns max	Delay from $\overline{CS}$ until $D_{OUT}A$/ $D_{OUT}B$ three-state disabled
	9.5	9.5	ns max	Delay from $\overline{CS}$ until MSB valid
t_{14}[2]	20	20	ns max	Data access time after SCLK rising edge
t_{15}	0.4 t_{SCLK}	0.4 t_{SCLK}	ns min	SCLK low pulse width
t_{16}	0.4 t_{SCLK}	0.4 t_{SCLK}	ns min	SCLK high pulse width
t_{17}	7	7	ns min	SCLK to data valid hold time after SCLK falling edge
t_{18}	12	12	ns max	$\overline{CS}$ rising edge to $D_{OUT}A$/ $D_{OUT}B$ high impedance
READING DURING CONVERSION				
t_{19}	15	15	ns min	BUSY to $\overline{CS}$ setup time
t_{20}	15	15	ns min	BUSY to $\overline{CS}$ hold time

[1] Sample tested during initial release to ensure compliance. All input signals are specified with $t_R = t_F$ = 5 ns (10% to 90% of V_{DD}) and timed from a voltage level of 1.6 V.
[2] A buffer is used on the data output pins for this measurement.

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted

Table 3.

Parameter	Rating
AV_{CC} to AGND, DGND	−0.3 V to +7 V
DV_{CC} to AV_{CC}	−0.3 V to AV_{CC} + 0.3 V
DV_{CC} to DGND, AGND	−0.3 V to +7 V
AGND to DGND	−0.3 V to +0.3 V
V_{DRIVE} to DGND	−0.3 V to +DV_{CC} + 0.3 V
Analog Input Voltage to AGND[1]	TBD
Digital Input Voltage to DGND	−0.3 V to V_{DRIVE} + 0.3 V
Digital Output Voltage to GND	−0.3 V to V_{DRIVE} + 0.3 V
REFIN to AGND	−0.3 V to AV_{CC} + 0.3 V
Input Current to Any Pin Except Supplies[1]	±10 mA
Operating Temperature Range	
B Version	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C
Pb/SN Temperature, Soldering	
Reflow (10 sec to 30 sec)	240(+0)°C
Pb-Free Temperature, Soldering Reflow	260(+0)°C
ESD	TBD kV

[1] Transient currents of up to 100 mA do not cause SCR latch-up.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages. These specifications apply to a four-layer board.

Table 4. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
64 LQFP	45	11	°C /W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

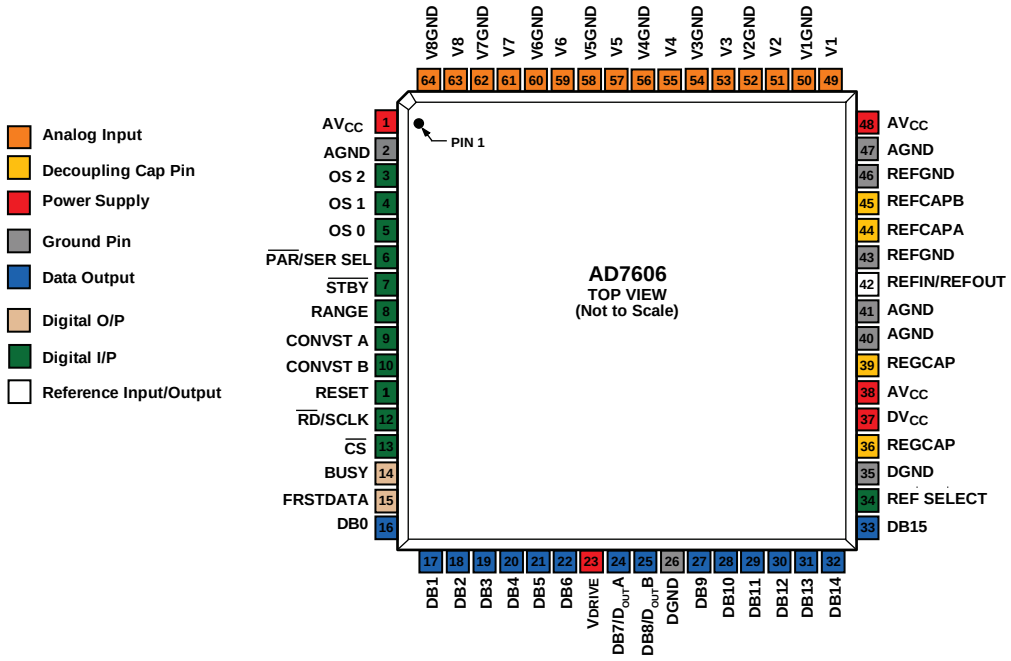

Figure 2. Pin Configuration

Table 5. Pin Function Descriptions

Pin No.	Type[1]	Mnemonic	Description
1, 38, 48	P	AV_{CC}	Analog Supply Voltage 4.75V to 5.25V. This supply voltage is applied to the internal front end amplifiers and to the ADC core. The AV_{CC} and DV_{CC} voltages should ideally be at the same potential and must not be more than 0.3 V apart, even on a transient basis. These supply pins should be decoupled to AGND.
2, 40, 41, 47	P	AGND	Analog ground. This pin is the ground reference point for all analog circuitry on the AD7606. All analog input signals and external reference signals should be referred to this pin. All four of these AGND pins should be connected to the AGND plane of a system. The AGND and DGND voltages should ideally be at the same potential and must not be more than 0.3 V apart, even on a transient basis.
37	P	DV_{CC}	Digital Supply Voltage 4.75V to 5.25V. The DV_{CC} and AV_{CC} voltages should ideally be at the same potential and must not be more than 0.3 V apart, even on a transient basis. This supply should be decoupled to DGND
26, 35	P	DGND	Digital Ground. This is the ground reference point for all digital circuitry on the AD7606. Both DGND pins should connect to the DGND plane of a system. The DGND and AGND voltages should ideally be at the same potential and must not be more than 0.3 V apart, even on a transient basis.
23	P	V_{DRIVE}	Logic Power Supply Input. The voltage (1.8V to 5V) supplied at this pin determines the operating voltage of the interface. This pin is nominally at the same supply as the supply of the host interface (i.e. DSP, FPGA).
36, 39	P	REGCAP	Decoupling capacitor pins for voltage output from internal regulator. These output pins should be decoupled separately to AGND using a 1µF capacitor. The voltage on these output pins is in the range of 2.5V to 2.7V.
49, 51, 53, 55, 57, 59, 61, 63	A.I.	V1 to V8	Analog Input 1 to Analog Input 8. These pins are single-ended analog inputs. The analog input range of these channels is determined by the RANGE pin
50, 52, 54 ,56 58, 60, 62, 64.	A.I.	V1GND to V8GND	Analog input ground pins corresponding to the analog input pins V1 to V8. All eight of these AGND pins should be connected to the AGND plane of a system.
42	REF	REFIN/REFOUT	Reference Input/ Reference Output. The on-chip reference of 1.2V is available on this pin for if the REF SELECT pin is set to a logic high. Alternatively, the internal reference can be disabled be setting the REF SELECT pin to a logic low and an external reference of 1.2V can be applied to this input. See the INternal/external Reference section. Decoupling is required on this pin for both the internal or external reference options. A 1uF

[1]Refers to classification of pin type; P denotes power, A.I. denotes analog input, REF denotes reference, D.I. denotes digital input, D.O. denotes digital output.

Pin No.	Type[1]	Mnemonic	Description
			capacitor should be applied from this pin to ground close to the REFGND pins.
34	D.I.	REF SELECT	Internal/ External reference selection input. Logic input. If this pin is set to logic high then the internal reference is selected and is enabled, if this pin is set to logic low then the internal reference is disabled and an external reference voltage must be applied to the REFIN/REFOUT pin.
44, 45	REF	REFCAPA, REFCAPB	Reference buffer output force/sense pins. These pins must be connected together and decoupled to AGND using a low ESR 10µF capacitor.
43, 46	REF	REFGND	Reference ground pins. These should be shorted together and connected to AGND.
8	D.I.	RANGE	Analog Input Range Selection. Logic input. The polarity on this pin determines the input range of the analog input channels. If this pin is tied to a logic high, the analog input range is ±10V for all channels, V1 to V8. If this pin is tied to a logic low, the analog input range is ±5V for all channels, V1 to V8. A logic change on this pin will have an immediate effect on the analog input range. Changing this pin during a conversion is not recommended. See Analog Input section for more details.
6	D.I.	$\overline{PAR}$/SER SEL	Parallel/serial interface selection input. Logic input. If this pin is tied to a logic low, the parallel interface is selected. If this pin is tied to a logic high, the serial interface is selected. When the serial interface is selected: $\overline{RD}$/SCLK pin functions as the Serial Clock input. DB7/D_{OUT}A pin functions as a Serial Data Output.. DB8/D_{OUT}B pin functions as a Serial Data Output.. When the serial interface is selected pins DB[15:9] and DB[6:0] should be tied to DGND.
9, 10	D.I.	CONVST A CONVST B	Conversion Start Input A, Conversion Start Input B. Logic inputs. These logic inputs are used to initiate conversions on the analog input channels. For simultaneous sampling of all 8 input channels CONVST A and CONVST B can be shorted together and a single convert start signal applied. Alternatively, CONVST A can be used to initiate simultaneous sampling for the first 4 analog inputs; (V1, V2, V3 and V4) and CONVST B can be used to initiate simultaneous sampling on the other four analog inputs; (V5, V6, V7 and V8). This is only possible when oversampling is not switched on. When the CONVST A or CONVST B pins transitions from low to high, the front end track and hold circuitry for analog inputs V1 to V4, or V5 to V8 respectively is set to hold. This function allows a phase delay to be created inherently between the sampling instants of channels V1 to V4 and channels V5 to V8.
13	D.I.	$\overline{CS}$	Chip Select. This active low logic input frames the data transfer. When both $\overline{CS}$ and $\overline{RD}$ are logic low in parallel mode, the output bus DB[15:0] is enabled and the conversion result is output on the parallel data bus lines. In serial mode, the $\overline{CS}$ is used to frame the serial read transfer and clock out the MSB of the serial output data.
12	D.I.	$\overline{RD}$/SCLK	Parallel Data Read control input when parallel interface selected. Serial clock input when the serial interface is selected. When both $\overline{CS}$ and $\overline{RD}$ are logic low in parallel mode, the output bus is enabled. In serial mode this pin acts as the serial clock input for data transfers. The $\overline{CS}$ falling edge takes the data output lines D_{OUT}A and D_{OUT}B out of tri-state and clocks out the MSB of the conversion result. The rising edge of SCLK clocks all subsequent data bits onto the serial data outputs D_{OUT}A and D_{OUT}B. See DIGITAL Interface for more information.
14	D.O.	BUSY	Busy Output. This pin transitions to a logic high after both CONVST A and CONVST B rising edges and indicates that the conversion process has started. The BUSY output remains high until the conversion process for all eight channels is complete. The falling edge of BUSY signals that the conversion data is being latched into the output data registers and will be available to be read after a time t_2 or t_{22}. Any data read while BUSY is high should be complete before the falling edge of BUSY occurs or unread data will be lost. Rising edges on CONVST A or CONVST B will have no effect whilst the BUSY signal is high.
11	D.I.	RESET	RESET input. When set to logic high, the rising edge of RESET resets the AD7606. The AD7606 should receive a RESET pulse after power-up. The RESET high pulse should be typically 100 ns wide. If a RESET pulse is applied during a conversion then the conversion is aborted. If a RESET pulse is applied during a read then contents of the output registers will reset to all zeros.
15	D.O.	FRSTDATA	Digital output. The FRSTDATA output signal indicates when the first channel, V1, is being read back on either the parallel or serial interface. When the $\overline{CS}$ input is high the FRSTDATA output pin is in three-state. The falling edge of $\overline{CS}$ takes FRSTDATA out of three-state. In parallel mode the falling edge of $\overline{RD}$ corresponding to the result of V1 will then set the FRSTDATA pin high indicating that the result from V1 is available on the output data bus. The FRSTDATA output

Pin No.	Type[1]	Mnemonic	Description
			returns to a logic low following the next falling edge of RD. In serial mode FRSTDATA will go high on the falling edge of $\overline{CS}$ as this clocks out the MSB of V1 on $D_{OUT}A$. It returns low on the sixteenth SCLK falling edge after the $\overline{CS}$ falling edge. See DIGITAL Interface for more details.
7	D.I.	$\overline{STBY}$	Standby Mode Input. This pin is used to place the AD7606 in Standby mode. When this pin is low all circuitry except the on-chip regulators and regulator buffers is powered down. The $\overline{STBY}$ pin is high for normal operation and low for standby operation.
3,4,5	D.I.	OS [2: 0]	Over-sampling mode pins. Logic inputs. These inputs are used to select the over-sampling ratio. OS 2 is the MSB control bit while OS 0 is the LSB control bit. See the Over sampling Mode section for further details on the over-sampling mode of operation and **Table 7** for over-sampling bit decoding.
33 to 27	D.O.	DB[15: 9]	Parallel output data bits, Data Bit15 to Data Bit 9. When $\overline{PAR}$/SER SEL = 0, these pins act as three-state parallel digital input/output pins. When $\overline{CS}$ and $\overline{RD}$ are low, these pins are used to output DB15 to DB9 of the conversion result. When $\overline{PAR}$/SER SEL = 1, these pins should be tied to DGND.
25	D.O.	DB7/$D_{OUT}A$	Parallel output Data Bit 7/ Serial interface data output pin $D_{OUT}A$. When $\overline{PAR}$/SER SEL = 0, this pins acts as a three-state parallel digital input/output pin. When $\overline{CS}$ and $\overline{RD}$ are low, this pin is used to output DB7 of the conversion result. When $\overline{PAR}$/SER SEL = 1, this pin functions as $D_{OUT}A$ and outputs serial conversion data. See DIGITAL Interface for further details.
24	D.O.	DB8/$D_{OUT}B$	Parallel output Data Bit 8/ Serial interface data output pin $D_{OUT}B$. When $\overline{PAR}$/SER SEL = 0, this pins acts as a three-state parallel digital input/output pin. When $\overline{CS}$ and $\overline{RD}$ are low, this pin is used to output DB8 of the conversion result. When $\overline{PAR}$/SER SEL = 1, this pin functions as $D_{OUT}B$ and outputs serial conversion data. See DIGITAL Interface for further details.
22 to 16	D.O.	DB[6: 0]	Parallel output data bits Data Bit 6 to Data Bit 0. When $\overline{PAR}$/SER SEL = 0, these pins act as three-state parallel digital input/output pins. When $\overline{CS}$ and $\overline{RD}$ are low, these pins are used to output DB6 to DB 0 of the conversion result. When $\overline{PAR}$/SER SEL = 1, these pins should be tied to DGND

TERMINOLOGY

Integral Nonlinearity
The maximum deviation from a straight line passing through the endpoints of the ADC transfer function. The endpoints of the transfer function are zero scale, a ½ LSB below the first code transition and full scale at ½ LSB above the last code transition.

Differential Nonlinearity
The difference between the measured and the ideal 1 LSB change between any two adjacent codes in the ADC.

Bipolar Zero Code Error
The deviation of the midscale transition (all 1s to all 0s) from the ideal V_{IN} voltage, that is, AGND − 1 LSB.

Bipolar Zero Code Error Match
The difference in bipolar zero code error between any two input channels.

Positive Full-Scale Error
The deviation of the last code transition (011…110) to (011…111) from the ideal (+4 × V_{REF} − 1 LSB, +2 × V_{REF} − 1 LSB) after adjusting for the bipolar zero code error.

Positive Full-Scale Error Match
The difference in positive full-scale error between any two input channels.

Negative Full-Scale Error
The deviation of the first code transition (10…000) to (10…001) from the ideal (−4 × V_{REF} + 1 LSB, −2 × V_{REF} + 1 LSB) after adjusting for the bipolar zero code error.

Negative Full-Scale Error Match
The difference in negative full-scale error between any two input channels.

Track-and-Hold Acquisition Time
The track-and-hold amplifier returns to track mode at the end of the conversion. The track-and-hold acquisition time is the time required for the output of the track-and-hold amplifier to reach its final value, within ±1 LSB, after the end of the conversion. See the Track-and-Hold for more details.

Signal-to-(Noise + Distortion) Ratio
The measured ratio of signal-to-(noise + distortion) at the output of the ADC. The signal is the rms amplitude of the fundamental. Noise is the sum of all nonfundamental signals up to half the sampling frequency (f_S/2, excluding dc). The ratio depends on the number of quantization levels in the digitization process: the more levels, the smaller the quantization noise. The theoretical signal-to-(noise + distortion) ratio for an ideal N-bit converter with a sine wave input is given by

Signal-to-(*Noise* + *Distortio*n) = (6.02 *N* + 1.76) dB

Thus, for a 16-bit converter, this is 98 dB.

Total Harmonic Distortion (THD)
The ratio of the rms sum of the harmonics to the fundamental. For the AD7606, it is defined as

$$THD(\text{dB}) = 20\log\frac{\sqrt{V_2{}^2 + V_3{}^2 + V_4{}^2 + V_5{}^2 + V_6{}^2}}{V_1}$$

where:

V_1 is the rms amplitude of the fundamental.
V_2, V_3, V_4, V_5, and V_6 are the rms amplitudes of the second through sixth harmonics.

Peak Harmonic or Spurious Noise
The ratio of the rms value of the next largest component in the ADC output spectrum (up to f_S/2, excluding dc) to the rms value of the fundamental. Normally, the value of this specification is determined by the largest harmonic in the spectrum, but for ADCs where the harmonics are buried in the noise floor, it is determined by a noise peak.

Intermodulation Distortion
With inputs consisting of sine waves at two frequencies, fa and fb, any active device with nonlinearities create distortion products at sum and difference frequencies of mfa ± nfb, where m, n = 0, 1, 2, 3. Intermodulation distortion terms are those for which neither m nor n are equal to 0. For example, the second-order terms include (fa + fb) and (fa − fb), and the third-order terms include (2fa + fb), (2fa − fb), (fa + 2fb), and (fa − 2fb).

The AD7606 is tested using the CCIF standard in which two input frequencies near the top end of the input bandwidth are used. In this case, the second-order terms are usually distanced in frequency from the original sine waves, and the third-order terms are usually at a frequency close to the input frequencies. As a result, the second- and third-order terms are specified separately. The calculation of the intermodulation distortion is per the THD specification, where it is the ratio of the rms sum of the individual distortion products to the rms amplitude of the sum of the fundamentals expressed in decibels.

Power Supply Rejection (PSR)
Variations in power supply affect the full-scale transition but not the converter's linearity. Power supply rejection is the maximum change in full-scale transition point due to a change in power supply voltage from the nominal value. The power supply rejection ratio is defined as the ratio of the power in the ADC output at full-scale frequency, f, to the power of a 200 mV p-p sine wave applied to the ADC's V_{DD} and V_{SS} supplies of frequency f_S

PSRR (dB) = 10 log (*Pf*/*Pf*$_S$)

where:

Pf is equal to the power at frequency *f* in the ADC output.
Pf_S is equal to the power at frequency f_S coupled onto the V_{DD} and V_{SS} supplies.

Channel-to-Channel Isolation
Channel-to-channel isolation is a measure of the level of crosstalk between any two channels. It is measured by applying a full-scale, 10 kHz sine wave signal to all unselected input channels and determining the degree to which the signal attenuates in the selected channel with a 1 kHz signal.

THEORY OF OPERATION

CONVERTER DETAILS

The AD7606 is a high speed, low power analog-to-digital converter that allows the simultaneous sampling of eight analog input channels. The analog inputs on the AD7606 can accept true bipolar input signals. The RANGE pin is used to select either ±10V or ±5V as the input range.

The AD7606 contains a high speed SAR ADC, eight signal scaling amplifiers, eight track-and-hold amplifiers, an on-chip 1.2 V reference, reference buffers, over-sampling options and high speed parallel and serial interfaces. The AD7606 has two CONVST pins, CONVST A and CONVST B. By connecting both CONVST pins together, the AD7606 is configured to simultaneously sample all eight input channels. Alternatively, the eight input channels can be grouped into two separate groups of four channels each. Each group has an associated CONVST signal used to initiate simultaneous sampling on each group of four channels. CONVST A is used to initiate simultaneous sampling on V1, V2, V3 and V4 and CONVST B is used to initiate simultaneous sampling on V5, V6, V7 and V8.

The conversion process is initiated on the AD7606 by pulsing the CONVST A and CONVST B inputs. On the rising edge of CONVST A, the track-and-hold amplifiers for channels V1 to V4 are placed into hold mode. On the rising edge of CONVST B, the track-and-hold amplifiers for channels V5 to V8 are placed into hold mode. The conversion process begins once both rising edges of CONVST have occurred, so BUSY will go high on the rising edge of the later CONVST signal. If both CONVST A and CONVST B are tied together then the conversion process will start on the rising edge of the signal applied to both pins and BUSY will go high at this time to indicate the conversion process is taking place. It should be noted that when oversampling is switched on then CONVST A and CONVST B must be controlled simultaneously.
The conversion clock for the part is internally generated, and the conversion time for all eight channels on the AD7606 is 4 µs. The BUSY signal returns low after all eight conversions to indicate the end of the conversion process. On the falling edge of BUSY, the track-and-hold amplifiers return to track mode. New data can be read from the output register via the parallel or serial interface after BUSY goes low or alternatively data from the previous conversion may be read while BUSY is high. Reading data from the AD7606 while a conversion is in progress will have no effect on performance and will allow a faster throughput to be achieved. See the DIGITAL Interface section for more details.

Track-and-Hold Amplifiers

The track-and-hold amplifiers on the AD7606 allow the ADC to accurately acquire an input sine wave of full-scale amplitude to 16-bit resolution. The analog input impedance of each channel on the AD7606 is approximately 1MΩ as shown in Figure 3. The bandwidth of the analog input channels is dominated by that of the front end signal scaling amplifiers which is in the range of 5 to 10kHz.

The track-and-hold amplifiers sample their respective inputs simultaneously on the rising edge of CONVST. The aperture time for the track-and-hold (that is, the delay time between the external CONVST signal and the track-and-hold actually going into hold) is TBD ns. This figure is well matched across all eight track-and-holds on one device and from device to device. This allows more than one AD7606 device to be sampled simultaneously in a system. The end of the conversion process across all eight channels is indicated by the falling edge of BUSY, and it is at this point that the track-and-holds return to track mode and the acquisition time for the next set of conversions begins.

Analog Input

The AD7606 can handle true bipolar input voltages. The logic level on the RANGE pin determines the analog input range of the analog input channels. If this pin is tied to a logic high, the analog input range is ±10V for all channels, V1 to V8. If this pin is tied to a logic low, the analog input range is ±5V for all channels, V1 to V8. A logic change on this pin will have an immediate effect on the analog input range. Recommended practice is to hardwire the range pin according to the desired input range for the system signals. Changing the setting on this pin would result in a settling time in the order of TBD typically in addition to the normal acquisition time requirement.

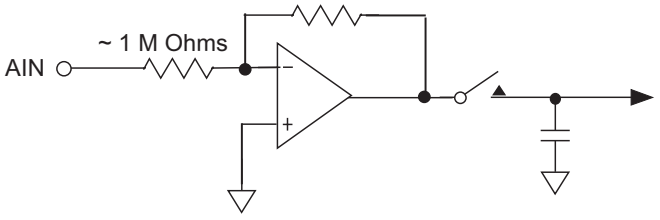

Figure 3 Analog Input circuitry

ADC TRANSFER FUNCTION

The output coding of the AD7606 is twos complement. The designed code transitions occur midway between successive integer LSB values, that is, 1/2 LSB, 3/2 LSB. The LSB size is FSR/65,536 for the AD7606. The ideal transfer characteristic for the AD7606 is shown in Figure 4.

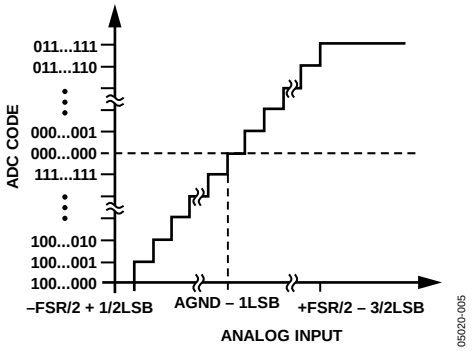

Figure 4. AD7606 Transfer Characteristic

The LSB size is dependent on the analog input range selected (see Table 6).

Table 6. LSB Size for Each Analog Input Range

	AD7606 Range	
Input Range	±10 V	±5 V
LSB Size	0.305 mV	0.152 mV
FS Range	20 V/65,536	10 V/65,536

INTERNAL/EXTERNAL REFERENCE

The REFIN/REFOUT pin allows access to a 1.2V reference which generates the on-chip 4.5 V reference internally, or it allows an external reference of 1.2V to be applied to the AD7606 . An externally applied reference of 1.2V is also gained up to 4.5V internally. The REF SELECT pin is a logic input pin which allows the user to select between the internal reference or and external reference . If this pin is set to logic high then the internal reference is selected and is enabled, if this pin is set to logic low then the internal reference is disabled and an external reference voltage must be applied to the REFIN/REFOUT pin. The reference buffer is always enabled.

After a RESET, the AD7606 operates in the reference mode selected by the REF SELECT pin. Decoupling is required on the REFIN/REFOUT pin for both the internal or external reference options. A 10uF capacitor should be applied from this pin to ground close to the REFGND pins.

The AD7606 contains a 1.2V band-gap reference and a reference buffer configured to gain this up to ~4.5V as shown in Figure 5. The REFCAPA and REFCAPB pins must be shorted together externally and a capacitor of 10µF applied to AGND to ensure the reference buffer is in closed loop operation.

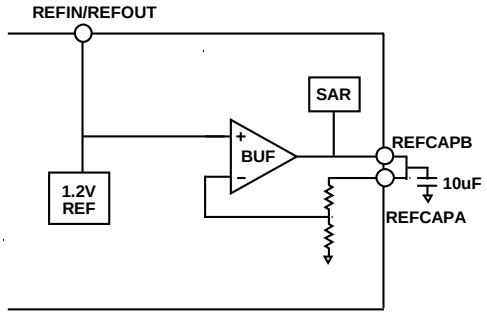

Figure 5 Reference Circuitry

DRIVING THE ANALOG INPUTS

An external driver amplifier/buffer is not required to drive the front end of the AD7606. The analog input impedance of each channel is 1MΩ allowing direct connection to the signal source in many cases. This eliminates the need for an external buffer and therefore removes bipolar supplies from the signal chain, which are often a source of noise.

TYPICAL CONNECTION DIAGRAM

Figure 6 shows the typical connection diagram for the AD7606. There are three AV_{CC} supply pins on the part which can be tied together and decoupled using a 100nF cap at each supply pin and a 10 µF capacitor at the supply source. The AD7606 can operate with the internal reference or an externally applied reference. In this configuration, the parts are configured to operate with the internal reference. The REFIN/REFOUT pin is decoupled with a 1 µF capacitor. The REFCAPA and REFCAPB pins are shorted together and decoupled with a 10 µF capacitor. AGND pins are connected to the AGND plane of the system. The DGND pins are connected to the digital ground plane in the system. The AGND and DGND planes should be connected together at one place in the system. This connection should be as close as possible to the AD7606 in the system.

The V_{DRIVE} supply is connected to the same supply as the processor. The voltage on V_{DRIVE} controls the voltage value of the output logic signals. If V_{DRIVE} is at the same potential as DV_{DD} then the one source and decoupling capacitor may be shared.

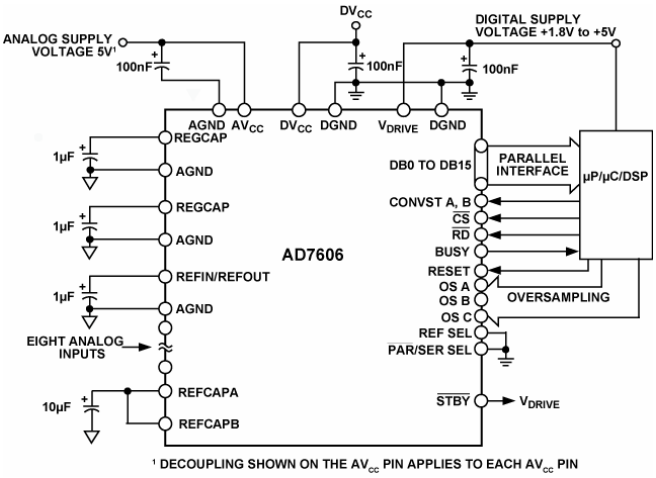

Figure 6 Typical Connection Diagram

DIGITAL INTERFACE

The AD7606 provides two interface options, a parallel interface and a high-speed serial interface. The required interface mode is selected via the PAR/SER SEL pin. The operation of the interface modes is discussed in the following sections.

PARALLEL INTERFACE (PAR/SER SEL= 0)

Sampling 8-channels simultaneously

The AD7606 allows simultaneous sampling of eight analog input channels. All eight channels are sampled simultaneously when both CONVST pins (CONVST A, CONVST B) are tied together. A single CONVST signal is used to control both inputs. The rising edge of this common CONVST signal initiates simultaneous sampling on all eight channels (V1 to V8).

The AD7606 contains an on-chip oscillator that is used to perform the conversions. The conversion time for all eight ADC channels, t_{CONV}, is 4 µs. The BUSY signal indicates to the user when conversions are in progress, so when the rising edge of CONVST is applied, BUSY goes logic high, and transitions low at the end of the entire conversion process. The falling edge of the BUSY signal is used to place all eight track-and-hold amplifiers back into track mode. The falling edge of BUSY also indicates that the new data may now be read from the parallel bus DB[15:0].

Data can be read from the AD7606 via the parallel data bus with standard $\overline{CS}$ and $\overline{RD}$ signals. To read the data over the parallel bus, the PAR/SER SEL pin should be tied low. The $\overline{CS}$ and $\overline{RD}$ input signals are internally gated to enable the conversion result onto the data bus. The data lines DB0 to DB15 leave their high impedance state when both $\overline{CS}$ and $\overline{RD}$ are logic low.

The rising edge of the $\overline{CS}$ input signal tri-states the bus and the falling edge of the $\overline{CS}$ input signal takes the bus out of the high impedance state . $\overline{CS}$ is the control signal that enables the data lines, it is the function that allows multiple AD7606 devices to share the same parallel data bus.

The $\overline{CS}$ signal can be permanently tied low, and the $\overline{RD}$ signal can be used to access the conversion results as shown in Figure 9. A read operation of new data can take place after the BUSY signal goes low, or alternatively a read operation of data from the previous conversion process can take place while BUSY is high.

The $\overline{RD}$ pin is used to read data from the output conversion results register. Applying a sequence of $\overline{RD}$ pulses to the AD7606 $\overline{RD}$ pin clocks the conversion results out from each channel onto the parallel output bus DB[15:0] in ascending order. The first $\overline{RD}$ falling edge after BUSY goes low clocks out the conversion result from channel V1, the next $\overline{RD}$ falling edge updates the bus with the V2 conversion result and so on. The 8th falling edge of $\overline{RD}$ clocks out the conversion result for channel V8. When the $\overline{RD}$ signal is logic low, it enables the data conversion result from each channel to be transferred to the digital host (DSP, FPGA).

When there is only one AD7606 in a system/board and it does not share the parallel bus, data can be read using just one control signal from the digital host. The $\overline{CS}$ and $\overline{RD}$. signals can be tied together as shown in Figure 7 and Figure 8. In this case the data bus comes out of tri-state on the falling edge of $\overline{CS}$/$\overline{RD}$. The combined $\overline{CS}$ and $\overline{RD}$ signal allows the data to be clocked out of the AD7606 and to be read by the digital host. In this case $\overline{CS}$ is used to frame the data transfer of each data channel.

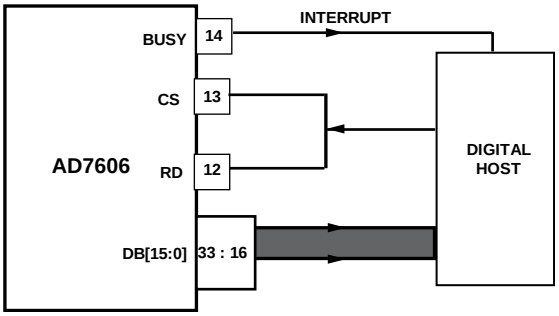

Figure 7 AD7606 interface diagram: One AD7606 using the parallel bus; $\overline{CS}$ and $\overline{RD}$ shorted together.

Simultaneously sampling two sets of 4 channels

The AD7606 also allows for the analog input channels to be sampled simultaneously in two groups of four. This is accomplished by pulsing the two CONVST pins independently and is only possible if oversampling is not in use. CONVST A is used to initiate simultaneous sampling on V1 to V4, CONVST B is used to initiate simultaneous sampling on V5 to V8 as illustrated in Figure 10.

On the rising edge of CONVST A, the track-and-hold amplifiers for channels V1 to V4 are placed into hold mode. On the rising edge of CONVST B, the track-and-hold amplifiers for channels V5 to V8 are placed into hold mode. The conversion process begins once both rising edges of CONVST have occurred, so BUSY will go high on the rising edge of the later CONVST signal. If both CONVST A and CONVST B are tied together then the conversion process will start on the rising edge of the signal applied to both pins and BUSY will go high at this time to indicate the conversion process is taking place. The conversion results are stored in the output data registers and a read of this new data can take place once BUSY has returned low.

There is no change to the data read process when using two separate CONVST signals.

Connect all unused analog input channel to AGND. The results for any unused channels will still be included in the data read as all eight channels are always converted.

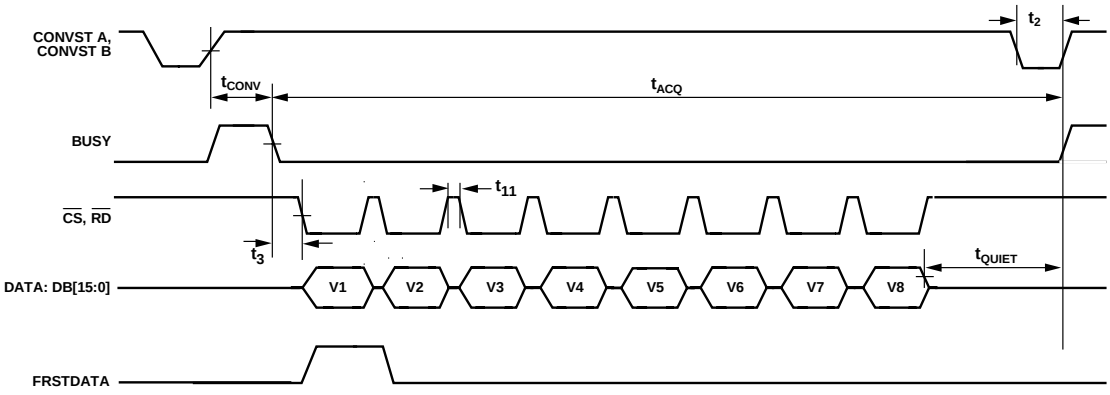

Figure 8. Parallel Interface: $\overline{CS}$ and $\overline{RD}$ tied together; (Sampling all 8-channel simultaneously) . No over sampling.

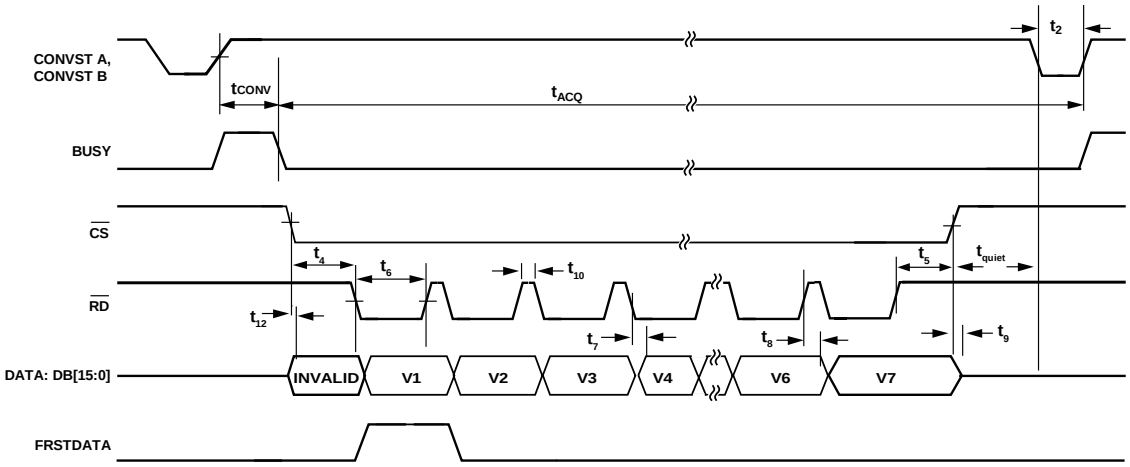

Figure 9. Parallel Interface Separate: $\overline{CS}$ and $\overline{RD}$ signals; (Sampling all 8 channels simultaneously) .No over sampling.

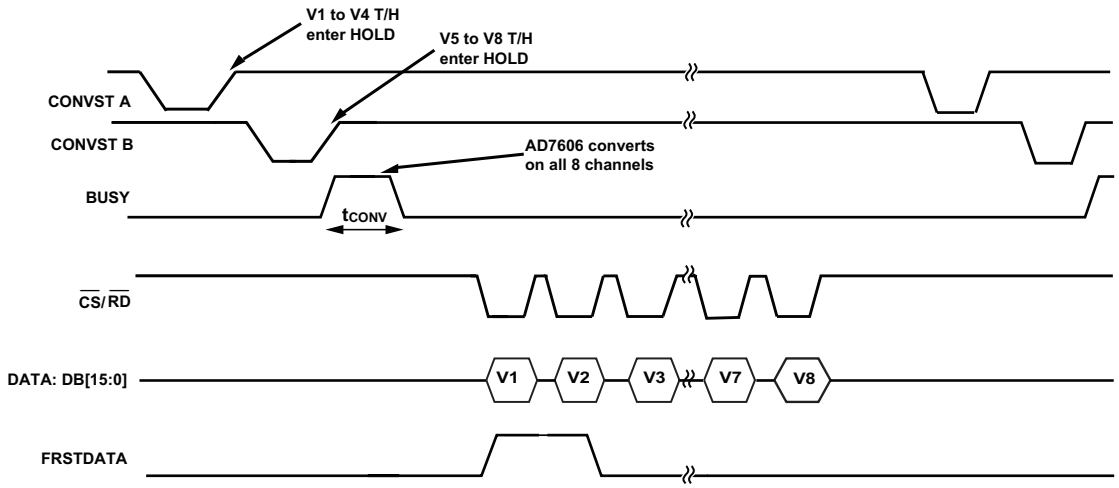

Figure 10. Parallel Interface Mode – Staggered CONVST (separate simultaneous sample instances for V1 to V4 and V5 toV8) No oversampling.

Serial Interface ($\overline{PAR}$/SER SEL= 1)

The AD7606 allows simultaneous sampling of eight analog input channels. All eight channels are sampled simultaneously when both CONVST pins (CONVST A, CONVST B) are tied together. A single CONVST signal is used to control both inputs. The rising edge of this common CONVST signal initiates simultaneous sampling on all eight channels (V1 to V8).

The AD7606 contains an on-chip oscillator that is used to perform the conversions. The conversion time for all eight ADC channels, t_{CONV}, is 4 µs. The BUSY signal indicates to the user when conversions are in progress, so when the rising edge of CONVST is applied, BUSY goes logic high, and transitions low at the end of the entire conversion process. The falling edge of the BUSY signal is used to place all eight track-and-hold amplifiers back into track mode. The falling edge of BUSY also indicates that the new data may now be read via the serial interface.

To read data back from the AD7606 over the serial interface, the $\overline{PAR}$/SER SEL pin should be tied high. The $\overline{CS}$ and SCLK signals are used to transfer data from the AD7606. The AD7606 has two serial data output pins, $D_{OUT}A$, and $D_{OUT}B$. Data can be read back from the AD7606 using one or both of these DOUT lines. Conversion results from channels V1 to V4 first appear on $D_{OUT}A$ while conversion results from channels V5 to V8 first appear on $D_{OUT}B$. The $\overline{CS}$ falling edge takes the data output lines $D_{OUT}A$ and $D_{OUT}B$ out of tri-state and clocks out the MSB of the conversion result. The rising edge of SCLK clocks all subsequent data bits onto the serial data outputs $D_{OUT}A$ and $D_{OUT}B$. The $\overline{CS}$ input can be held low for the entire serial read or it can be pulsed to frame each channel read of 16 SCLK cycles.

Figure 11 shows a read of eight simultaneous conversion results using two DOUT lines. In this case, 64 SCLK transfers are used to access data from the AD7606 and $\overline{CS}$ is held low to frame the entire 64 SCLK cycles.

Data can also be clocked out using just one DOUT line, in which case $D_{OUT}A$ is recommended to access all conversion data as the channel data will be output in ascending order from channel V1 to V8. To access all eight conversion results on one DOUT line a total of 128 SCLK cycles are required. These 128 SCLK cycles can be framed by one $\overline{CS}$ signal or each group of 16 SCLK cycles can be individually framed by the $\overline{CS}$ signal. The disadvantage of using just one DOUT line is that the throughput rate is reduced. The unused DOUT line should be left unconnected in serial mode. If $D_{OUT}B$ is to be used as a single DOUT line then the channel results will be output in the order V5, V6, V7, V8, V1, V2, V3, V4.

Figure 12 shows the timing diagram for reading one channel of data, framed by the $\overline{CS}$ signal, from the AD7606 in serial mode. The SCLK input signal provides the clock source for the serial read operation. The $\overline{CS}$ goes low to access the data from the AD7606. The falling edge of $\overline{CS}$ takes the bus out of three-state and clocks out the MSB of the 16-bit conversion result. This MSB is valid on the first falling edge of the SCLK after the $\overline{CS}$ falling edge. The subsequent 15 data bits are clocked out of the AD7606 on the SCLK rising edge. Data is valid on the SCLK falling edge. Sixteen clock cycles must be provided to the AD7606 to access each conversion result.

The FRSTDATA output signal indicates when the first channel, V1, is being read back. When the $\overline{CS}$ input is high the FRSTDATA output pin is in three-state. In serial mode, the falling edge of $\overline{CS}$ takes FRSTDATA out of three-state and sets the FRSTDATA pin high indicating that the result from V1 is available on the $D_{OUT}A$ output data line. The FRSTDATA output returns to a logic low following the sixteenth SCLK falling edge. If all eight channels are read on $D_{OUT}B$ then the FRSTDATA output will not go high when V1 is being output on this serial data output pin. It only goes high when V1 is available on $D_{OUT}A$ (and this is when V5 is available on $D_{OUT}B$).

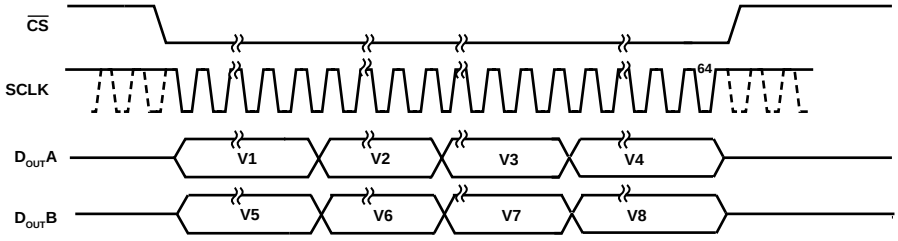

Figure 11. Serial Interface with two DOUT Lines

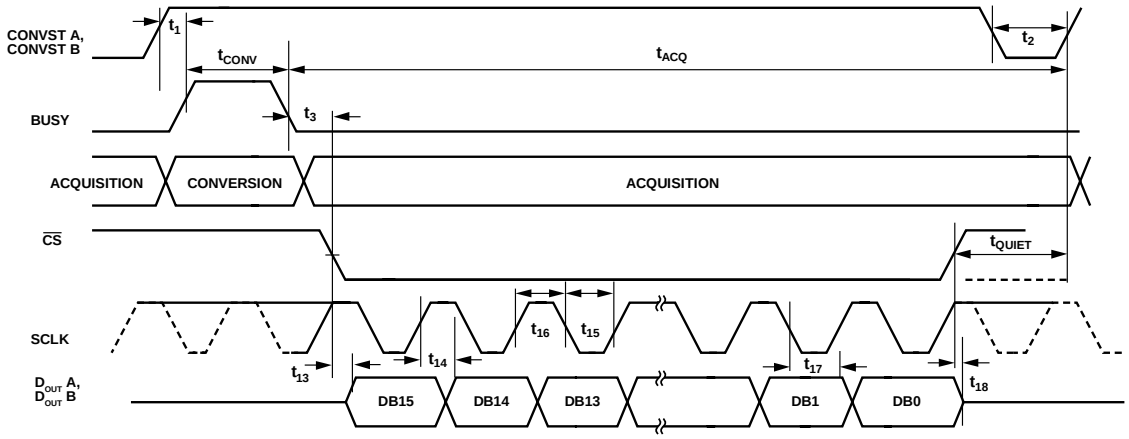

Figure 12 Serial Read Operation

READING DURING CONVERSION

Data may be read from the AD7606 while BUSY is high and conversions are in progress. This will not affect the performance of the converter and allows a faster throughput rate to be achieved. A parallel or serial read may be performed during conversion and oversampling may be in use or off. Figure 13 shows the timing diagram for reading while BUSY is high in parallel or serial mode. Reading during conversion allows for the full throughput rate to be achieved when using the serial interface.

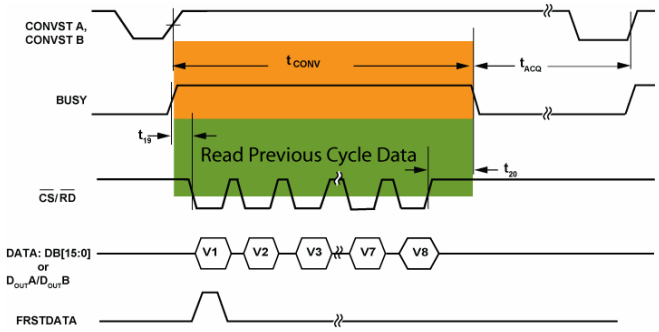

Figure 13 Read During Conversion

OVER SAMPLING MODE

The AD7606 converts all eight channels simultaneously at a rate of 200ksps per channel. However, the AD7606 features an over-sampling mode, which can be taken advantage of in applications where slower throughput rates are used and where higher signal to noise ratio or dynamic range is desirable. In addition to the over-sampling function the output result is decimated to 16-bit resolution. There are three over-sampling mode pins on the AD7606, OS 2, OS 1 and OS 0. These logic inputs are used to select the over-sampling rate. OS 2 is the MSB control bit while OS 0 is the LSB control bit. Table 7 provides the over-sampling bit decoding to set the required over-sample rate.

Table 7 Over-sample Bit Decoding

OS 2	OS 1	OS 0	Over-sample Rate
0	0	0	1
0	0	1	2
0	1	0	4
0	1	1	8
1	0	0	16
1	0	1	32
1	1	0	64
1	1	1	Not allowed

To set the over-sample rate, the logic values on the pins OS 2, OS 1 and OS 0 must be set as required and are then latched on the falling edge of the BUSY output for the next conversion. The next and all subsequent conversion cycles should be executed as usual allowing adequate acquisition time and a rising edge on the CONVST pins at the sampling instant. The CONVST A and CONVST B pins must be tied/ driven together when over-sampling is turned on. When the over-sampling function is turned on, then the BUSY high time for the conversion process will be seen to extend. The actual BUSY high time will depend on the over-sampling rate selected; the higher the over-sampling rate, the longer the BUSY high, or conversion, time. As a result, the achievable throughput rate per channel is reduced but the benefit is an improvement of ~3dB in SNR for each over-sampling increment. Figure 14, Figure 15 and Figure 16 show an example with a throughput rate of 10ksps, or a cycle time of 100 µs, with no over-sampling in Figure 14, an over-sampling rate of 4 in Figure 15 and an over-sampling rate of 8 in Figure 16. The conversion time can be seen to extend as the over-sampling rate is increased, leaving less time available to read within the cycle time. In this example, there is adequate cycle time to continue to increase the over-sampling rate further. In a case where the initial sampling or throughput rate is at 200ksps for example, then if over-sampling is turned on, then the throughput rate will have to be reduced to accommodate the longer conversion time and to allow for the read. The read may be performed during the BUSY high time in order to achieve the fastest throughput rate possible when over-sampling is tuned on, or even if over-sampling is not in use. Figure 17 illustrates the effect of over-sampling on the code spread in a DC histogram plot. As the over-sample rate is increased, the spread of codes is reduced. The BUSY high time when over-sampling is off is simply 1 × conversion time and total cycle time required is t_{ACQ} + conversion time. When over-sampling is turned on then the BUSY high time is (N × conversion time) + (N-1 × t_{ACQ}) where N = over-sampling rate. The total cycle time required is now t_{ACQ} + BUSY high time.

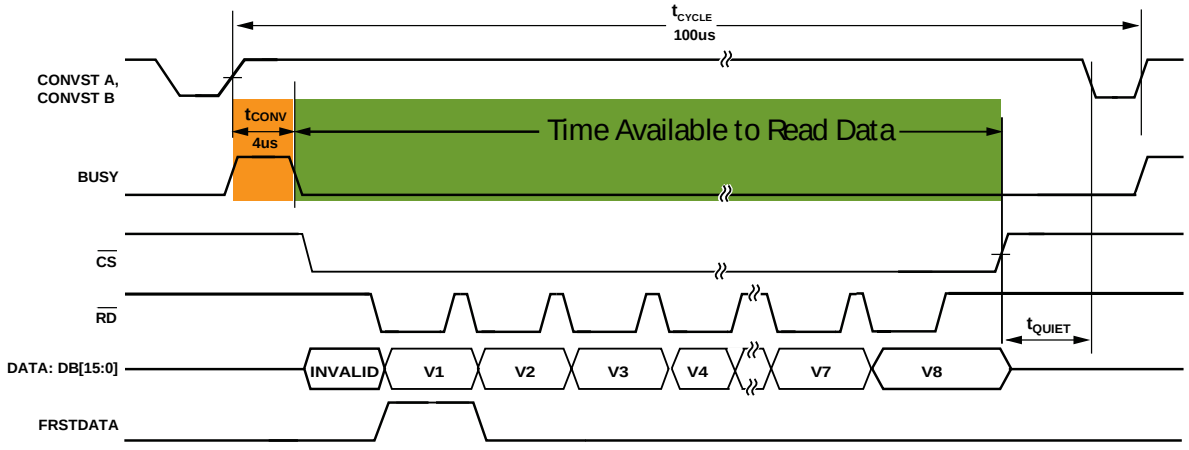

Figure 14 Over-sampling Off, 10kSPS Example

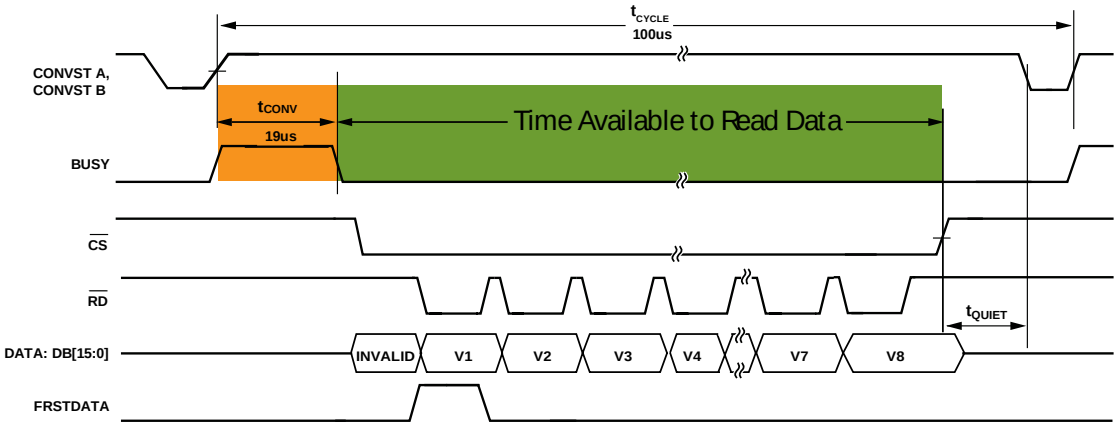

Figure 15 Over-sampling ON Rate =4, 10kSPS Example

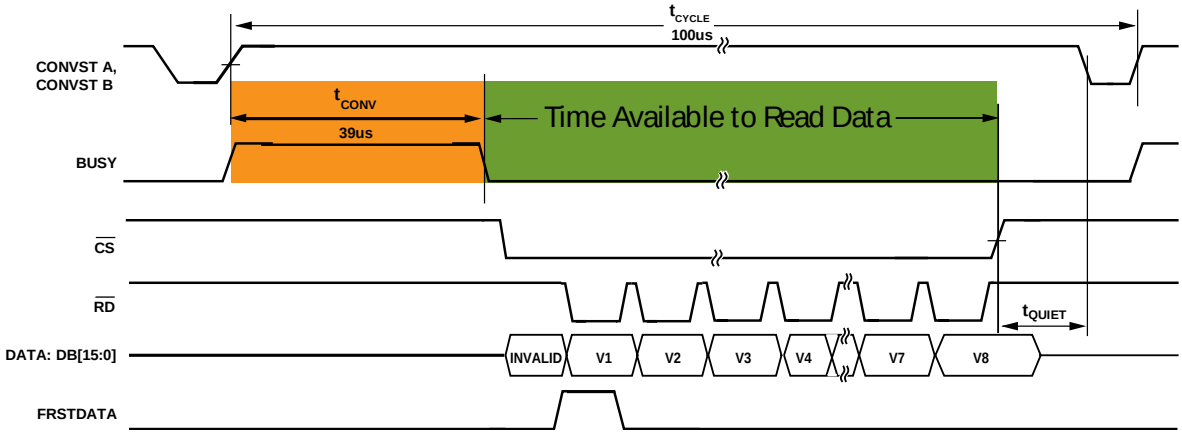

Figure 16 Over-sampling ON Rate = 8, 10kSPS Example

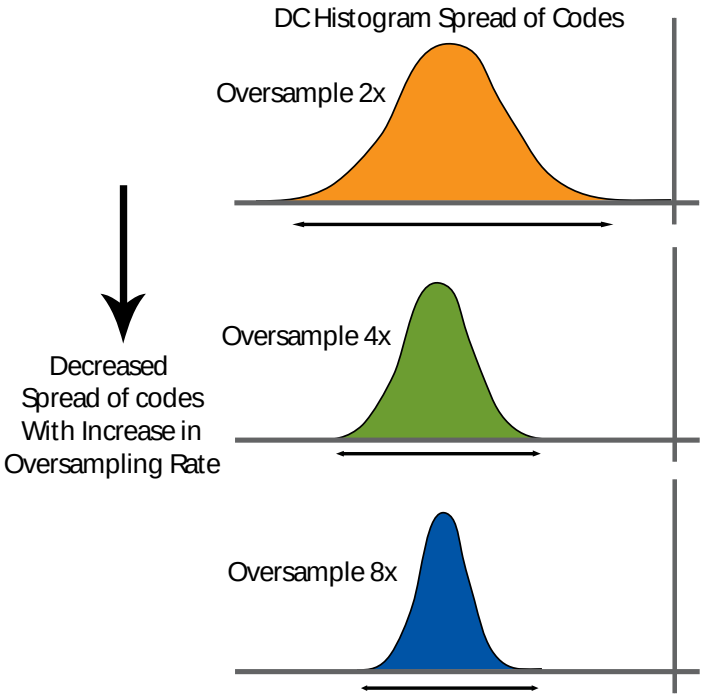

Figure 17 Effect of Over-sampling rate on DC Histogram of Codes

AD7606 LAYOUT GUIDELINES

The printed circuit board that houses the AD7606 should be designed so that the analog and digital sections are separated and confined to different areas of the board.

At least one ground plane should be used. It can be common or split between the digital and analog sections. In the case of the split plane, the digital and analog ground planes should be joined in only one place, preferably underneath the AD7606, or at least as close as possible to the part.

If the AD7606 is in a system where multiple devices require analog-to-digital ground connections, the connection should still be made at only one point, a star ground point, which should be established as close as possible to the AD7606. Good connections should be made to the ground plane. Avoid sharing one connection for multiple ground pins. Individual vias or multiple vias to the ground plane should be used for each ground pin.

Avoid running digital lines under the devices because doing so couples noise onto the die. The analog ground plane should be allowed to run under the AD7606 to avoid noise coupling. Fast-switching signals like CONVST or clocks should be shielded with digital ground to avoid radiating noise to other sections of the board, and they should never run near analog signal paths. Crossover of digital and analog signals should be avoided. Traces on layers in close proximity on the board should run at right angles to each other to reduce the effect of feedthrough through the board.

The power supply lines to the AV_{CC}, DV_{CC}, and V_{DRIVE}, pins on the AD7606 should use as large a trace as possible to provide low impedance paths and reduce the effect of glitches on the power supply lines. Good connections should be made between the AD7606 supply pins and the power tracks on the board; this should involve the use of a single via or multiple vias for each supply pin.

Good decoupling is also important to lower the supply impedance presented to the AD7606 and to reduce the magnitude of the supply spikes. The decoupling capacitors should be placed close to, ideally right up against, these pins and their corresponding ground pins.

OUTLINE DIMENSIONS

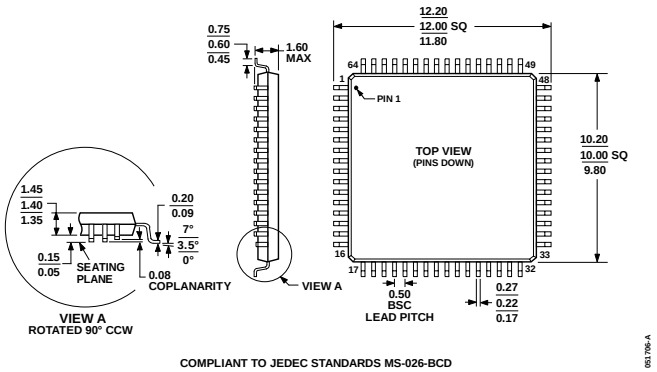

Figure 18 64-Lead Low Profile Quad Flat Package [LQFP]

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD7606BSTZ[1]	−40°C to +85°C	64-Lead Low Profile Quad Flat Package [LQFP]	ST-64-2

[1] Z = RoHS Compliant Part.

NOTES

PR08095-0-2/09(PrG)