BT2402

DEVICE

48 Gb/s Bit Error Rate Tester, Dual 24 Gb/s CH

OVERVIEW

The Optilab BT2402 is a Dual 24 Gb/s Bit Error Rate Tester (BERT) combined, for 48 Gb/s. This high performance BT2402 provides an easy solution for bit error rate testing of (D) QPSK system with data rate up to 48 Gb/s. The Optilab BT2402 consists PG2402 Pattern Generator and EA2402 Error Analyzer. The user selectable reference clock allows testing BER at a specific data rate with external clock input or at a pre- defined data rate using the internal clock. A high speed synchronized clock at half or full data rate is available for eye pattern monitoring or RZ pulse generation. An intuitive GUI, Optilab Teraport, is provided with the BERT system for easy operation. Contact Optilab for more information.

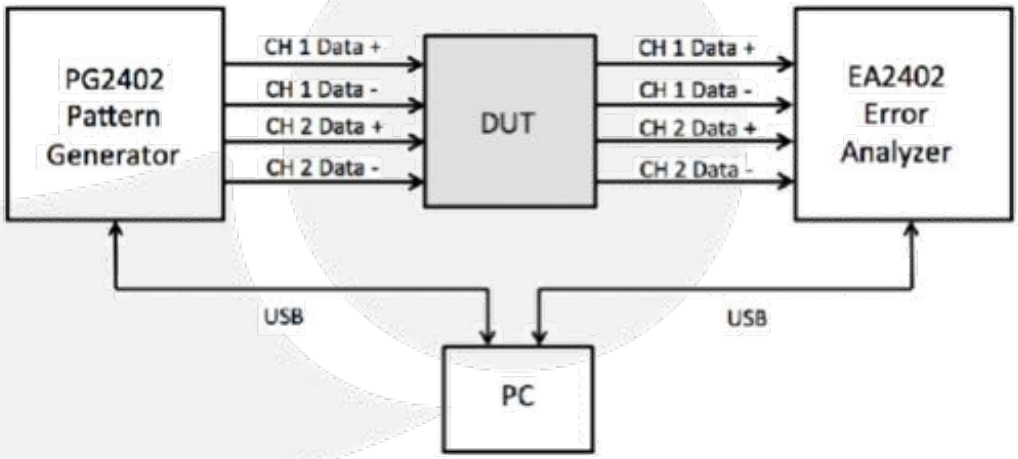
FEATURES

- Data Rate from 2 x 20 to 2 x 24 Gbps
- PRBS of 2^7-1 or 2^{31}-1
- Integrated DQPSK Precoder
- Error injection function
- Teraport GUI software included
- Differential output adjustable to 1 volt
- Eye Crossing Adjustment

USE IN

- Photonics module testing
- 43 Gbps DQPSK Link
- Electrical eye diagram to 24 Gb/s x 2
- 100 Gbps DP-QPSK testing

FUNCTIONAL DIAGRAM



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SPECIFICATIONS

PG2402 DATA OUTPUT

Data Pattern	128 bit Flexed Pattern or PRBS (2^7-1 or 2^{31}-1)
Data Output Type	DC Coupled, Differential
Output Data Rate	20 Gb/s min., 24 Gb/s max.
Output Data Amplitude	0.1 Vpp min., 1 Vpp max.
Differential Output Impedance	100 Ω typ
Data Output RMS Jitter	1.9 ps typ.
Rise/Falls Time (20% to 80%)	20 ps typ.
Electrical Connectors	2.92 mm Female (K or SMA compa.)

PG2402 CLOCK INPUT

Ref Clock Input Frequency	622.5 MHz min, 750 MHz max
Ref Clock Input Amplitude	-5 dBm min, 0 dBm typ, 3 dBm max
HS Clock Output Frequency	10 GHz (half), 12 GHz (full) min.; 20 GHz (half), 24 GHz (full) max.
HS Clock Phase Adjustment Range	0.9 UI min., 1.0 UI typ.
Clock Connectors	SMA Female

EA2402 DATA INPUT

Data Pattern	128 bit Flexed Pattern or PRBS (2^7-1 or 2^{31}-1)
Data Input Type	DC Coupled, Differential
Input Data Rate	20 Gb/s min., 24 Gb/s max.
Input Data Amplitude	0.1 Vpp min., 0.8 Vpp max.
Differential Input Impedance	100 Ω typ
Lock Mode	Lock to ref clock or lock to data
Electrical Connectors	2.92 mm Female (K or SMA compa.)

EA2402 CLOCK INPUT

Ref Clock Input Frequency	622.5 MHz min., 750 MHz max.
Ref Clock Input Amplitude	-5 dBm min., 0 dBm typ., 3 dBm max.
Recovered Clock Frequency	622.5 MHz min., 750 MHz max.
Clock Connectors	SMA Female

MECHANICAL

Operating Temperature	0 °C to +50 °C
Storage Temperature	-40 °C to +70 °C
Operating Humidity	85%
Power Supply Requirements	100 – 240 VAC
Dimensions	Two 1U Rackmount Units, each is 482.6 x 476.6 x 44.5 (mm)
Control Interface	USB

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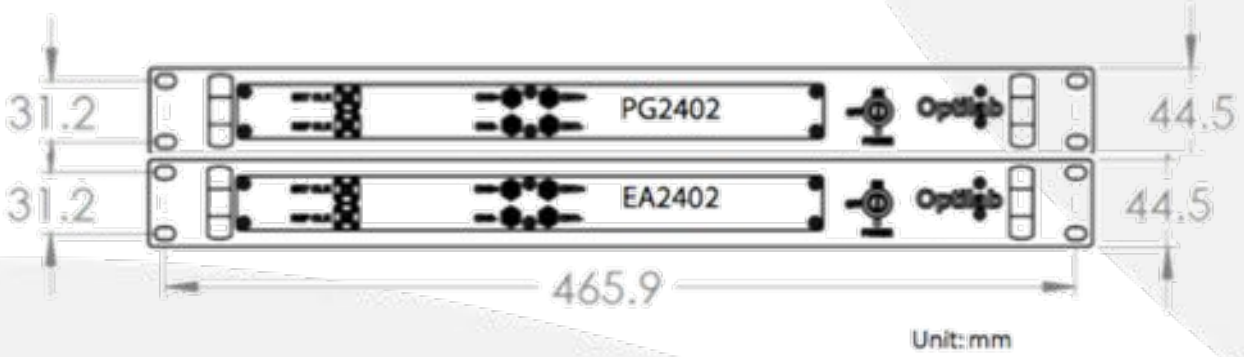
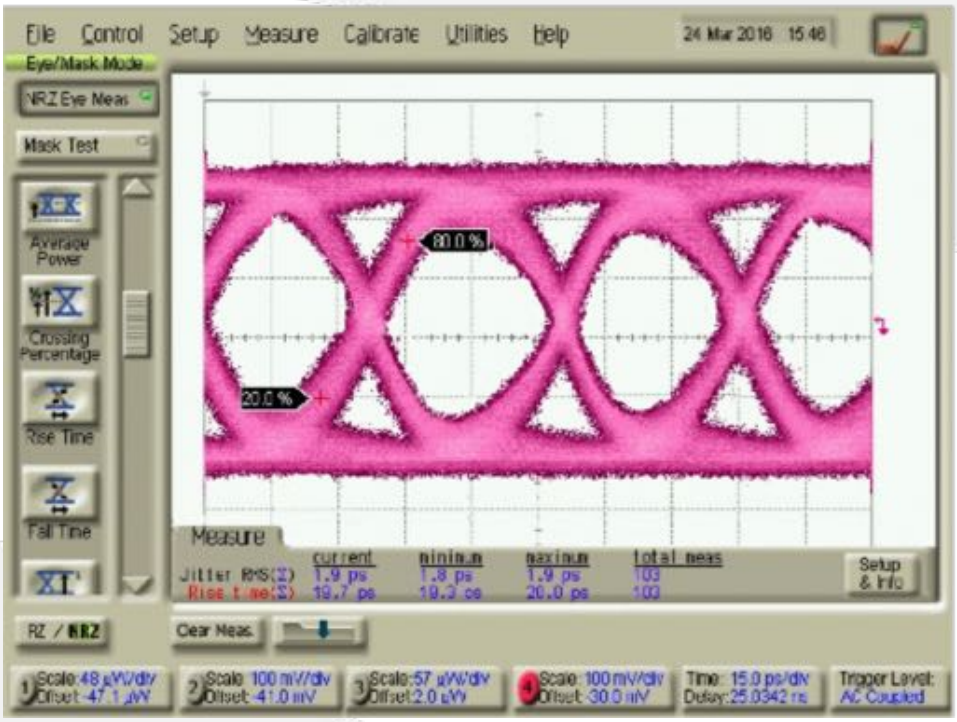
MECHANICAL DRAWING



EYE DIAGRAM



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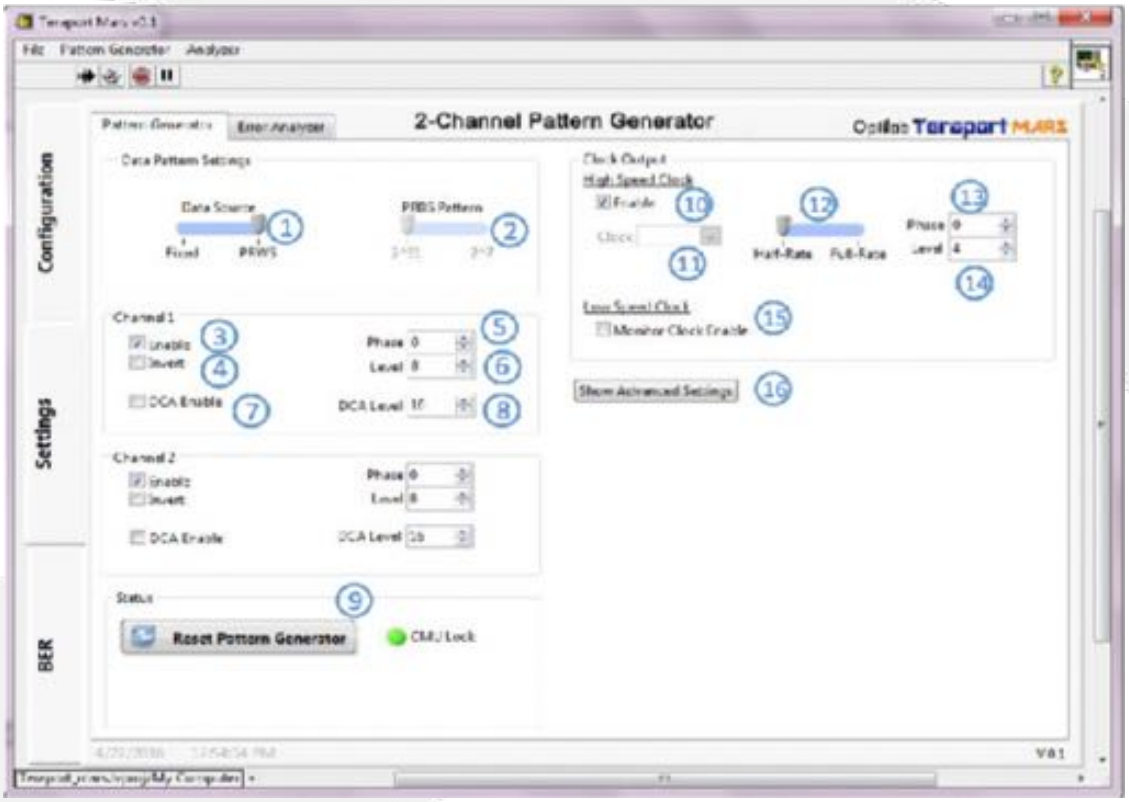
TERAPORT INTERFACE

No.	Function	Description
☑	Data Source	Fixed or PRBS pattern
☑	PRBS Pattern	2^7-1 or 2^31-1
☑	Enable	Enable channel
☑	Invert	Invert data pattern
☑	Phase	Phase adjust
☑	Level	Output voltage level
☑	DCA Enable	Turn on data crossing adjustment
☑	DCA Level	Data crossing adjustment level
☑	Reset Pattern Generator	Reset operation
☑	Enable	Turn on high speed clock output
☑	Clock	Select clock
☑	Half Rate, Full Rate	Select half or full rate
☑	Phase	Phase adjustment
☑	Level	Clock output level adjustment
☑	Monitor Clock Enable	Turn on low speed clock
☑	Show Advanced Setting	Additional control function



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TERAPORT INTERFACE

No.	Function	Description
1	Auto Lock	Automatically lock input
2	DQPSK Decoder Enable	For DQPSK only
3	CKSRC Enable	Enable recovered clock
4	CDR Lock Error	CDR lock error indicator
5	Peak Detector	Input peak detector output
6	RXS	Receiver status indicator
7	LOS	Loss of signal indicator
8	Show Advanced Settings	Menu of advanced setting
9	Reset Error Analyzer	Reset analyzer
10	Show Advanced Reset Setttings	Reset advanced setting
11	Delay Calibration Start	Calibration phase delay