

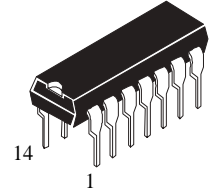
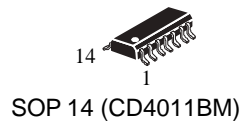


Description

The CD4011 NAND gates provide the system designer with direct implementation of the NAND function.

Features

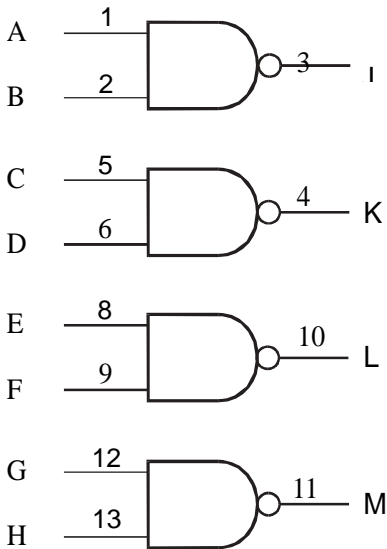
- Operating Voltage Range: 3.0 to 18 V
- Maximum input current of 1 at 18 V over full package-temperature range 100 nA at 18 V and 25 °C
- Noise margin (over full package temperature range):
 - 1.0 V min @ 5.0 V supply
 - 2.0 V min @ 10.0 V supply
 - 2.5 V min @ 15.0 V supply



DIP 14(CD4011BE)

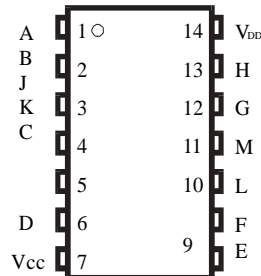
Package

Logic Diagram



PIN 14 = V_{DD}
PIN 7 = V_{CC}

Pin Assignment



Function Table

Inputs		Output
C	D	$J = A \cdot B$
E	F	$K = C \cdot D$
G	H	$L = E \cdot F$
H	H	$M = \overline{G \cdot H}$
H	L	L
L	H	H
L	L	H

Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to +20	V
V_{IN}	DC Input Voltage (Referenced to GND)	-0.5 to $V_{CC} + 0.5$	V
I_{IN}	DC Input Current, per Pin	± 10	mA
P_D	Power Dissipation in Still Air, Plastic DIP+	750 500	mW
P_D	Power Dissipation per Output Transistor	100	mW
Tstg	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package)	260	°C

Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

+Derating - Plastic DIP: - 10 mW/ °C from 65° to 125°C

SOIC Package: - 7 mW/ °C from 65° to 125°C

Recommended Operating Conditions

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	3.0	18	V
V_{IN}, V_{OUT}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V_{CC}	V
T_A	Operating Temperature, All Package Types	-55	+125	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{IN} and V_{OUT} should be constrained to the range $GND \leq (V_{IN} \text{ or } V_{OUT}) \leq V_{CC}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

DC Electrical Characteristics

(Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V _{CC} V	Guaranteed Limit			Unit
				≥-55°C	25°C	≤125 °C	
V _{IH}	Minimum High-Level Input Voltage	V _{OUT} =0.5 V or V _{CC} - 0.5 V V _{OUT} =1.0 V or V _{CC} - 1.0 V V _{OUT} =1.5 V or V _{CC} - 1.5 V V _{OUT} = V _{CC} - 0.5V	5.0	3.5	3.5	3.5	V
			10	7	7	7	
			15	11	11	11	
V _{IL}	Maximum Low -Level Input Voltage	V _{OUT} = V _{CC} - 1.0 V V _{OUT} = V _{CC} - 1.5V	5.0	1.5	1.5	1.5	V
			10	3	3	3	
			15	4	4	4	
V _{OH}	Minimum High-Level Output Voltage	V _{IN} =GND or V _{CC}	5.0	4.95	4.95	4.95	V
			10	9.95	9.95	9.95	
			15	14.95	14.95	14.95	
V _{OL}	Maximum Low-Level Output Voltage	V _{IN} = V _{CC}	5.0	0.05	0.05	0.05	V
			10	0.05	0.05	0.05	
			15	0.05	0.05	0.05	
I _{IN}	Maximum Input Leakage Current	V _{IN} = GND or V _{CC}	18	±0.1	±0.1	±1.0	μA
I _{CC}	Maximum Quiescent Supply Current	V _{IN} = GND or V _{CC}	5.0	0.25	0.25	7.5	μA
			10	0.5	0.5	15	
			15	1.0	1.0	30	
			20	5.0	5.0	150	
I _{OL}	Minimum Output Low (Sink) Current	V _{IN} = GND or V _{CC} U _{OL} =0.4 V U _{OL} =0.5 V U _{OL} =1.5 V V _{IN} = GND or V _{CC}	5.0	0.64	0.51	0.36	mA
			10	1.6	1.3	0.9	
			15	4.2	3.4	2.4	
I _{OH}	Minimum Output High (Source) Current	U _{OH} =2.5 V U _{OH} =4.6 V U _{OH} =9.5 V U _{OH} =13.5 V	5.0	-2.0	-1.6	-1.15	mA
			5.0	-0.64	-0.51	-0.36	
			10	-1.6	-1.3	-0.9	
			15	-4.2	-3.4	-2.4	

AC Electrical Characteristics

($C_i=50\text{pF}$, $R_f=200\text{ k}\Omega$, Input $t_r=t_f=20$)

Symbol	Parameter	V _{CC} V	Guaranteed Limit			Unit
			≥-55°C	25°C	≤125°C	
t _{PLH} , t _{PHL}	Maximum Propagation Delay, Input A or B to Output (Figure 1)	5.0	250	250	250	ns
		10	120	120	120	
		15	90	90	90	
t _{TLH} , t _{THL}	Maximum Output Transition Time, Any Output (Figure 1)	5.0	200	200	200	ns
		10	100	100	100	
		15	80	80	80	
C _{IN}	Maximum Input Capacitance	-		7.5		pF

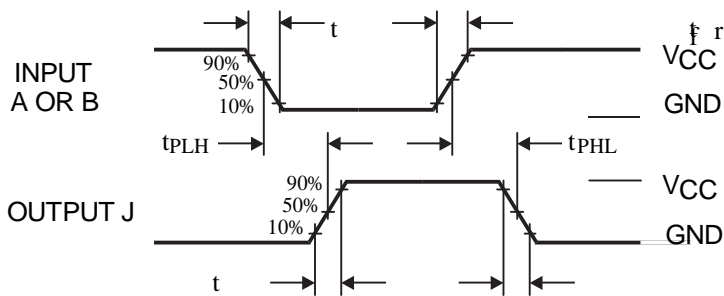


Figure 1. Switching Waveforms

Expanded Logic Diagram (1/4 of the Device)

