Preliminary

Ver.: 0.10

TFT LCD Specification

Model Name: 990000006

Customer Signature
Date

This technical specification is subjected to change without notice

Table of Contents

Record of Revision

Rev	Issued Date	Description
0.00	May 28, 2007	New create.
0.01	Jul 10, 2007	Modify item 7.1 Optical Specification
0.10	Aug. 2, 2007	Modify item 3.1 TFT LCD Panel

1. FEATURES

The 3.0” LCD module is the active matrix color TFT LCD module. LTPS (Low Temperature Poly Silicon) TFT technology is applied with vertical and horizontal drivers built on the panel.

Both of horizontal and vertical scan are reversible and controlled by the serial interface commands.

The product is designed for the requirement of the green product, and the specification complies with TPO’s “Green Product Chemical Substance Specification Standard Hand Book”.

2. GENERAL SPECIFICATIONS

Item	Description	Unit
Display Size (Diagonal)	3.0	Inch
Aspect ratio	16:9	-
Display Type	Transmissive	-
Active Area (HxV)	65.31 x 36.84	mm
Number of Dots (HxV)	960 x 240	Dot
Dot Pitch (HxV)	0.068 x 0.1535	mm
Color Arrangement	RGB Delta	-
Color Numbers	16Million	-
NTSC	40	%
Outline Dimension (HxVxT)	75.31x43.44x2.58*(Approx.)	mm
Weight	TBD	G
Panel surface treatment	Hard Coating (3H)	-

*Exclude FPC and protrusions.

3. INPUT/OUTPUT TERMINALS

3.1TFT LCD Panel

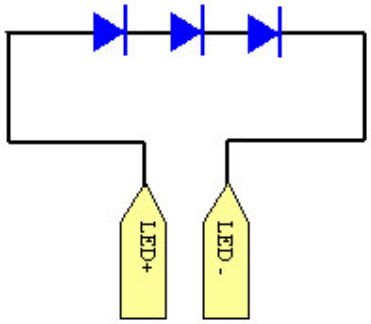
Recommend connector:

Compatible with JAE IL-FHJ-39S-HF-A1

Pin	Symbol	I/O	Description	Remark
1	CP3	C	Capacitor for power setting	
2	CP4	C	Capacitor for power setting	
3	CP5	C	Capacitor for charge pump	
4	CP6	C	Capacitor for charge pump	
5	CP7	C	Capacitor for charge pump	
6	CP8	C	Capacitor for charge pump	
7	DUMMY	--	Dummy	
8	DUMMY	--	Dummy	
9	PCD	C	Capacitor for pre-charge data signal high	
10	VCOML	C	Capacitor for VCOM low	
11	VCOMH	C	Capacitor for VCOM high	
12	AGND	--	Analog ground	
13	PVDD	C	Regulation capacitor for charge pump	
14	AVDD	C	Regulation capacitor for analog voltage	
15	CP1	C	Capacitor for charge pump	
16	CP2	C	Capacitor for charge pump	
17	PWM	O	Power transistor gate signal for the boost converter	
18	FB	I	Main boost regulator feedback input.	
19	LED-	--	LED power: cathode	Note 3-1
20	LED+	--	LED power: anode	
21	DUMMY	--	Dummy	
22	GND	--	Ground	
23	VCC	--	Power supply for digital circuit and charge pump circuit	
24	VSYNC	I	Vertical sync input. Negative polarity	
25	HSYNC	I	Horizontal sync input. Negative polarity	
26	DCLK	I	Clock signal, latch data onto line latches at the rising edge	
27	DIN0	I	Data input	
28	DIN1	I	Data input	
29	DIN2	I	Data input	
30	DIN3	I	Data input	
31	DIN4	I	Data input	

32	DIN5	I	Data input	
33	DIN6	I	Data input	
34	DIN7	I	Data input	
35	SDA	I/O	Serial interface data line	
36	SCL	I	Serial interface clock line	
37	SCEN	I	Serial interface chip enable line	
38	SHDB	I	Shutdown input	
39	GREST	I	System reset pin	

Note 3-1: The figure below shows the connection of backlight LED.



4. ABSOLUTE MAXIMUM RATINGS

Ta = 25℃

Item	Symbol	MIN	MAX	Unit	Remark
Logic Power Supply	DVDD	-0.5	5	V	
Driver Power Supply	AVDD	-0.5	6	V	
Back Light Forward Current	I_F	--	25	mA	
Operating Temperature	T_{OPR}	-10	+60	℃	
Storage Temperature	T_{STG}	-30	+80	℃	

5. ELECTRICAL CHARACTERISTICS

5.1. Driving TFT LCD Panel

GND=0V, Ta=25℃

Item		Symbol	MIN	TYP	MAX	Unit	Remark
Power Supply Voltage		V_{CC}	3	3.3	3.6	V	Note 5-1
Input Signal Voltage	Low Level	V_{IL}	GND	-	0.3x Vcc*	V	VD, HD, DCLK, DIN[0:7], SDA, SCL, SCEN, SHDB, GRESTB
	High Level	V_{IH}	0.7x Vcc*	-	Vcc*	V	
PWM Output Voltage		V_{PWM}	0	-	Vcc*	V	
Feedback Voltage		V_{FB}	0.55	0.6	0.65	V	Note 5-2
Panel Power Consumption		W_P	-	70	TBD	mW	

Vcc* =Vcc (TYP)

Note 5-1: The Vcc power is provided for overall panel module supply voltage.

Note 5-2: DC/DC feedback control voltage

5.2 Driving Backlight

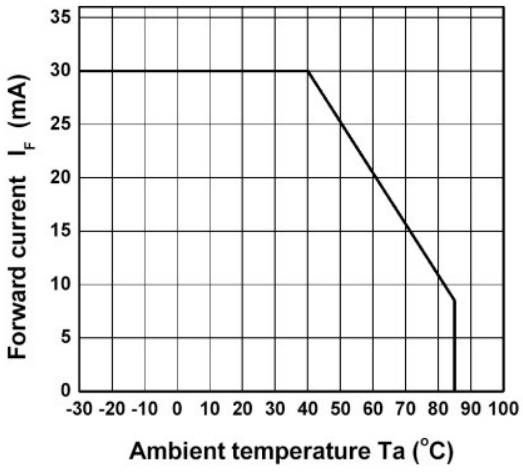
Ta=25℃

Item	Symbol	MIN	TYP	MAX	Unit	Remark
Forward Current	I_F	--	23	25	mA	Note 5-3
Forward Current Voltage	V_F	--	9.6	10.5	V	
Backlight Power Consumption	W_{BL}	--	220.8	262.5	mW	

Note 5-3: Backlight driving circuit is recommended as the fix current circuit.

* Ta: Ambient Temperature

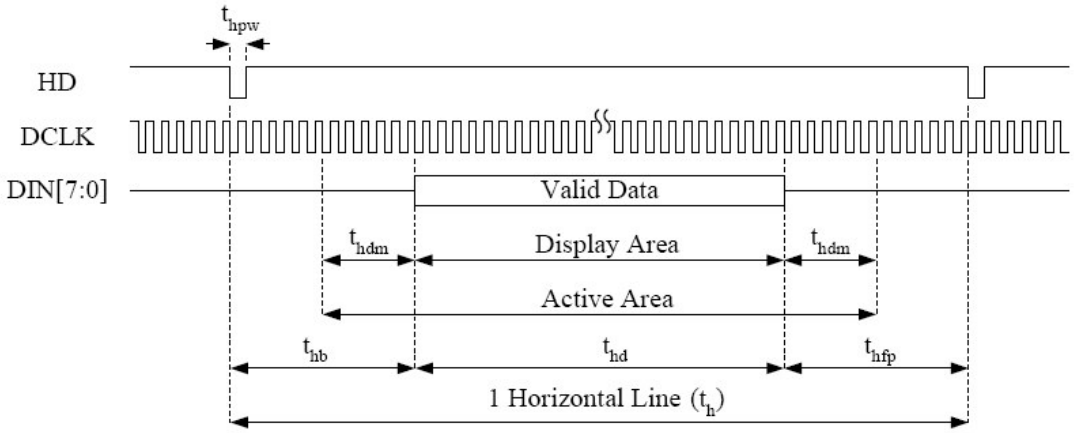
* High temperature operation: Test current refers the diagram as following.



6. TIMING CHART

<Input timing 1> Serial RGBDummy or Serial-YUV 4:2:2 mode

--Horizontal--



(1) NTSC Mode:

Parameter	Symbol	MIN	TYP	MAX	Unit
DCLK Frequency	F_{DCLK}	--	27	--	MHz
Horizontal valid data	t_{hd}	--	1440	--	DCLK
1 Horizontal Line	t_h	--	1716	--	DCLK
HSYNC Pulse Width	t_{hpw}	1	1	--	DCLK
Hsync blanking	t_{hp}	--	240	--	DCLK
Horizontal Front Porch	t_{hfp}	--	36	--	DCLK
Horizontal Dummy Time	t_{hdm}	--	0	--	DCLK

Parameter	Symbol	MIN	TYP	MAX	Unit
DCLK Frequency	F_{DCLK}	--	24.54	--	MHz
Horizontal valid data	t_{hd}	--	1280	--	DCLK
1 Horizontal Line	t_h	--	1560	--	DCLK
HSYNC Pulse Width	t_{hpw}	1	1	--	DCLK
Hsync blanking	t_{hp}	--	240	--	DCLK
Horizontal Front Porch	t_{hfp}	--	40	--	DCLK
Horizontal Dummy Time	t_{hdm}	--	0	--	DCLK

(2) PAL Mode:

Parameter	Symbol	MIN	TYP	MAX	Unit
DCLK Frequency	F_{DCLK}	--	27	--	MHz
Horizontal valid data	t_{hd}	--	1440	--	DCLK
1 Horizontal Line	t_h	--	1728	--	DCLK
HSYNC Pulse Width	t_{hpw}	1	1	--	DCLK
Hsync blanking	t_{hp}	--	240	--	DCLK
Horizontal Front Porch	t_{hfp}	--	48	--	DCLK
Horizontal Dummy Time	t_{hdm}	--	0	--	DCLK

Parameter	Symbol	MIN	TYP	MAX	Unit
DCLK Frequency	F_{DCLK}	--	24.38	--	MHz
Horizontal valid data	t_{hd}	--	1280	--	DCLK
1 Horizontal Line	t_h	--	1560	--	DCLK
HSYNC Pulse Width	t_{hpw}	1	1	--	DCLK
Hsync blanking	t_{hp}	--	240	--	DCLK
Horizontal Front Porch	t_{hfp}	--	40	--	DCLK
Horizontal Dummy Time	t_{hdm}	--	0	--	DCLK

(3) QVGA Mode:

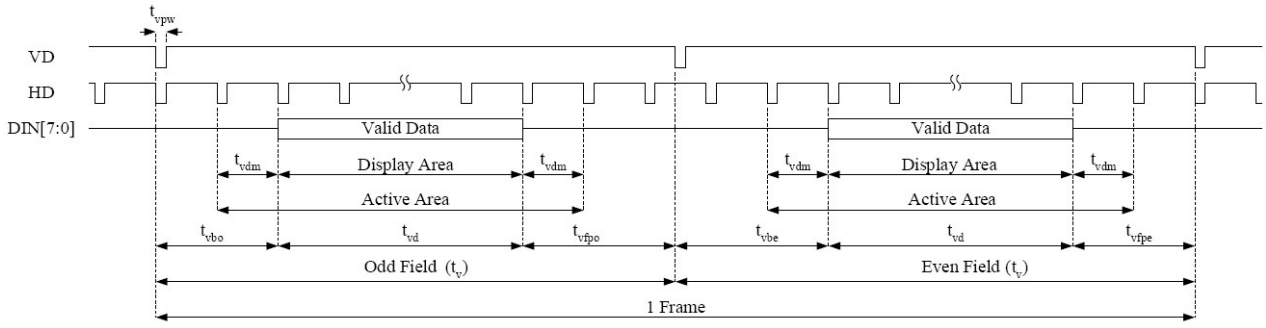
Parameter	Symbol	MIN	TYP	MAX	Unit
DCLK Frequency	F_{DCLK}	--	25	--	MHz
Horizontal valid data	t_{hd}	--	1280	--	DCLK
1 Horizontal Line	t_h	--	1560	--	DCLK
HSYNC Pulse Width	t_{hpw}	1	1	--	DCLK
Hsync blanking	t_{hp}	--	240	--	DCLK
Horizontal Front Porch	t_{hfp}	--	40	--	DCLK
Horizontal Dummy Time	t_{hdm}	--	0	--	DCLK

--Vertical--

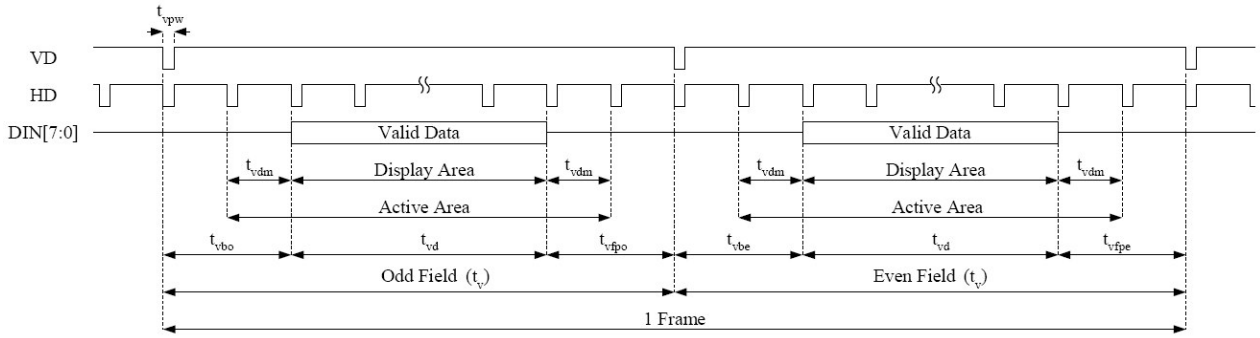
Interlace:

ODD Field: same phase VD and HD

EVEN Field: same phase VD and Half-HD



Non-interlace:



(1) Interlace Mode: NTSC/QVGA

Parameter		Symbol	MIN	TYP	MAX	Unit
Vertical valid data		t_{vd}	-	240	-	H
1 Vertical field		t_v	-	262.5	-	H
VSYNC Pulse Width		t_{vpw}	1	1	-	DCLK
Vsync blanking	Odd Field	t_{vbo}	-	21	-	H
	Even Field	t_{vbe}	-	21.5	-	H
Vertical Front Porch	Odd Field	t_{vfpo}	-	1.5	-	H
	Even Field	t_{vfpe}	-	1	-	H
Vertical dummy time		t_{vdm}	-	0	-	H

(2) Interlace Mode: PAL

Parameter		Symbol	MIN	TYP	MAX	Unit
Vertical valid data		t_{vd}	-	288	-	H
1 Vertical field		t_v	-	312.5	-	H
VSYNC Pulse Width		t_{vpw}	1	1	-	DCLK
Vsync blanking	Odd Field	t_{vbo}	-	24	-	H
	Even Field	t_{vbe}	-	24.5	-	H
Vertical Front Porch	Odd Field	t_{vfpo}	-	0.5	-	H
	Even Field	t_{vfpe}	-	0	-	H
Vertical dummy time		t_{vdm}	-	0	-	H

(3) Non-Interlace Mode: NTSC/QVGA

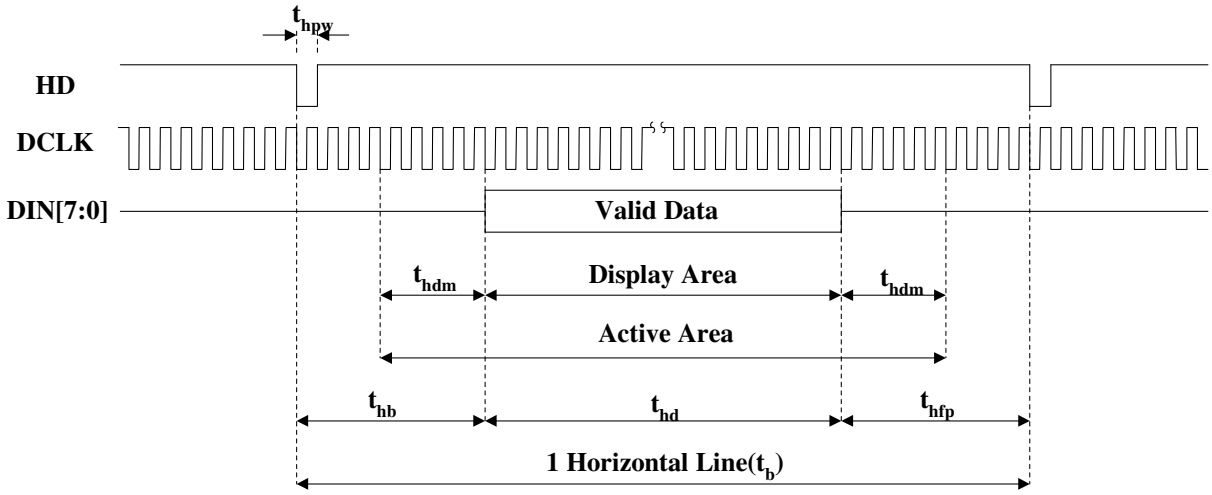
Parameter		Symbol	MIN	TYP	MAX	Unit
Vertical valid data		t_{vd}	-	240	-	H
1 Vertical field		t_v	-	262	-	H
VSYNC Pulse Width		t_{vpw}	1	1	-	DCLK
Vsync blanking	Odd Field	t_{vbo}	-	21	-	H
	Even Field	t_{vbe}	-	21	-	H
Vertical Front Porch	Odd Field	t_{vfpo}	-	1	-	H
	Even Field	t_{vfpe}	-	1	-	H
Vertical dummy time		t_{vdm}	-	0	-	H

(4) Non-Interlace Mode: PAL

Parameter		Symbol	MIN	TYP	MAX	Unit
Vertical valid data		t_{vd}	-	288	-	H
1 Vertical field		t_v	-	312	-	H
VSYNC Pulse Width		t_{vpw}	1	1	-	DCLK
Vsync blanking	Odd Field	t_{vbo}	-	24	-	H
	Even Field	t_{vbe}	-	24	-	H
Vertical Front Porch	Odd Field	t_{vfpo}	-	0	-	H
	Even Field	t_{vfpe}	-	0	-	H
Vertical dummy time		t_{vdm}	-	0	-	H

<Input timing 2> Through mode

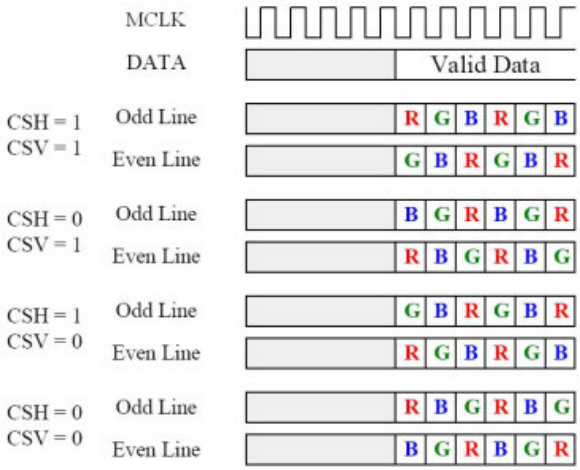
--Horizontal-



Parameter	Symbol	MIN	TYP	MAX	Unit
DCLK Frequency	F_{DCLK}	--	18.42	--	MHz
Horizontal valid data	t_{hd}	--	960	--	DCLK
1 Horizontal Line	t_h	--	1171	--	DCLK
HSYNC Pulse Width	t_{hpw}	1	1	--	DCLK
Hsync blanking	t_{hp}	--	152	--	DCLK
Hsync front porch	t_{hfp}	--	59	--	DCLK
Horizontal dummy time	t_{hdm}	--	0	--	DCLK

(1) Input RGB Sequence

Resolution (960 x 240)

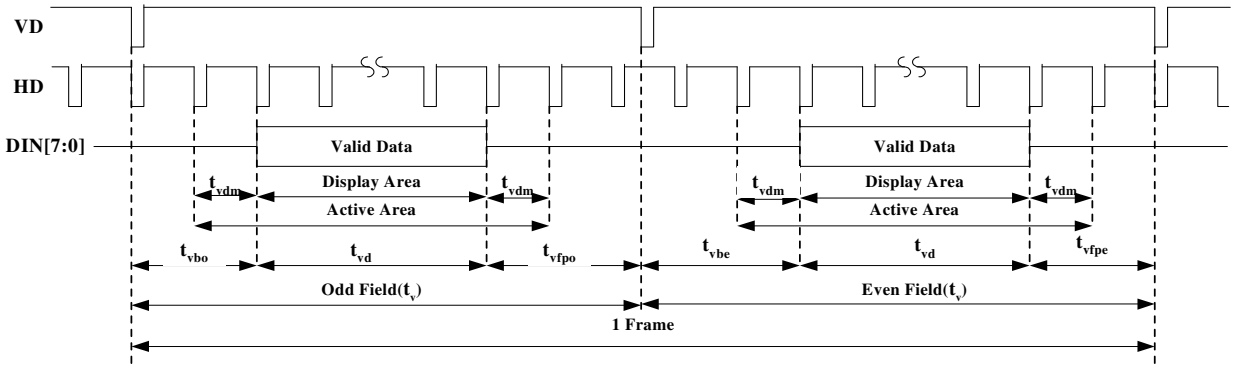


--Vertical--

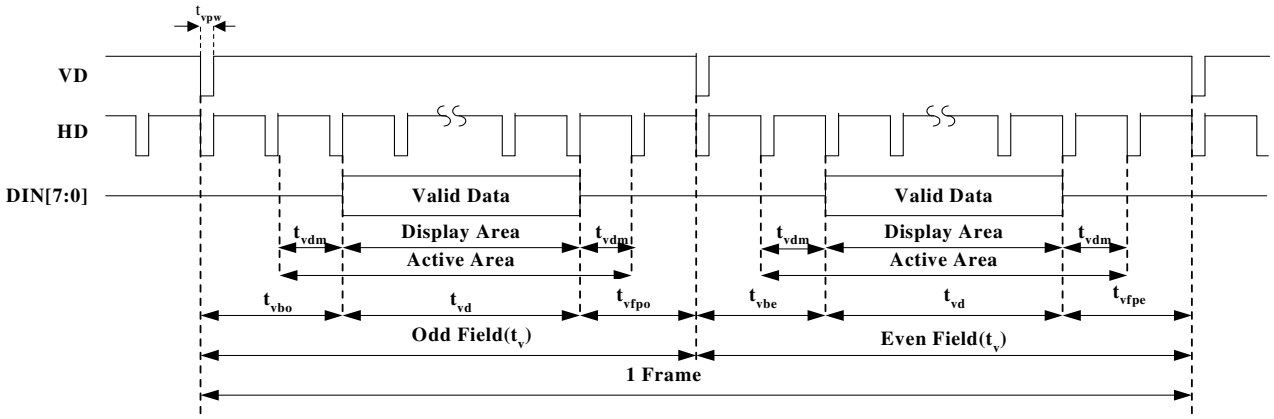
Interlace:

ODD Field: same phase VD and HD

EVEN Field: same phase VD and Half-HD



Non-interlace:



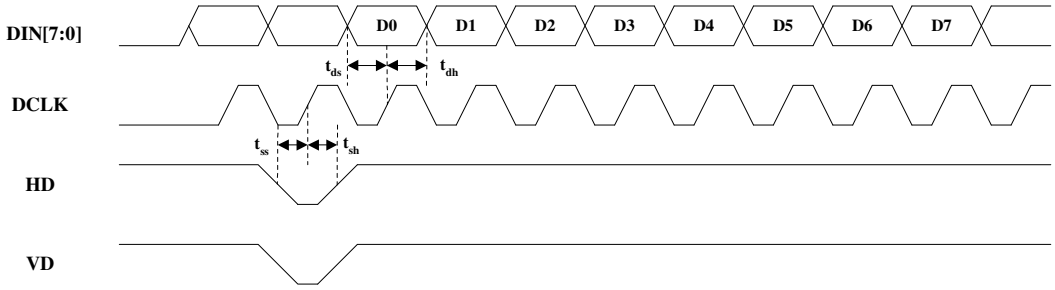
(1) Interlace Mode

Parameter		Symbol	MIN	TYP	MAX	Unit
Vertical valid data		t_{vd}	-	240	-	H
1 Vertical field		t_v	-	262.5	-	H
Vsync pulse width		t_{vpw}	1	1	-	DCLK
Vsync blanking	Odd Field	t_{vbo}	-	14	-	H
	Even Field	t_{vbe}	-	14.5	-	H
Vsync front porch	Odd Field	t_{vfpo}	-	8.5	-	H
	Even Field	t_{vfpe}	-	8		H
Vertical dummy time		t_{vdm}	-	0	-	H

(2) Non-Interlace Mode

Parameter		Symbol	MIN	TYP	MAX	Unit
Vertical valid data		t_{vd}	-	240	-	H
1 Vertical field		t_{v}	-	262	-	H
Vsync pulse width		t_{vpw}	1	1	-	DCLK
Vsync blanking	Odd Field	t_{vbo}	-	14	-	H
	Even Field	t_{vbe}	-	14	-	H
Vsync front porch	Odd Field	t_{vfpo}	-	8	-	H
	Even Field	t_{vfpe}	-	8	-	H
Vertical dummy time		t_{vdm}	-	0	-	H

<Input timing 3> Timing Diagram



Item	Symbol	MIN	TYP	MAX	Unit
DCLK Duty Ratio	Duty	40	-	60	%
Data Setup Time	t_{ds}	12	-	-	ns
Data Hold Time	t_{dh}	12	-	-	ns
Control Signal Setup Time	t_{ss}	12	-	-	ns
Control Signal Hold Time	t_{sh}	12	-	-	ns

7. OPTICAL CHARACTERISTICS

7.1 Optical Specification

Ta=25℃

Item		Symbol	Condition	MIN	TYP	MAX	Unit	Remarks
Viewing Angles		Θ11	CR ≥ 10	TBD	60	-	Degree	Note 7-1
		Θ12		TBD	60	-		
		Θ21		TBD	50	-		
		Θ22		TBD	60	-		
Contrast Ratio		CR	Θ=0°	TBD	400	-		Note 7-2
Response Time	Rising	Tr		-	5	TBD	ms	Note 7-3
	Falling	Tf		-	11	TBD		
Luminance (I_F=23mA)		L		200	250	-	cd/m^2	Note 7-4
Chromaticity	White	x_W		0.26	0.31	0.36		Note 7-5
		y_W		0.29	0.34	0.39		

7.2 Basic Measure Conditions

(1) Driving voltage

Vcc= 3 V

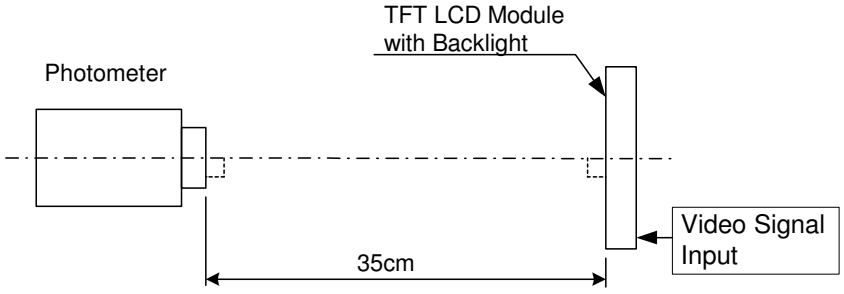
(2) Ambient Temperature: Ta=25℃

(3) Testing Point: Measure in the display center point and the test angle Θ=0°

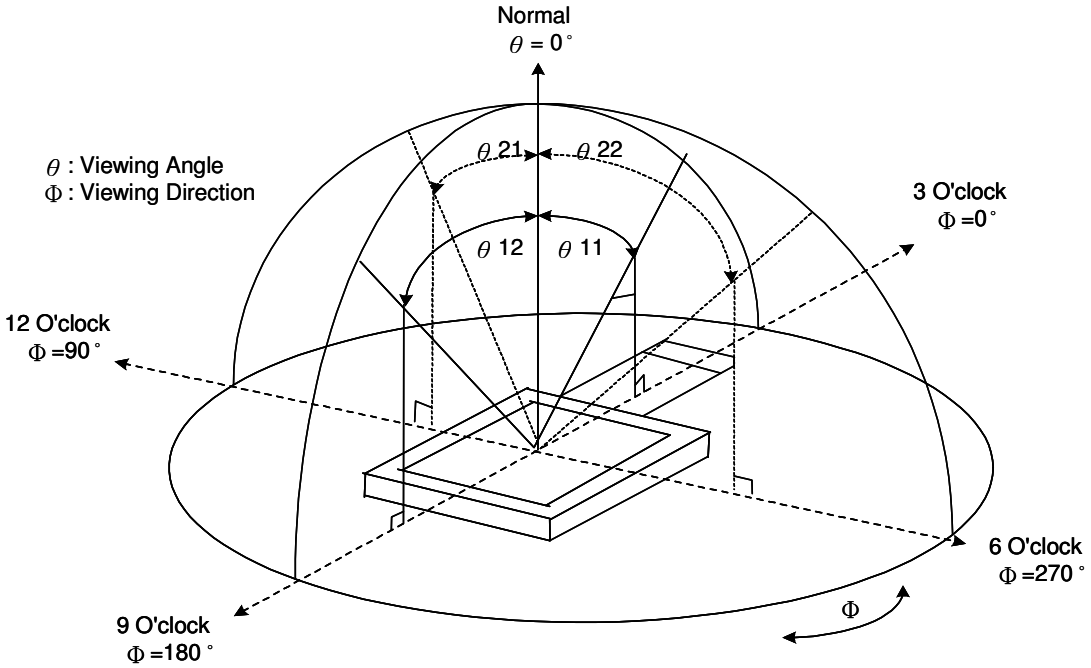
(4) LED Current: I_F=23mA.

(5) Testing Facility

Environmental illumination: ≤ 1 Lux



Note 7-1: Viewing angle diagrams:

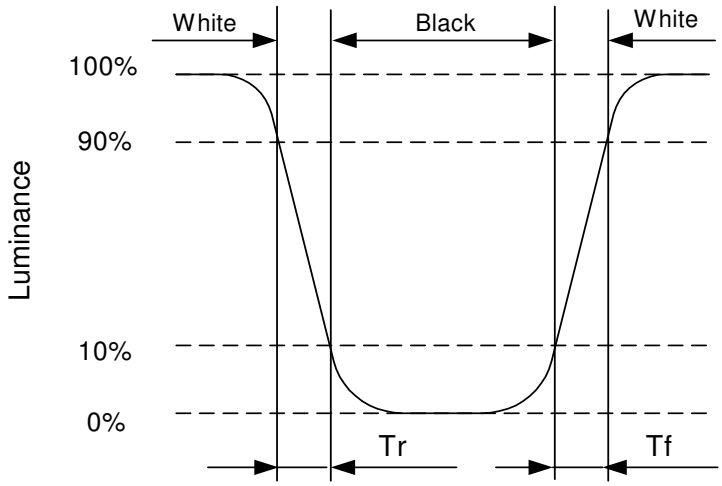


Note 7-2: Contrast Ratio:

Contrast ratio is measured in optimum common electrode voltage.

$$CR = \frac{\text{Luminance with white image}}{\text{Luminance with black image}}$$

Note 7-3: Definition of response time:



Note 7-4: Luminance:

Test Point: Display Center

Note 7-5: Chromaticity: The same test condition as Note 7-4, but change detector to spectrometer.

8 REILIABILITY

No	Test Item	Condition
1	High Temperature Operation	Ta=+60℃, 240hrs
2	High Temperature & High Humidity Operation	Ta=+40℃, 95% RH, 240hrs
3	Low Temperature Operation	Ta=-10℃, 240hrs
4	High Temperature Storage (non-operation)	Ta=+80℃, 240hrs
5	Low Temperature Storage (non-operation)	Ta=-30℃, 240hrs
6	Thermal Shock (non-operation)	-30℃←→70℃, 50 cycles 30 min 30 min
7	Surface Discharge (non-operation)	C=150pF, R=330Ω; Discharge: Air: ±15kV; Contact: ±8kV 5 times / Point; 5 Points / Panel
8	Vibration (non-operation)	Frequency: 10~55Hz; Amplitude: 1.5mm Sweep Time: 11min Test Time: 2 hrs for each direction of X, Y, Z
9	Shock (non-operation)	Acceleration: 100G; Period: 6ms Directions: ±X, ±Y, ±Z; Cycles: Twice

Ta: Ambient Temperature

9 HANDLING CAUTIONS

9.1 ESD (Electrical Static Discharge) Strategy

ESD will cause serious damage of the panel, ESD strategy is very important in handling. Following items are the recommend ESD strategy

(1) In handling LCD panel, please wear non-charged material gloves. And the conduction ring connect wrist to the earth and the conducting shoes to the earth is necessary.

(2) The machine and working table for the panel should have ESD prohibition strategy.

(3) In handling the panel, ionize flowing decrease the charge in the environment is necessary.

(4) In the process of assembly the module, shield case should connect to the ground.

9.2 Environment

(1) Working environment of the panel should in the clean room.

(2) The front polarizer is easy damaged, handle it carefully and do not scratch it by sharp material.

(3) Panel has polarizer protective film in the surface please remove the protection film of polarizer slowly with ionized air to prevent the electrostatic discharge.

9.3 Others

(1) Turn off the power supply before connecting and disconnecting signal input cable.

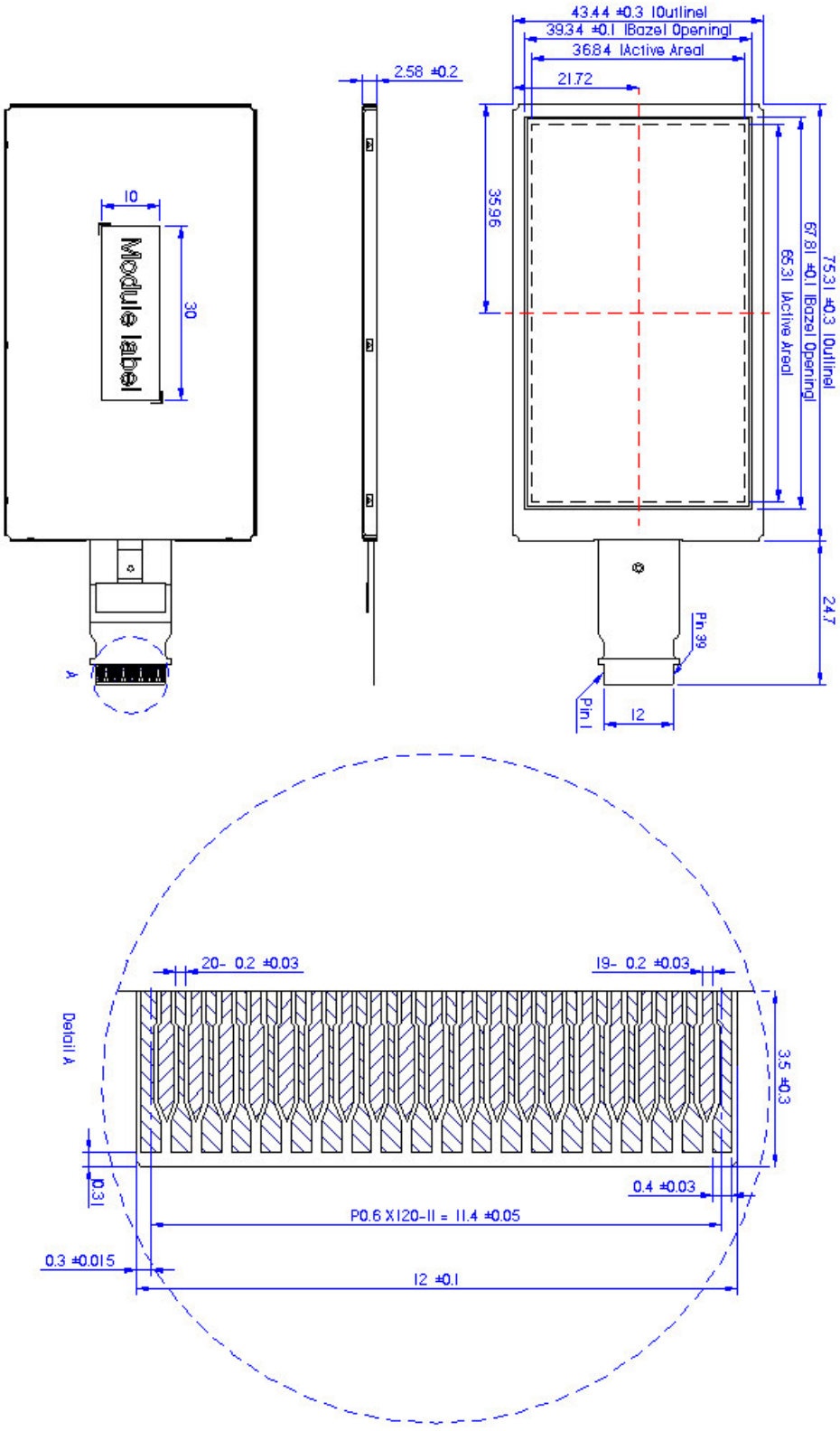
(2) The connection area of FPC and panel is very weak, do not handle panel only by FPC or bend FPC.

(3) Water drop on the surface or condensation as panel power on will corrode panel electrode.

(4) As the packing bag open, watch out the environment of the panel storage. High temperature and high humidity environment is prohibited.

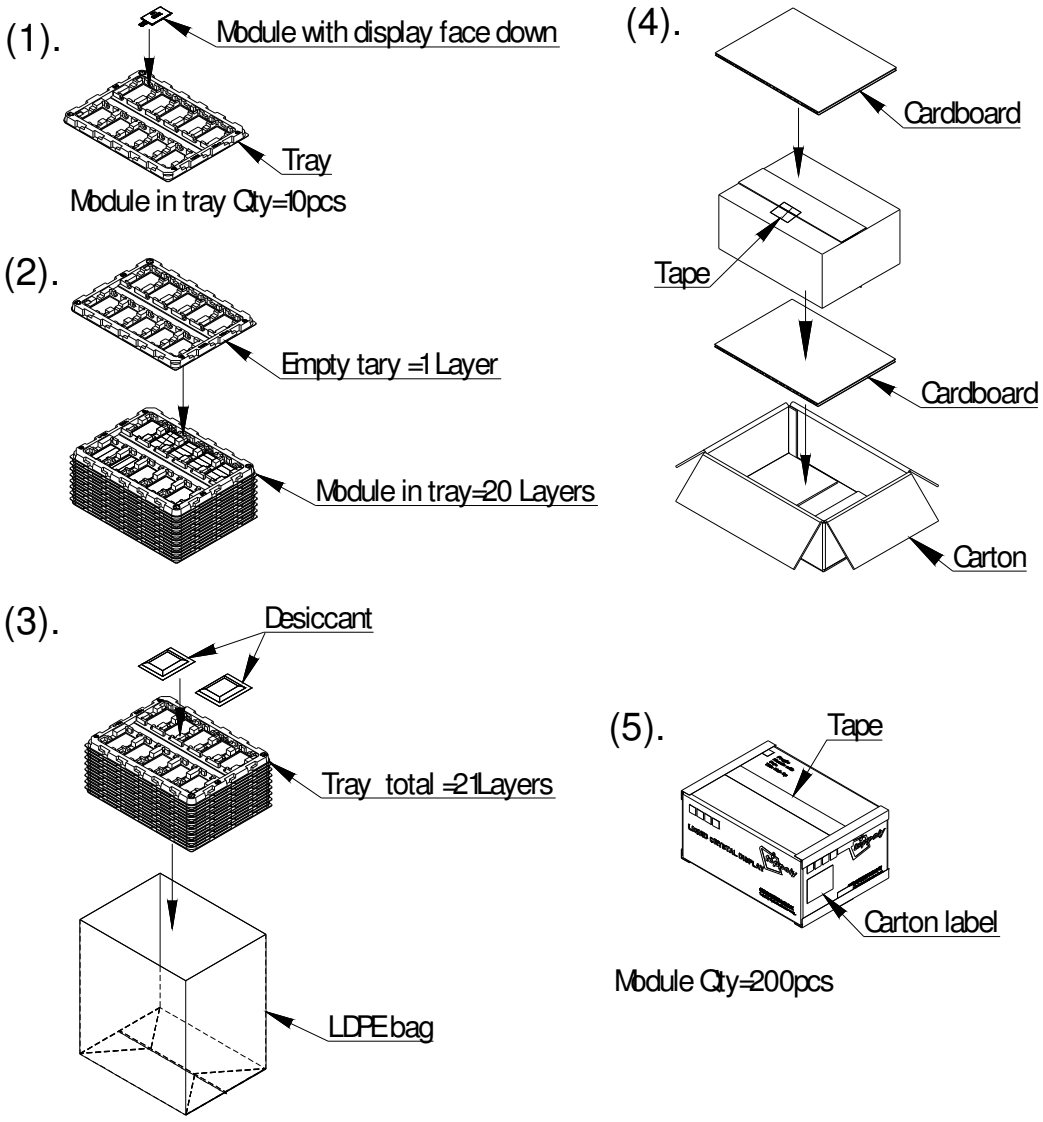
(5) When the TFT LCD module is broken, please watch out whether liquid crystal leaks out or not. If your hand touches liquid crystal, wash your hand cleanly by water and soap as soon as possible.

10 MECHANICAL DRAWING



Note: Unspecified tolerance is +/- 0.2mm

11 PACKING DRAWING



3.0" module (990000006) delivery packing method

11.1 Module packed into tray cavity (with Module display face down).

11.2 Tray stacking with 20 layers and with 1 empty tray above the stacking tray unit.
2pcs desiccant put above the empty tray

11.3 Stacking tray unit put into the LDPE bag and fix by adhesive tape.

11.4 Put 1pc cardboard inside the carton bottom, and then pack the package unit into the carton.
Put 1pc cardboard above the package unit.

11.5 Carton tapping with adhesive tape.