

SCHLAPPI ENGINEERING

The Nibbler is a four bit digital accumulator based on CMOS logic. This means that it counts in binary from zero to fifteen, with inputs and outputs for individual bits as well as stepped voltage outputs (digital to analog converters). It does this with individual logic chips instead of a CPU.

The concept here is that counting in binary (and its expression in bits) is inherently musical, and with slow clock speeds we can use it to create both rhythms and modulation voltages (or melodies). At audio rate we can generate subharmonics and modem-like sounds (or noise).

ADD SWITCHES

These four switches form a binary word, adding the indicated amount to the output register at each clock pulse.

RESET BUTTON

Clears the output register, holding all outputs at zero while the button is held if in SYNC mode and at the value indicated by the switches if in ASYNC MODE

SUBTRACT ADD SWITCH

Determines if the binary word is added or subtracted to the output register

ASYNC SYNC SWITCH

Determines if the output is updated only on a clock pulse (sync), or every time an input is received (async)

CLOCK INPUT

Input for any gate or trig signal, generally necessary for operation

RESET INPUT

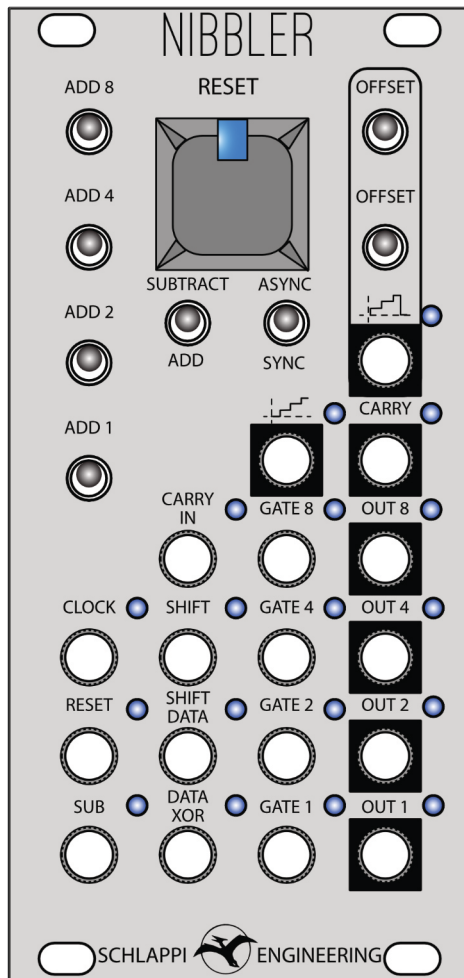
Resets the register to zero whenever a signal is received. Acts as a sync input at audio rates

SUB INPUT

Reverses the direction of the counter, XORs with the related switch.

DATA XOR INPUT

The input will be XOR'ed with whatever is present at the input to the shift register. Only active when using the SHIFT input.



OFFSET SWITCHES

These two switches set a phase offset for the related stepped voltage.

Lower offset switch	Upper offset switch	Degree offset	Numerical offset
down	down	0	0
up	down	45	2
down	up	90	4
up	up	180	8

STEPPED OUTPUTS

Stepped voltages made by adding the 4 gate outputs together with binary weights

CARRY OUTPUT

Gate output that goes high for one clock pulse when the accumulator overflows. Can be used to chain multiple nibblers or as a clock divider output.

GATE OUTPUTS

OUT1, OUT2, OUT4, OUT8 combined form a binary word and are the current contents of the output register. They can be used as clock dividers or to create rhythms.

SHIFT INPUT

If in SYNC mode then when the SHIFT is high then on clock pulses the register shifts up instead of adding, in ASYNC mode the register will shift on each pulse.

SHIFT DATA

Replaces the input of the shift register
With no input the top bit (OUT 8) cycles around and enters from the bottom.

GATE INPUTS

GATE 1, GATE 2, GATE 4, GATE 8 add to their respective switches then are added to the output register. Can be used without a clock.

PRO TIPS :

- *Black square around a jack indicates output, all others are inputs
- *A clock input is generally required
- *Check that at least one ADD switch is up

PATCHES TO START WITH

CLOCK DIVIDER

SWITCH POSITIONS **SUBTRACT ADD** ADD
 ASync SYNC SYNC
 ADD 1 **UP**
 OTHER SWITCHES DOWN

- CLOCK signal at CLOCK input
- take divider output from CARRY
- With only ADD1 up you will have divide by 16
- only ADD2 will give you divide by 8, ADD 4 will divider by 4
- Push the switches down and raise only ADD 8 for divider by 2
- In generally the ADD switches form the numerator of a divide by 16 calculation
- Try the GATE OUTPUTS to get other divisions

STEPPED VOLTAGES

- Start from the CLOCK DIVIDER patch
- Plug the two stepped (sawtooth) voltages into a pitched input
- Try different switch settings for different sequences

AUDIO RATE (FREQUENCY DIVIDER)

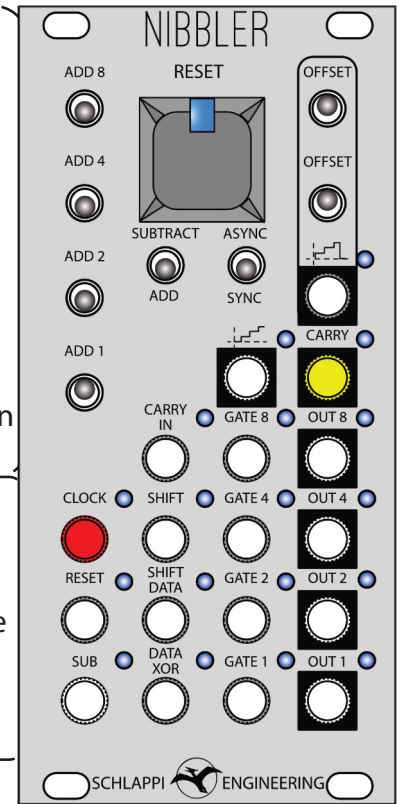
- Start from CLOCK DIVIDER patch
- Input audio at CLOCK input
- Listen to CARRY or GATE outs for pulse waves
- Listen to stepped outputs for saw, triangle, or other waveform outputs

TRIANGLE WAVE

- Start from STEPPED VOLTAGES
- Patch the CARRY out into SUB input
- This will cause the accumulator to alternate counting up and down, resulting in a triangle wave
- Works at LFO or audio rate

SHIFT REGISTER NOISE

- Start from AUDIO RATE patch
- Patch signals into the SHIFT INPUT
- Try all the other inputs as well



A BIT OF THEORY

The Nibbler is at it's core a 4-bit accumulator. That is an adder combined with a register (or memory), this means on each clock pulse the the accumulator word is added to itself (or the existing contents of the register). This is a core component of digital oscillators and filters.

