Graphenea

Measurement Protocols and Handling Instructions

Graphene Field-Effect Transistor Chip: S12

Typical Measurement Configurations

The following explains the electrical measurements that can be performed on the different devices in GFET S-12.

2-probe devices

These devices allow field-effect measurements by simultaneously applying two voltages:

- Source-drain voltage (V_{SD}): applied between the two probes (source and drain), while one of them is grounded (see Figure 1a). V_{SD} enables the transport of charge carriers through the graphene channel, with an associated source-drain current (I_{SD}). V_{SD} can be varied in order to get the desired I_{SD} outcome (see Figure 1b).
- Gate voltage (V_G): applied to the Si on the substrate. V_G creates an electric field on the graphene channel, modulating the conductivity of graphene oxide (see Figure 1c). However, it is not particularly useful in this device configuration.

The Si can be contacted either from the top surface by scratching the 90 nm-thick SiO_2 with a diamond pen in one of the chip corners; or alternatively from the underside of the chip, for instance using a probe station chuck.

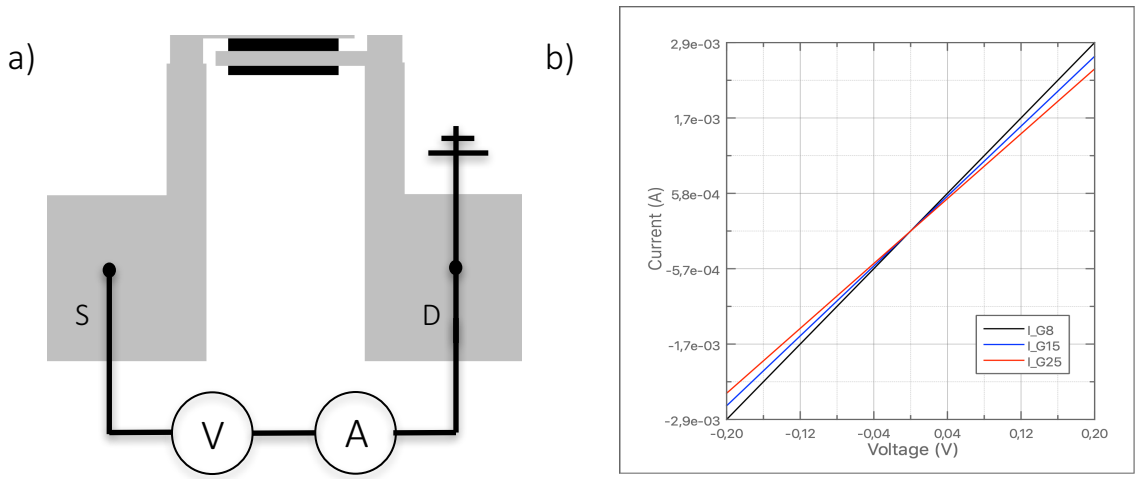

Figure 1. a) Scheme of the 2-probe device, with the corresponding electrical measurement configuration. b) Typical I_d-V_{sd} curves for different widths

Interdigitated electrodes

These devices have interdigitated electrodes (see Fig.2). These contacts are ideal for gas sensing applications, where the conductance modulation can be small and the small signal can indeed be lost due to large resistances and thus voltage drops between electrodes.
This contact scheme also provides larger current densities for the same amount of voltage, compared with a traditional 2-probe geometry, without affecting much the active area and actual device footprint.

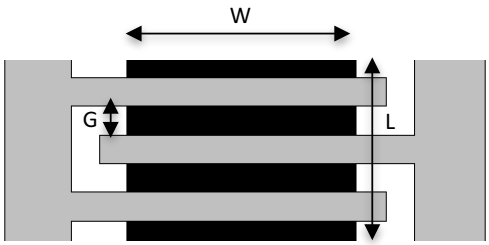

Figure 2. Scheme of the interdigitated electrode geometry.

The resistivity of graphene is usually expressed per thickness unit, i.e. the so-called sheet resistance R_s:

$$R = R_S \frac{L}{W},$$

being R the resistance of graphene oxide and W and L the width and inner length of the graphene channel, respectively. In an interdigitated electrode configuration with n pairs of fingers, its resistance R_n changes to

$$R_n = R_S \frac{G}{nW},$$

being G the gap between electrodes. Thus, the relation ship between R_n and R is

$$R_n = R \frac{G}{nL},$$

In the geometries presented here a factor of 5 orders of magnitude in current densities should be achieved compared with a 2-probe geometry.

Doping-reduction treatment

Graphene on SiO_2 is often p-doped after exposure to air due to the adsorption of water molecules and other adsorbates with the effect that the Dirac point is shifted to positive gate voltages and can cause the Dirac voltage to be located out of the recommended gate voltage range. In addition, a large hysteresis is observed between the forward and backward sweeps of a transfer curve.

Immersing the GFET chip in acetone for at least 12h reduces doping. After that, the chip should be rinsed with IPA, properly dried with an Ar or N_2 gun, and shortly introduced into the measurement equipment. In order to preserve the effectivity of this treatment, electrical characterization should be carried out in inert atmosphere or vacuum.

In addition, storage of the chips in a low humidity environment (N_2 cabinet, desiccator, or vacuum) is highly recommended.

Basic handling instructions

The graphene used in our GFETs is high-quality monolayer CVD graphene and highly prone to damage by external factors. To maintain the quality of your devices, we recommend taking the following precautions:

- Be careful when handling the GFET chip that tweezers do not make contact with the device area. Metallic tweezers should be avoided, as they can damage/scratch the chip edges/surface
- Treat the devices as sensitive electronic devices and take precautions against electrostatic discharge
- Ideally store in inert atmosphere or under vacuum in order to minimize adsorption of unknown species from the ambient air
- Do not ultrasonicate the GFET dies
- Do not apply any plasma treatment to the GFET dies
- Do not subject the GFET dies to strongly oxidizing reagents

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