

## Measurement Protocols and Handling Instructions

### Graphene Field-Effect Transistor Chip: GFET-S10

#### Typical Measurement Configurations

The following explains the electrical measurements that can be performed on the different devices in GFET-S10.

#### 2-probe devices

These devices allow field-effect measurements by simultaneously applying two voltages:

- Source-drain voltage ( $V_{SD}$ ): applied between the two probes (source and drain), while one of them is grounded (see Figure 1a).  $V_{SD}$  enables the transport of charge carriers through the graphene channel, with an associated source-drain current ( $I_{SD}$ ).  $V_{SD}$  can be varied in order to get the desired  $I_{SD}$  outcome (see Figure 1b).
- Gate voltage ( $V_G$ ): applied to the Si on the substrate.  $V_G$  creates an electric field on the graphene channel, modulating the conductivity of graphene (see Figure 1c).

The Si can be contacted either from the top surface by scratching the 90 nm-thick  $\text{SiO}_2$  with a diamond pen in one of the chip corners; or alternatively from the underside of the chip, for instance using a probe station chuck.

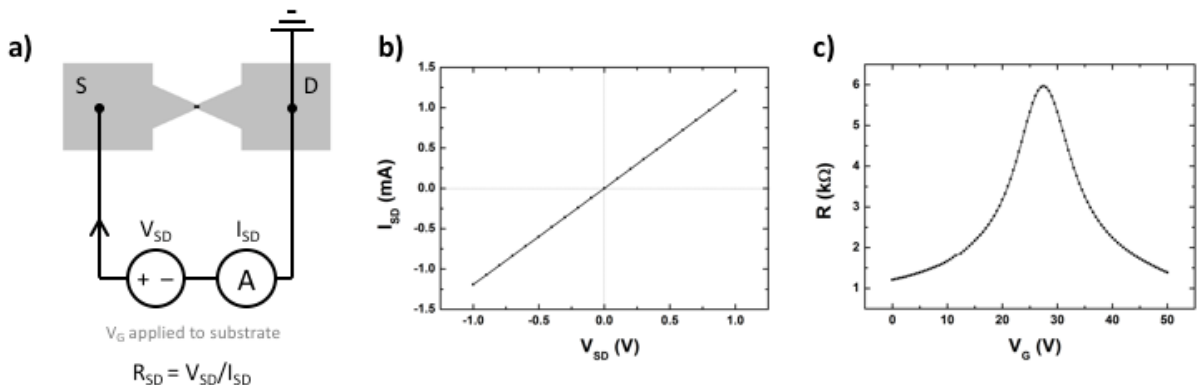


Figure 1. a) Scheme of the 2-probe device, with the corresponding electrical measurement configuration. b) Typical output curve measured at room temperature and vacuum conditions. c) Typical transfer curve measured at  $V_{SD}=20\text{mV}$  (right), measured at the same conditions as in b).

## Hall Bars

### Field-effect measurement

A common modification on the 2-probe GFET measurement is to apply a source-drain voltage between two outer contacts, measure the current between those two contacts but additionally measure the voltage directly across the graphene channel using two additional inner contacts,  $V_{12}$  (see Figure 2). The benefit of this is that the resistance of the graphene channel alone can be measured without including any voltage drops at the graphene-metal interfaces.

The graphene-metal interface resistance does depend on  $V_G$  but not in the same way as the graphene channel resistance therefore measuring the graphene channel resistance directly in the 4-probe measurement configuration can achieve greater sensitivity to applied gate fields or surface charge changes.

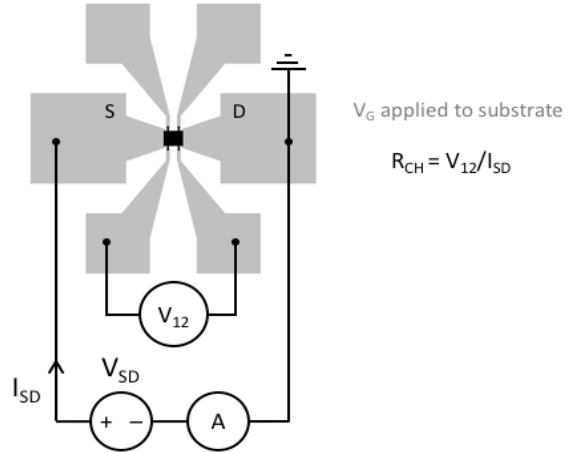


Figure 2. Scheme of the 4-probe measurement in a Hall bar device, with the corresponding electrical measurement configuration.

The resistivity of graphene is usually expressed per thickness unit, i.e. the so-called sheet resistance:

$$R_S = R_{CH} \frac{W}{L1},$$

being  $R_{CH}$  the resistance of the graphene channel, and  $W$  and  $L1$  the width and inner length of the graphene channel, respectively. The field-effect mobility ( $\mu_{FE}$ ) can be calculated by using the following equation:

$$\mu_{FE} = g \cdot \frac{1}{C_{SiO2}},$$

where:

- $g = d\sigma/dV_G$  is the transconductance, being  $\sigma=1/R_S$ ,
- $C_{SiO2}$  is the capacitance per unit area of the 90 nm-thick  $SiO_2$  dielectric.

$\mu_{FE}$  is usually calculated using the maximum transconductance.

## Hall Bars

### Hall measurement

Hall measurements are an alternative for extracting the mobility and charge carrier density on graphene. In this case,  $V_{SD}$  is applied between the longitudinal contacts, whereas the transversal voltage or Hall voltage,  $V_H$ , is measured.  $V_H$  varies with the out-of-plane applied magnetic field,  $B$ : due to the Lorentz force that the charge carriers experience, which deflect them toward the transverse contact, an electric field is created and measured by  $V_H$  (see Figure 3a).

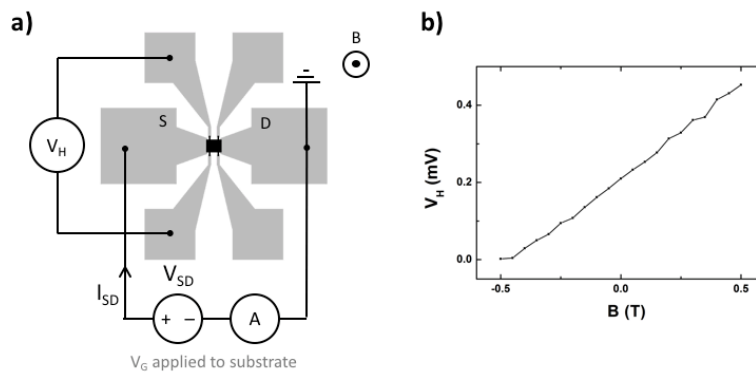


Figure 3. a) Scheme of the Hall measurement configuration in a Hall bar. b) Typical Hall measurement, performed at room temperature and vacuum conditions, with  $I_{SD} = 10 \mu A$ .

The Hall mobility ( $\mu_H$ ) and charge carrier density ( $n_H$ ) are calculated as follows:

$$n_H = \frac{1}{R_H \cdot e}$$

where  $R_H$  is the Hall coefficient:

$$R_H = \frac{dV_H}{dB} \cdot \frac{1}{I_{SD}}$$

Lastly, the mobility can be calculated as:

$$\mu_H = \frac{n_H \cdot e}{R_S}$$

## Doping-reduction treatment

Graphene on SiO<sub>2</sub> is often p-doped after exposure to air due to the adsorption of water molecules and other adsorbates with the effect that the Dirac point is shifted to positive gate voltages and can cause the Dirac voltage to be located out of the recommended gate voltage range. In addition, a large hysteresis is observed between the forward and backward sweeps of a transfer curve.

**Immersing the GFET chip in acetone for at least 12h reduces doping.** After that, the chip should be rinsed with IPA, properly dried with an Ar or N<sub>2</sub> gun, and shortly introduced into the measurement equipment. In order to preserve the effectivity of this treatment, electrical characterization should be carried out in inert atmosphere or vacuum.

In addition, storage of the chips in a low humidity environment (N<sub>2</sub> cabinet, desiccator, or vacuum) is highly recommended.

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## Basic handling instructions

The graphene used in our GFETs is high-quality monolayer CVD graphene and highly prone to damage by external factors. To maintain the quality of your devices, we recommend taking the following precautions:

- Be careful when handling the GFET chip that tweezers do not make contact with the device area. Metallic tweezers should be avoided, as they can damage/scratch the chip edges/surface
  - Treat the devices as sensitive electronic devices and take precautions against electrostatic discharge
  - Ideally store in inert atmosphere or under vacuum in order to minimize adsorption of unknown species from the ambient air
  - Do not ultrasonicate the GFET dies
  - Do not apply any plasma treatment to the GFET dies
  - Do not subject the GFET dies to strongly oxidizing reagents
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