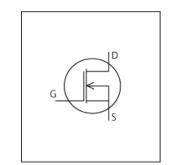


# PSpice Model NMOS Infineon IPD65R660CFDA



### **Model Information**

Model A macro model based on BSIM3 model

Call Name MDC\_IPD65R660CFDA\_PS

Pin Assign 1:G 2:D 3:S

File List Model Library MDC\_IPD65R660CFDA\_PS03.lib

Model Report MDC\_IPD65R660CFDA\_PS.pdf (this file)

**Verified Simulator Version** 

Note

PSpice version 17.2

#### References

The information which was used for modeling is as follow:

[Data Sheet]

Date/VersionProduct name2016-04-18IPD65R660CFDA

■Company name Infineon Technologies AG

● Characteristics IdVds[Vgs],IdVds[Vgs]2,Rds(on)Id[Vgs],Rds(on)Temp[Id],IdV

gs[Temp],IsVsd[Temp],VgsQg[Vdd],BvTemp[ir],Capacitance Vds[Cname],SwitchingIdd[Tname],Trrlf[Ir],Qrrlf[Ir],Switching

Waveform, Trr Waveform

#### Simulation Range

This table shows the range of evaluated simulation range that was not occurs any convergence problems in this area.

| Item                      | Range |    |      | Unit  |
|---------------------------|-------|----|------|-------|
|                           | Min.  |    | Max. |       |
| Drain-source voltage (DC) | 0     | to | 650  | V     |
| Gate-source voltage (DC)  | -20   | to | 20   | V     |
| Temperature               | -40   | to | 150  | deg C |



**Model Functions Table** 

## **MOSFET**

O:Implemented

×: Not Implemented

—: Not applicable

## RANK=1

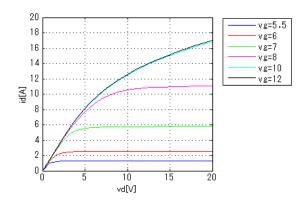
|                  | IVAIVIK-1 |             |
|------------------|-----------|-------------|
| Functions        | RANK      | Implemented |
| ID-VDS-VGS       | 1         | 0           |
| ID-VGS(Temp)     | 1         | 0           |
| RDS(on)          | 1         | 0           |
| Capacitance      | 1         | 0           |
| Gate Charge      | 1         | 0           |
| IS-VSD(Forward)  | 1         | 0           |
| Reverse recovery | 1         | 0           |
| Switching(Typ.)  | 1         | 0           |
| Bv               | 1         | 0           |
| Yfs              | 1         | _           |
| Vth              | 1         | _           |



Simulation results are following. Explanatory notes — : simulated

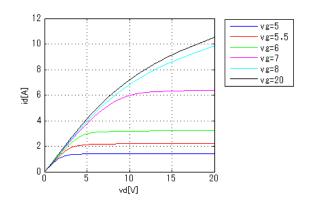
#### IdVds[Vgs]

Temp = 25degC



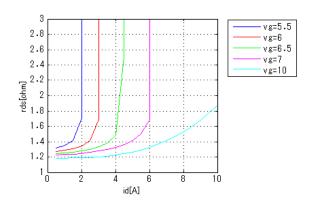
#### IdVds[Vgs]2

Temp = 125degC



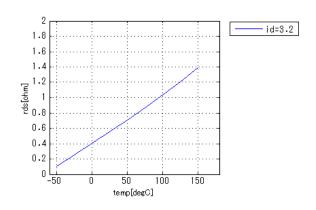
#### Rds(on)Id[Vgs]

Temp = 125degC



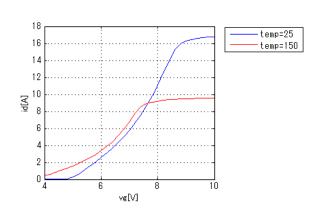
#### Rds(on)Temp[Id]

Vgs = 10V



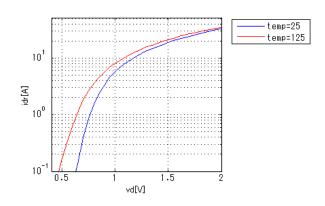
#### IdVgs[Temp]

Vds = 20V



#### IsVsd[Temp]

vg = 0V

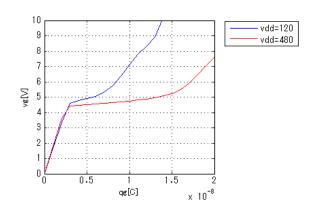




Simulation results are following. Explanatory notes — : simulated

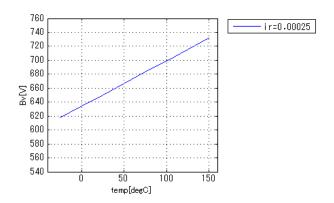
#### VgsQg[Vdd]

Id = 19.2A



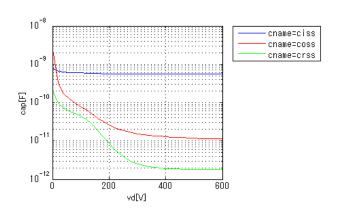
#### BvTemp[ir]

ir = 0.25E-3A



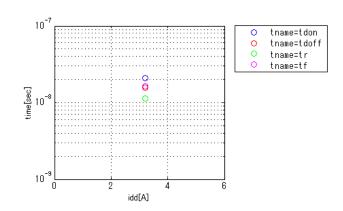
#### CapacitanceVds[Cname]

freq = 1000000Hz



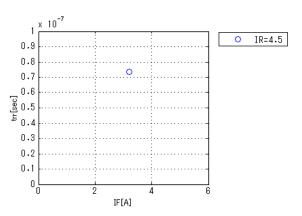
### Switchingldd[Tname]

vgg = 13V, vdd = 400V, RGG = 6.80hm



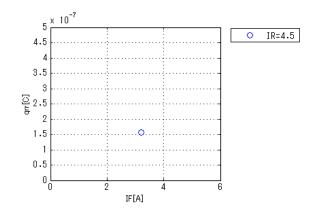
#### Trrlf[lr]

vdd = 400V, didt = 100A/us, Temp = 25degC



#### Qrrlf[lr]

vdd = 400V, didt = 100A/us, Temp = 25degC

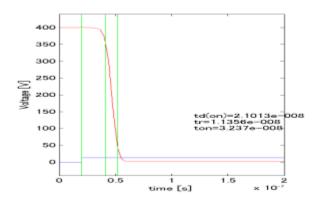


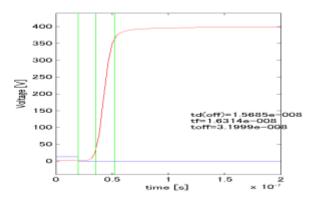


Simulation results are following. Explanatory notes — : simulated

#### Switching Waveform ( Blue : INPUT Red : OUTPUT )

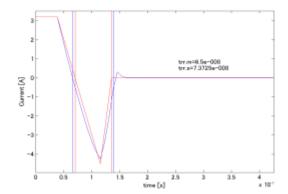
vgg = 13V, vdd = 400V, RGG = 6.8ohm, icc = 3.2A





#### Trr Waveform (Red : Datasheet Blue : Simulation )

vdd = 400V, didt = 100A/us, Temp = 25degC icc = 3.2A





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MoDeCH Inc.

**Head Office** 

Location: 5-15 Yokoyama-cho, Hachioji-Shi, Tokyo 192-0081, Japan

Tel:+81-42-656-3360

E-Mail:model-on-support@modech.co.jp

URL:http://www.modech.com/en/