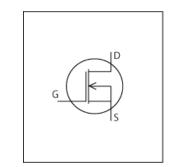


PSpice Model NMOS Potens PDD6988-5



Model Information

Model A macro model based on BSIM3 model

Call Name MDC_PDD6988-5_PS

Pin Assign 1:D 2:G 3:S

File List Model Library MDC_PDD6988-5_PS02.lib

Model Report MDC_PDD6988-5_PS.pdf (this file)

Verified Simulator Version PSpice version 17.2

Note

References

The information which was used for modeling is as follow:

[Data Sheet]

Date/Version UnknownProduct name PDD6988-5

Company namePotens Semiconductor

Characteristics NormRds(on)Temp[Id],NormVthTemp[ID],VgsQg[Vdd],IdVds

[Vgs],Rds(on)Id[Vgs],CapacitanceVds[Cname],SwitchingIdd[

Tname], Trrlf[Ir], Qrrlf[Ir], Vsdls[Temp], Vth Temp[Id], Switching

Waveform, TrrWaveform

Simulation Range

This table shows the range of evaluated simulation range that was not occurs any convergence problems in this area.

| Item | Range | | | Unit |
|---------------------------|-------|----|------|-------|
| | Min. | | Max. | |
| Drain-source voltage (DC) | 0 | to | 65 | V |
| Gate-source voltage (DC) | -12 | to | 20 | V |
| Temperature | -55 | to | 150 | deg C |



Model Functions Table

MOSFET

O: Implemented

×: Not Implemented

—: Not applicable

RANK=1

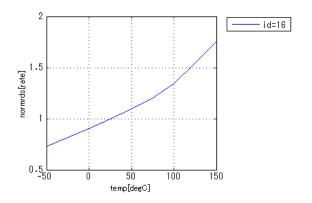
| | TO HAIR-I | |
|------------------|-----------|-------------|
| Functions | RANK | Implemented |
| ID-VDS-VGS | 1 | 0 |
| ID-VGS(Temp) | 1 | _ |
| RDS(on) | 1 | 0 |
| Capacitance | 1 | 0 |
| Gate Charge | 1 | 0 |
| IS-VSD(Forward) | 1 | 0 |
| Reverse recovery | 1 | 0 |
| Switching(Typ.) | 1 | 0 |
| Bv | 1 | _ |
| Yfs | 1 | _ |
| Vth | 1 | 0 |



Simulation results are following. Explanatory notes — : simulated

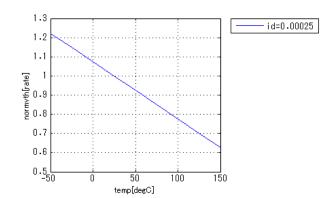
NormRds(on)Temp[Id]

Vgs = 10V



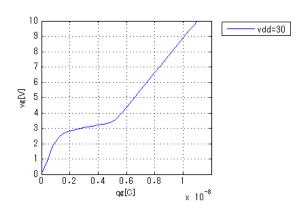
NormVthTemp[Id]

Vd = Vg



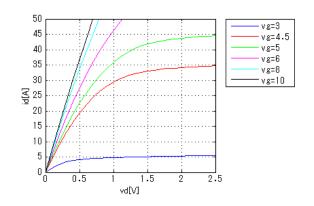
VgsQg[Vdd]

Id = 12A



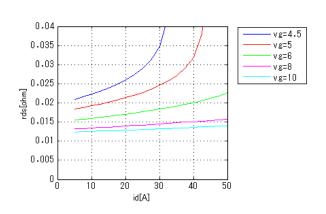
IdVds[Vgs]

Temp = 25degC



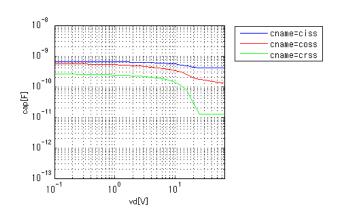
Rds(on)Id[Vgs]

Temp = 25degC



CapacitanceVds[Cname]

freq = 1000000Hz

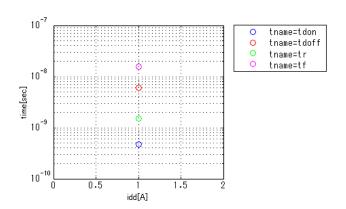




Simulation results are following. Explanatory notes — : simulated

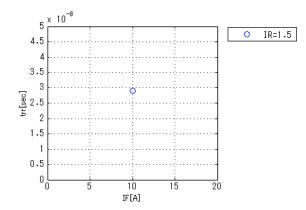
SwitchingIdd[Tname]

vgg = 10V, vdd = 30V, RGG = 3.3ohm



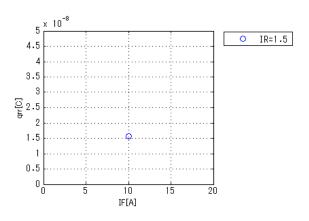
Trrlf[lr]

vdd = 30V, didt = 100A/us, Temp = 25degC



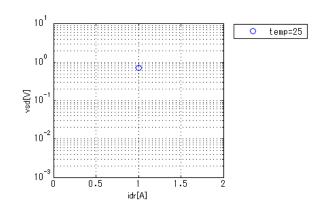
Qrrlf[lr]

vdd = 30V, didt = 100A/us, Temp = 25degC



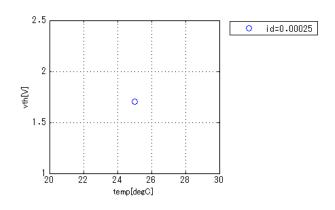
Vsdls[Temp]

vg = 0V



VthTemp[Id]

Vd = Vg

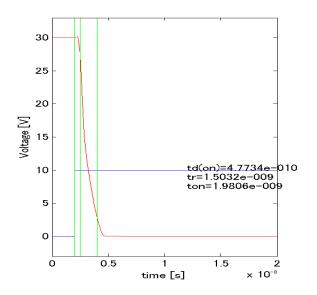


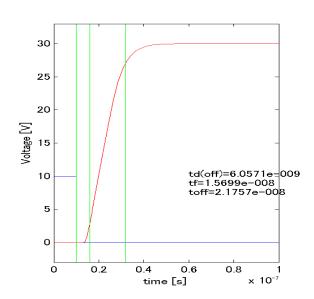


Simulation results are following. Explanatory notes — : simulated

Switching Waveform (Blue: INPUT Red: OUTPUT)

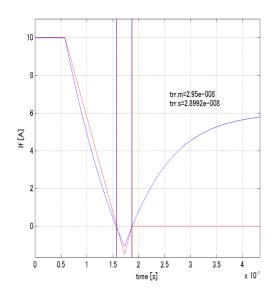
vgg = 10V, vdd = 30V, RGG = 3.3ohm, Temp = 25degC, Id = 1A





Trr Waveform (Red: Datasheet Blue: Simulation)

didt = 100A/us, vcc = 30V, if = 10A, ir = 1.5A





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