MDC_IPB180N04S4L-01_LT

LTspice Model NMOS Infineon IPB180N04S4L-01

Model Information

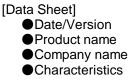
| Model Call Name | A macro model based on BSIM3 model MDC IPB180N04S4L-01 LT | | |
|--------------------|--------------------------------------------------------------|------------------------------------------------------------------------|--|
| Pin Assign | 1:G 2:S 3:S 4:D 5:S 6:S 7:S | | |
| File List | Model Library Model Report | MDC_IPB180N04S4L-01_LT01.lib MDC_IPB180N04S4L-01_LT.pdf (this file) | |

Verified Simulator Version Note

LTspice version XVII

References

The information which was used for modeling is as follow:

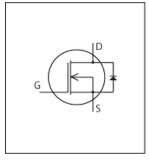


Rev. 1.0 2013-06-03 IPB180N04S4L-01 Infineon Technologies AG IdVds[Vgs],Rds(on)Id[Vgs],IdVgs[Temp],Rds(on)Temp[Id],Vt hTemp[Id],CapacitanceVds[Cname],IsVsd[Temp],BvTemp[ir] ,VgsQg[Vdd],SwitchingIdd[Tname],TrrIf[Ir],QrrIf[Ir],Switching Waveform,TrrWaveform

Simulation Range

This table shows the range of evaluated simulation range that was not occurs any convergence problems in this area.

| Item | Range | | Unit | |
|---------------------------|-------|----|------|-------|
| | Min. | | Max. | |
| Drain-source voltage (DC) | 0 | to | 40 | V |
| Gate-source voltage (DC) | -16 | to | 20 | V |
| Temperature | -55 | to | 175 | deg C |



Modech

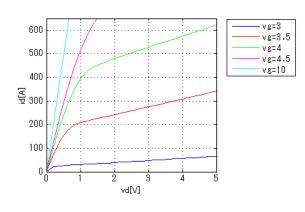
| MOSFET | | O : Implemented × : Not Implemented — : Not applicable | |
|-----------------------|--------|--------------------------------------------------------------|--|
| Model Functions Table | RANK=1 | | |
| Functions | RANK | Implemented | |
| ID-VDS-VGS | 1 | 0 | |
| ID-VGS(Temp) | 1 | 0 | |
| RDS(on) | 1 | 0 | |
| Capacitance | 1 | 0 | |
| Gate Charge | 1 | 0 | |
| IS-VSD(Forward) | 1 | 0 | |
| Reverse recovery | 1 | 0 | |
| Switching(Typ.) | 1 | 0 | |
| Bv | 1 | 0 | |
| Yfs | 1 | — | |
| Vth | 1 | 0 | |



Simulation results are following. Explanatory notes — : simulated

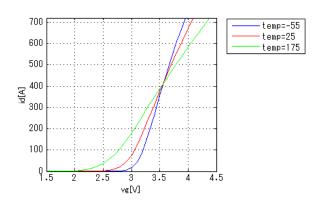
ldVds[Vgs]

Temp = 25degC



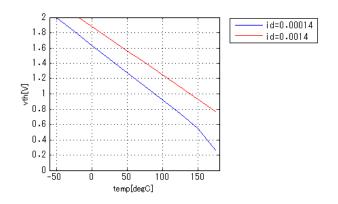
ldVgs[Temp]

Vds = 6V



VthTemp[Id]

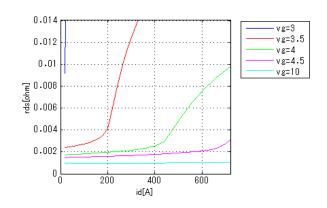
Vd = Vg



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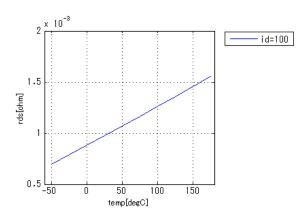
Rds(on)ld[Vgs]

Temp = 25degC



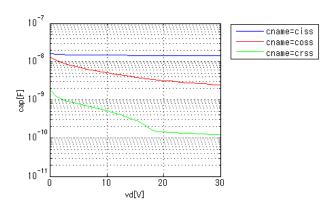
Rds(on)Temp[Id]

Vgs = 10V



CapacitanceVds[Cname]

freq = 1000000Hz

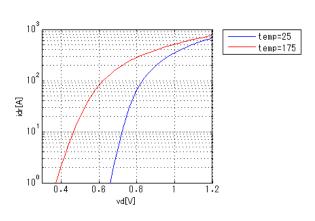




Simulation results are following. Explanatory notes — : simulated

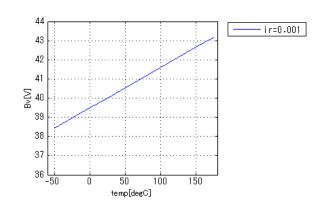
IsVsd[Temp]





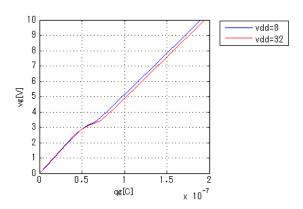
BvTemp[ir]

ir = 0.001A



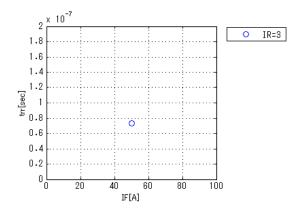
VgsQg[Vdd]

ld = 180A



Trrlf[lr]

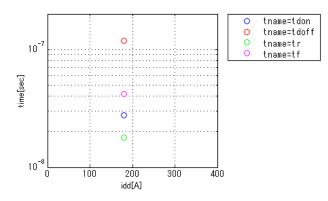
vdd = 20V, didt = 100A/us, Temp = 25degC



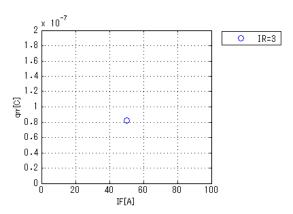
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Switchingldd[Tname]

vgg = 10V, vdd = 20V, RGG = 3.50hm



Qrrif[ir] vdd = 20V, didt = 100A/us, Temp = 25degC

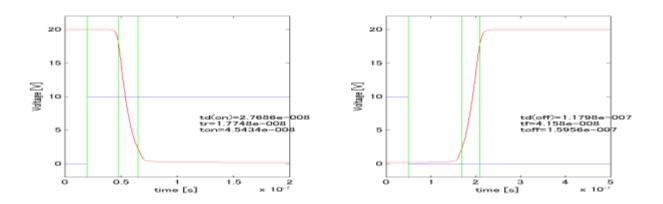




Simulation results are following. Explanatory notes — : simulated

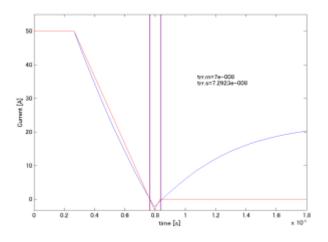
Switching Waveform (Blue : INPUT Red : OUTPUT)

vgg = 10V, vdd = 20V, RGG = 3.5ohm, idd = 180A



Trr Waveform (Red : Datasheet Blue : Simulation)

vdd = 20V, didt = 100A/us, Temp = 25degC, idd = 50A





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