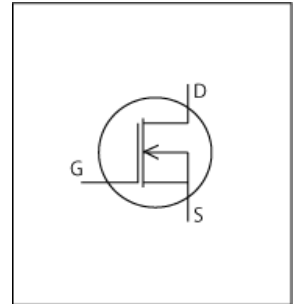


PSpice Model

NMOS

ON

NVMTS0D6N04C



Model Information

Model A macro model based on BSIM3 model
Call Name MDC_NVMTS0D6N04C_PS
Pin Assign 1:G 2:S 3:S 4:S 5:D 6:D 7:D 8:D
File List Model Library MDC_NVMTS0D6N04C_PS01.lib
 Model Report MDC_NVMTS0D6N04C_PS.pdf (this file)

Verified Simulator Version PSpice version 17.2
Note

References

The information which was used for modeling is as follow:

[Data Sheet]

- Date/Version January, 2020 Rev. 2
- Product name NVMTS0D6N04C
- Company name ON Semiconductor.
- Characteristics IdVds[Vgs], IdVgs[Temp], Rds(on)Vgs[Temp], Rds(on)Id[Vgs], Rds(on)Temp[Vgs], IdVds[temp], CapacitanceVds[Cname], VgsQg[Vdd], SwitchingRg[Tname], IsVsd[Temp], TrrIf[Ir], QrrIf[Ir], SwitchingWaveform, TrrQrrWaveform

Simulation Range

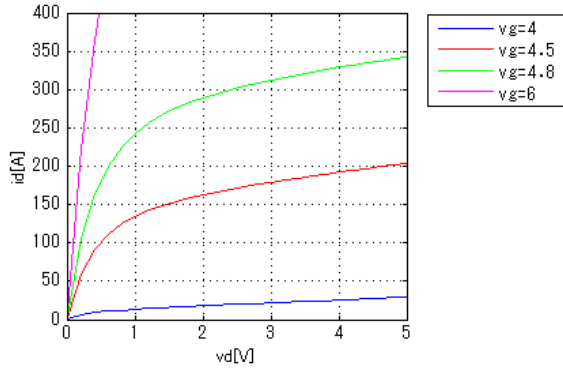
This table shows the range of evaluated simulation range that was not occurs any convergence problems in this area.

Item	Range			Unit
	Min.		Max.	
Drain-source voltage (DC)	0	to	40	V
Gate-source voltage (DC)	-20	to	20	V
Temperature	-55	to	175	deg C

Simulation results are following.
 Explanatory notes — : simulated

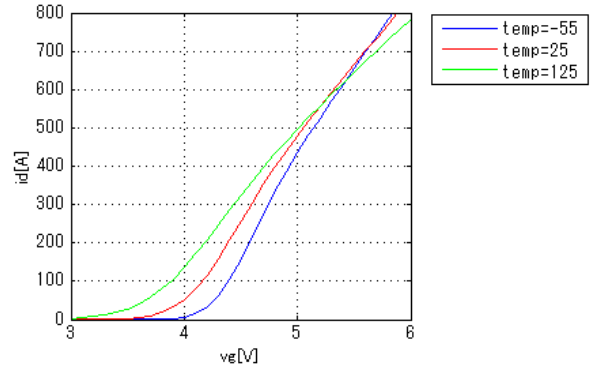
IdVds[Vgs]

Temp. = 25degC



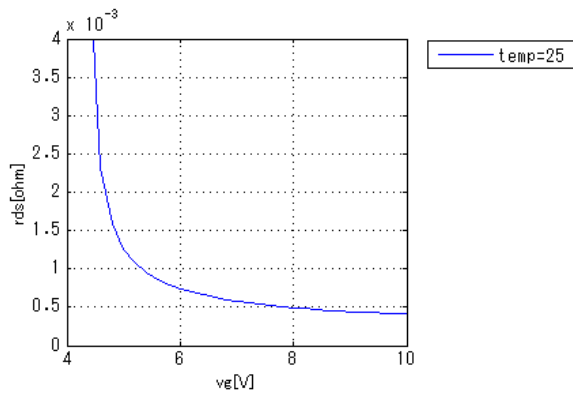
IdVgs[Temp]

$V_{ds} = 10V$

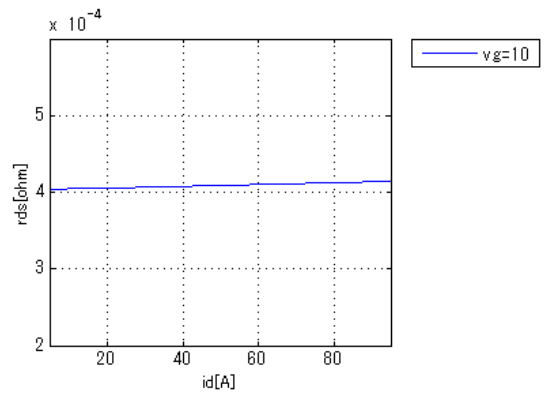


Rds(on)Vgs[Temp]

$I_d = 50A$

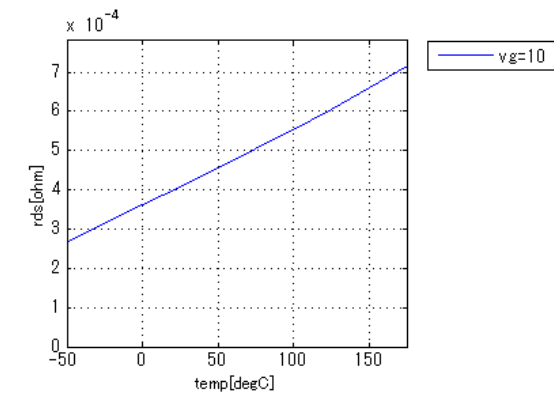


Rds(on)Id[Vgs]



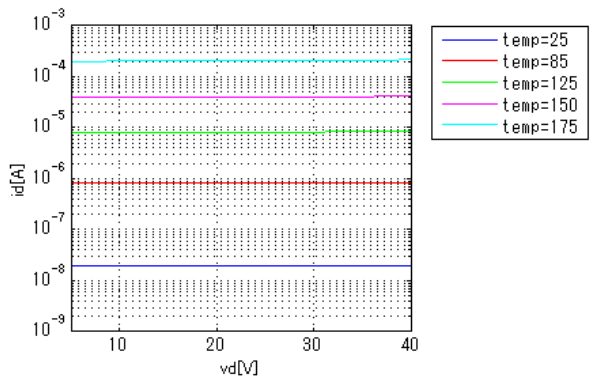
Rds(on)Temp[Vgs]

$I_d = 50A$



IdVds[temp]

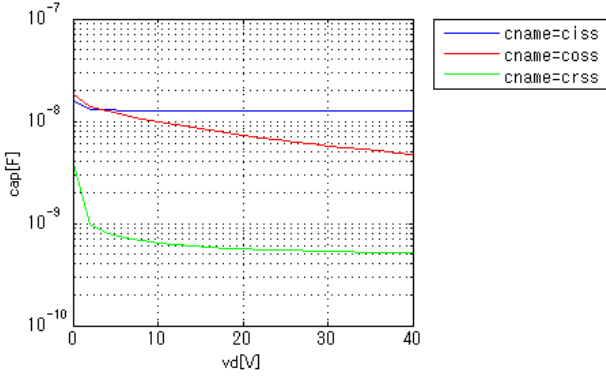
$v_g = 0V$



Simulation results are following.
 Explanatory notes — : simulated

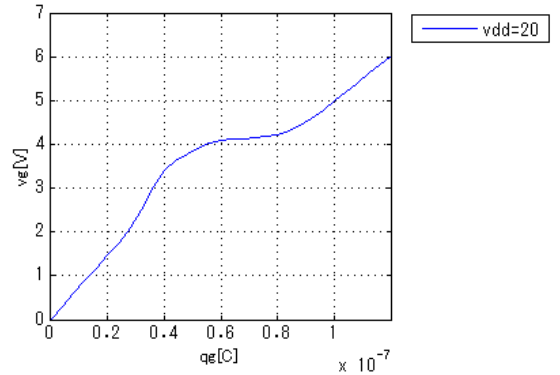
CapacitanceVds[Cname]

freq = 1000000Hz



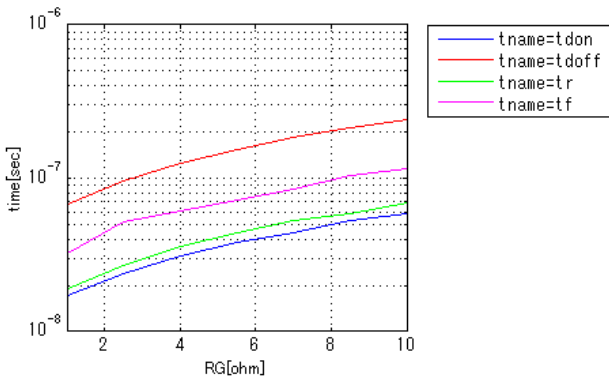
VgsQg[Vdd]

Id = 50A



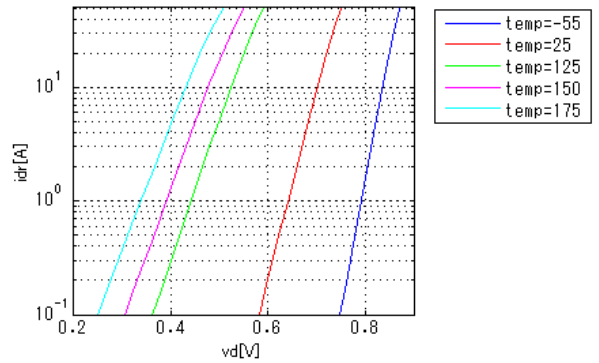
SwitchingRg[Tname]

vgg = 10V, vdd = 20V, idd = 50A



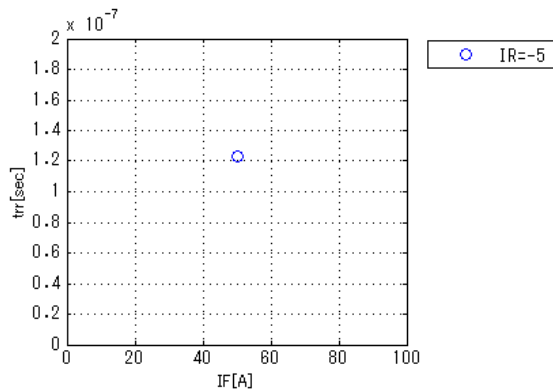
IsVsd[Temp]

vg = 0V



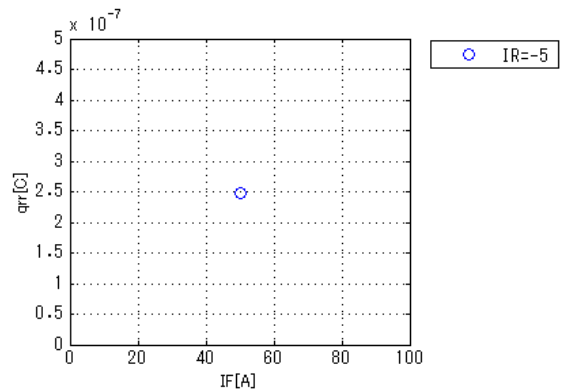
Trrlf[Ir]

vdd = 20V, didt = 100A/us



Qrrlf[Ir]

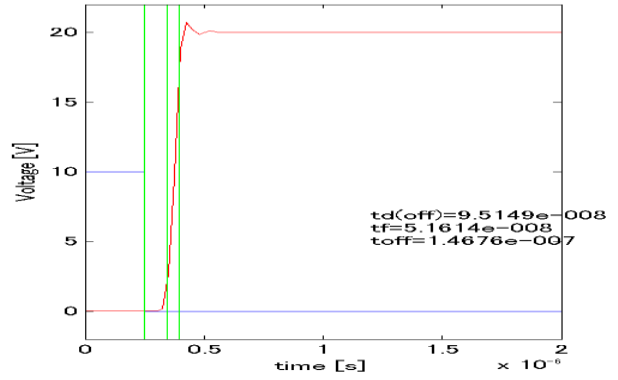
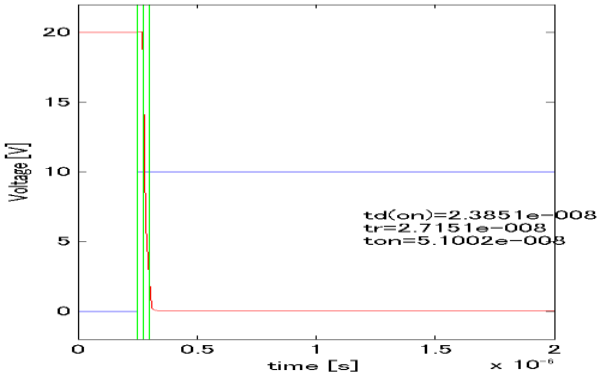
vdd = 20V, didt = 100A/us



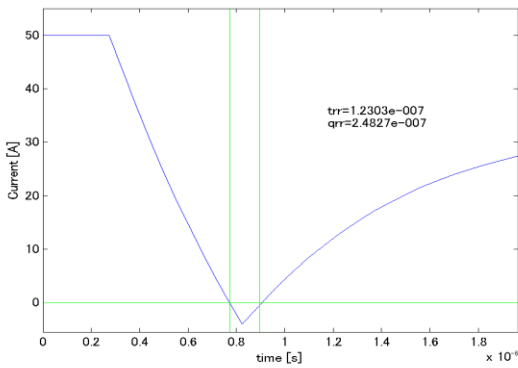
Simulation results are following.
Explanatory notes — : simulated

Switching Waveform

Blue : INPUT Red : OUTPUT



Trr Qrr Waveform



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