LTspice Model
Automotive, 500-mA LDO With Power-Good in Small Wettable Flank
TEXAS INSTRUMENTS
TPS74501PQWDRBRQ1

Model Information

Model	A macro model
Call Name	MDC_TPS74501PQWDRBRQ1_LT
Pin Assign	1:OUT 2:NC 3:FB 4:GND 5:EN 6:PG 7:NC 8:IN 9:ThermalPad
File List	Model Library MDC_TPS74501PQWDRBRQ1_LT.lib
	Model Report MDC_TPS74501PQWDRBRQ1_LT.pdf(this file)

Verified Simulator Version LTspice

Note

References

The information which was used for modeling is as follow:

[Data Sheet]

- ●Date/Version
- ●Product name TPS74501PQWDRBRQ1
- ●Company name TEXAS INSTRUMENTS

[Characteristics listed]

- ●Characteristics
  - Output Voltage vs Input Voltage
  - Start-Up With EN
  - Line regulation
  - Load regulation
  - Active output discharge
  - Low-Dropout Voltage
  - PG Delay Time
  - Current limit

Simulation Condition

This table shows the range of evaluated simulation range that was not occurs any convergence problems in this area.

Item	Condition	Unit
Temperature	25	deg C

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○ : Implemented
× : Not Implemented
— : Not applicable

Model Functions Table

	RANK=2	
Functions	**RANK**	**Implemented**
Input voltage range: 1.5 V to 6.0 V	1	○
Output voltage range: Adjustable option: 0.55 V to 5.5 V	1	○
Power-good output options: Open-drain	1	○
Output accuracy: ±0.85% (25℃)	1	○
Active output discharge	1	○
Under voltage lockout (UVLO)	1	○
Enable Operation	1	○
Ultra-low dropout: 160 mV (max) at 500 mA (3.3 VOUT)	1	○
Current limit	1	○
Line regulation	1	○
Load regulation	1	○
Line transient	2	○
Load transient	2	○

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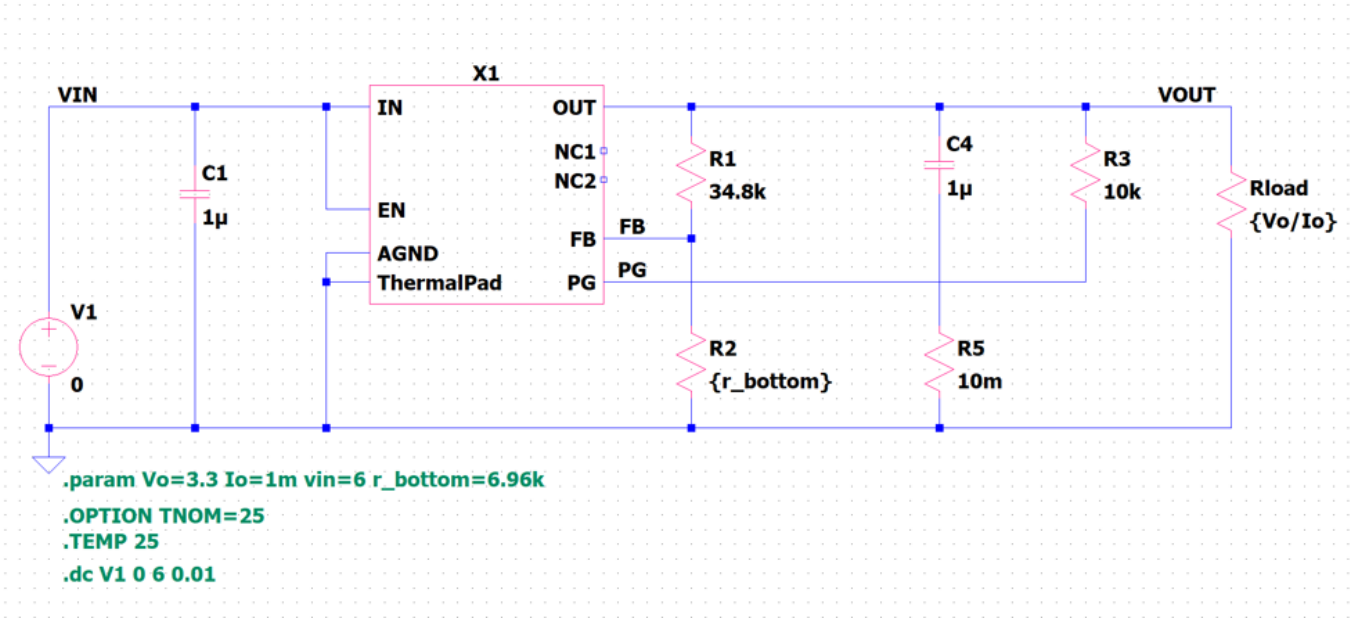
Output Voltage vs Input Voltage (Input=0V~6V Output=3.3V IOUT=1mA)

Simulation results are following.
Explanatory notes — : simulated

Testbench

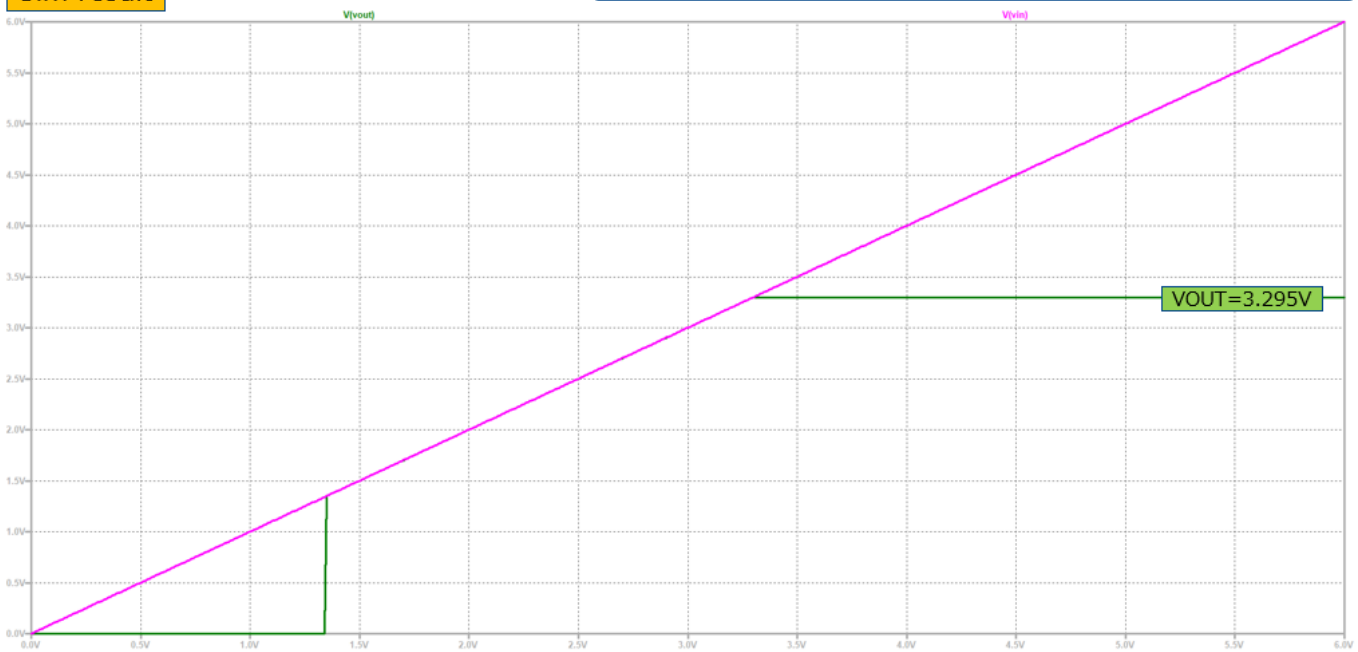


Output Voltage vs Input Voltage (Input=0V~6V Output=3.3V IOUT=1mA)

Simulation results are following.
Explanatory notes — : simulated

Sim result

The output voltage does not change even if the input voltage changes



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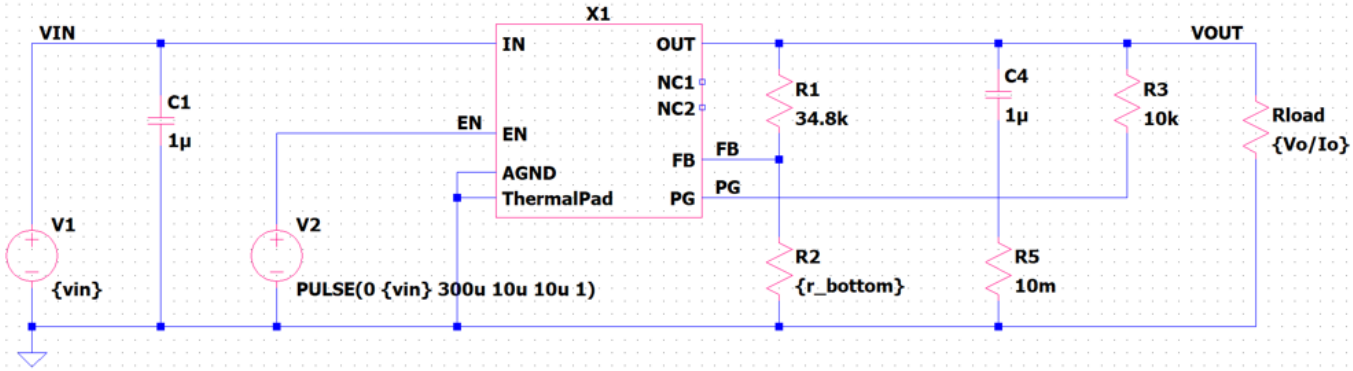
Start-Up With EN

Simulation results are following.
Explanatory notes — : simulated

Testbench



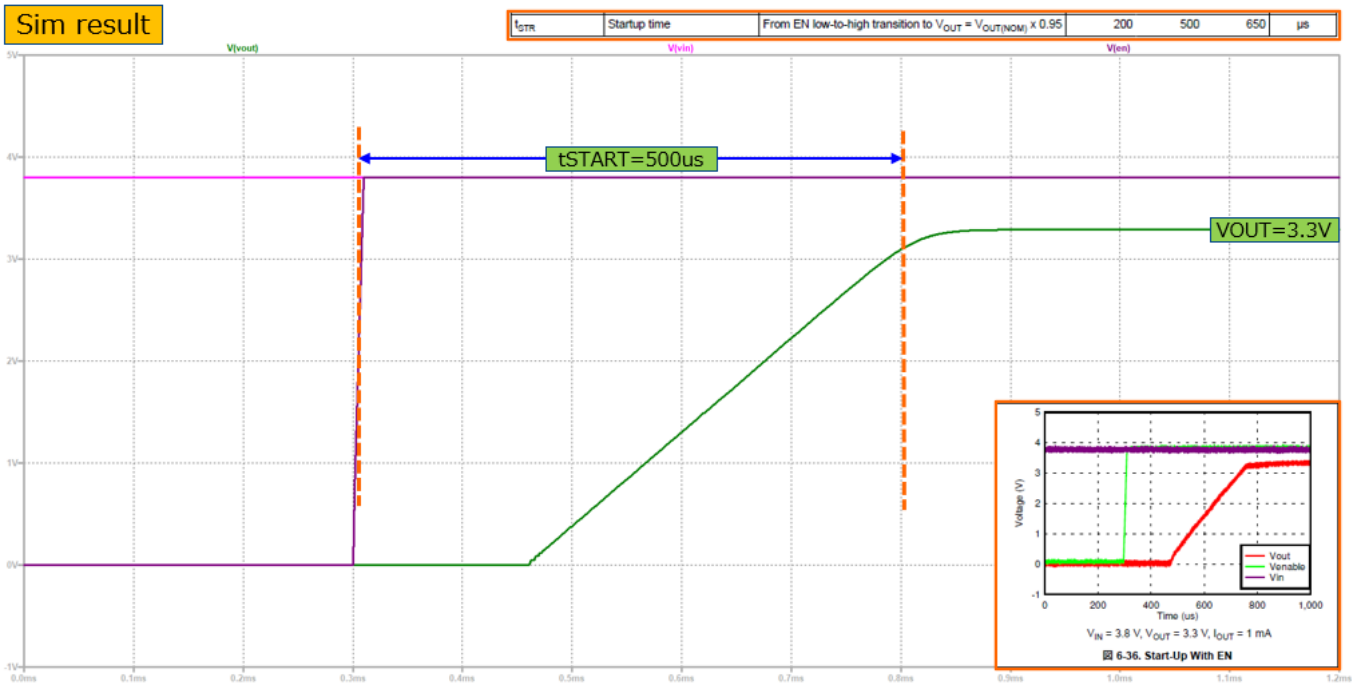

```
.param Vo=3.3 Io=1m vin=3.8 r_bottom=6.98k      .meas TRAN tSTR TRIG V(EN)=1.9 RISE=1 TARG V(VOUT)=3.292*0.95 RISE=1
.OPTION TNOM=25
.TEMP 25
.step param r_bottom list 54.9k 15.4k 6.98k 4.32k

.tran 0 1.2m 0 10n
```

Start-Up With EN

Simulation results are following.
Explanatory notes — : simulated

Sim result



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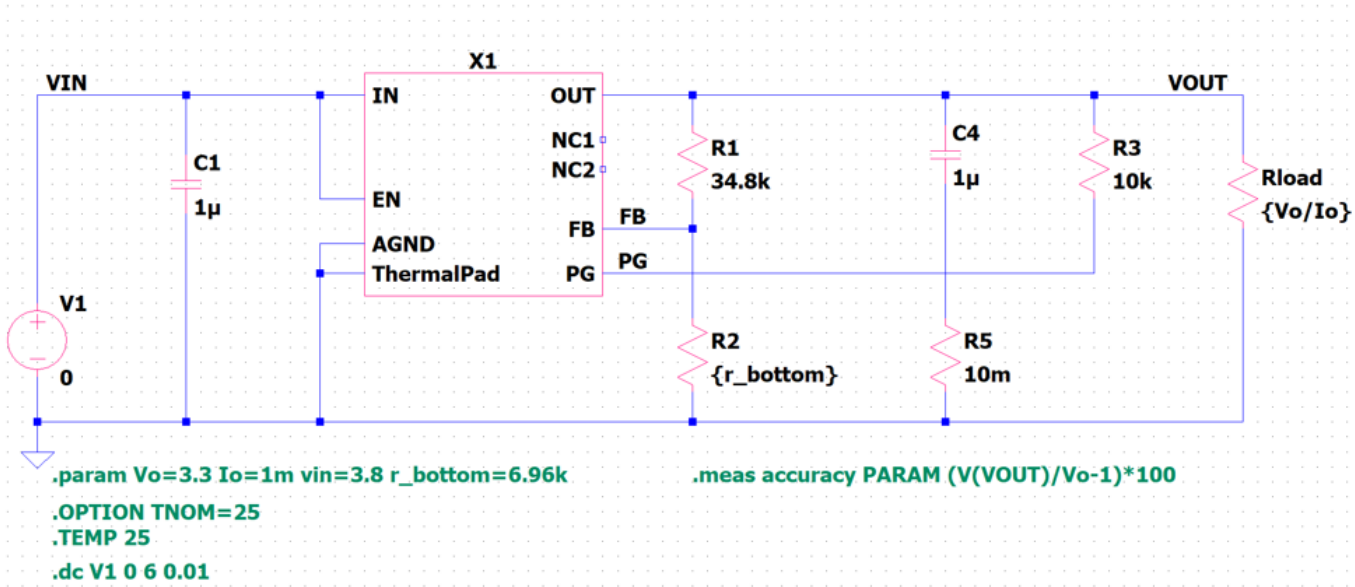
Line regulation (Input=0V~6V Output=3.3V IOUT=1mA)

Simulation results are following.
Explanatory notes — : simulated

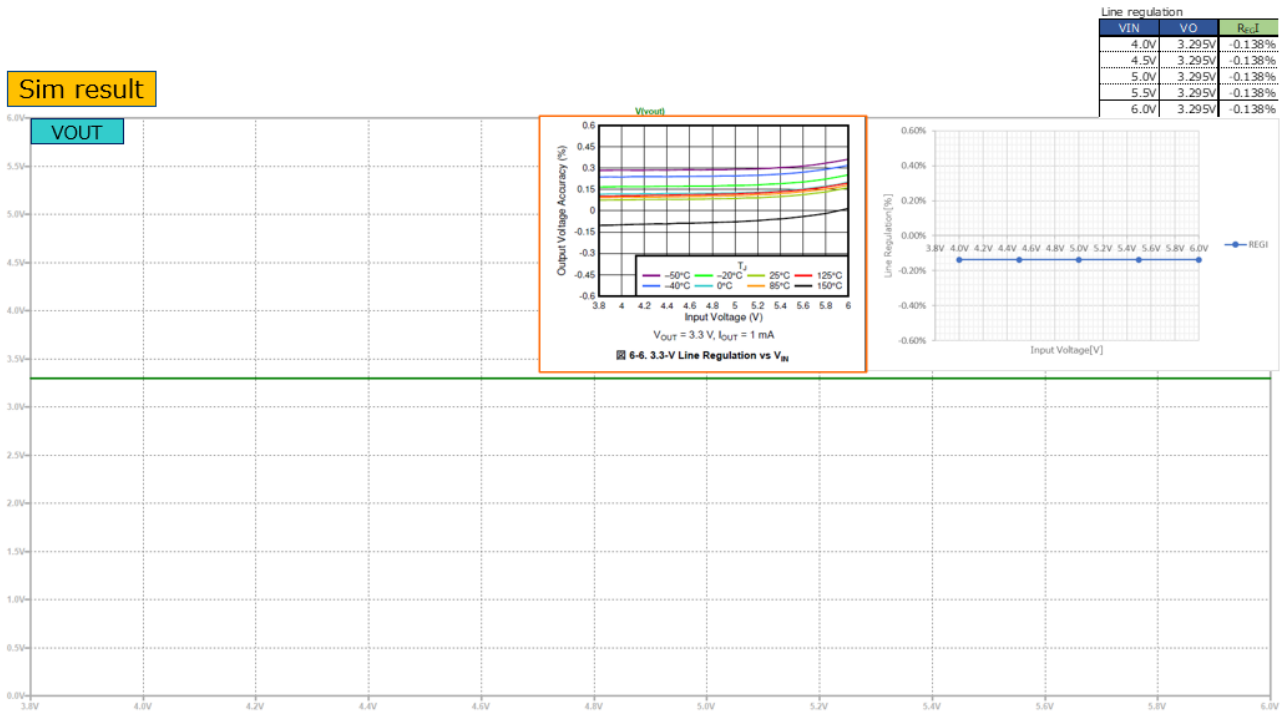
Testbench



Line regulation (Input=0V~6V Output=3.3V IOUT=1mA)

Simulation results are following.
Explanatory notes — : simulated

Sim result



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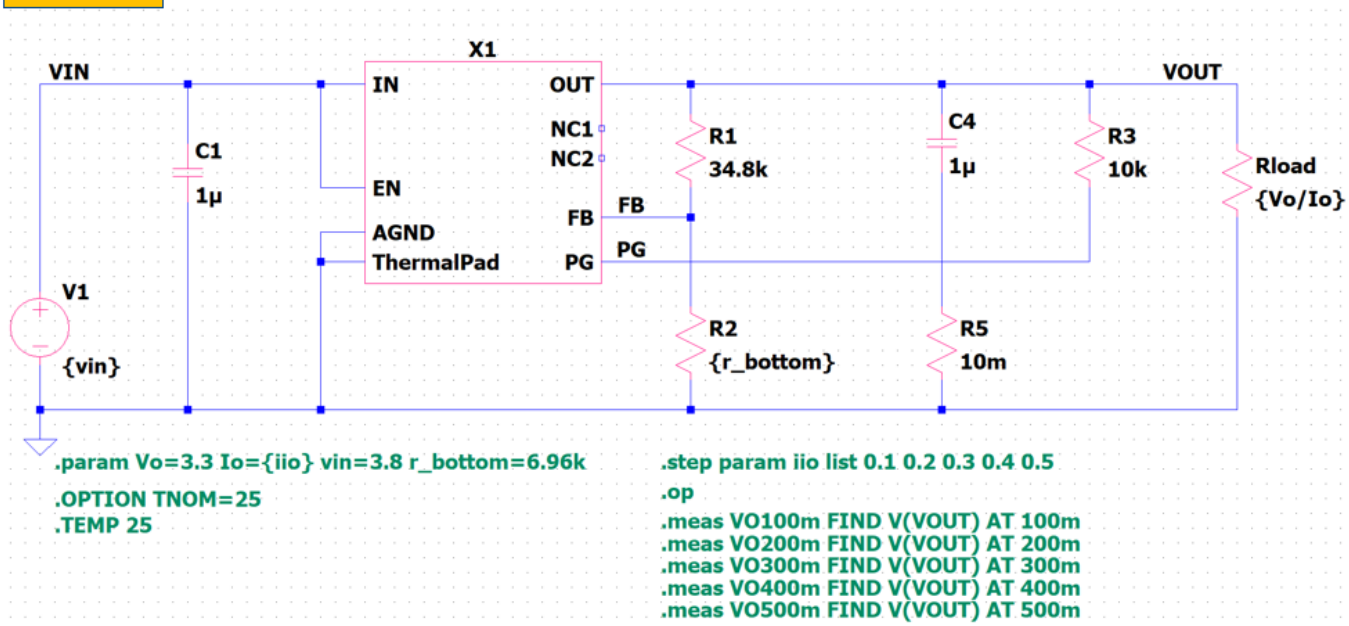
Load regulation (Input=3.8V Output=3.3V IOUT=0.1A~0.5A)

Simulation results are following.
Explanatory notes — : simulated

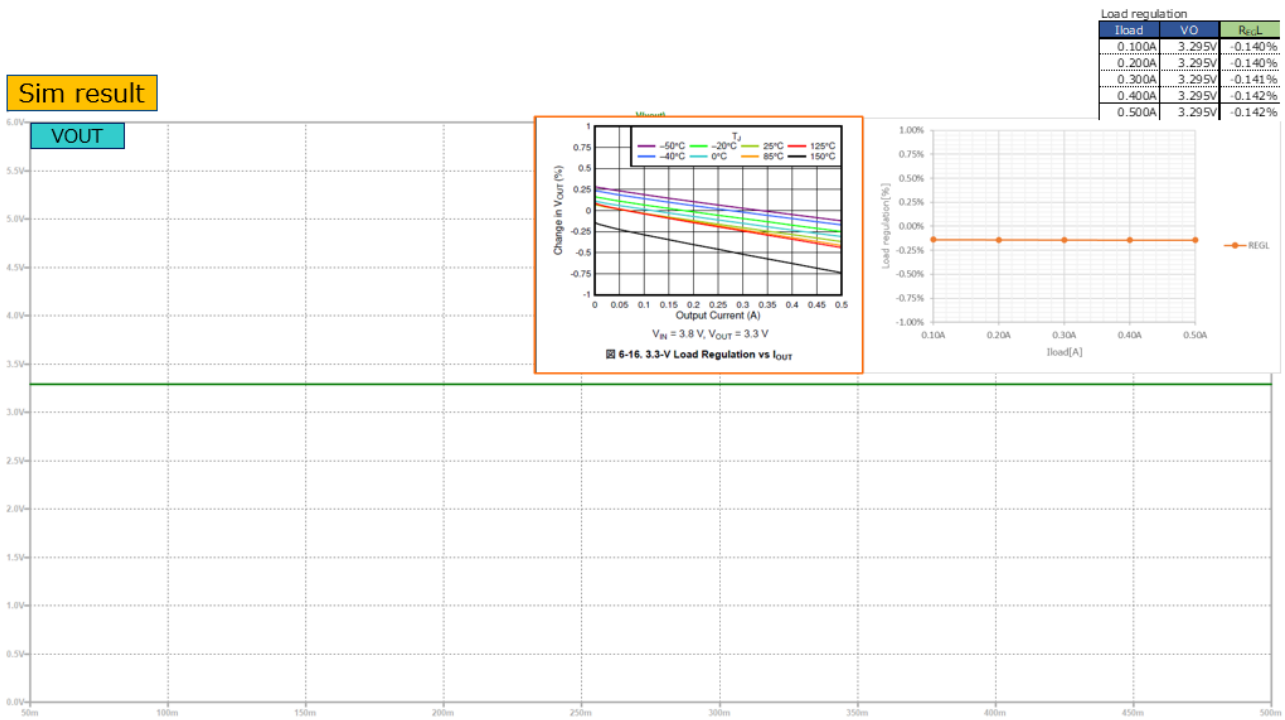
Testbench



Load regulation (Input=3.8V Output=3.3V IOUT=0.1A~0.5A)

Simulation results are following.
Explanatory notes — : simulated

Sim result



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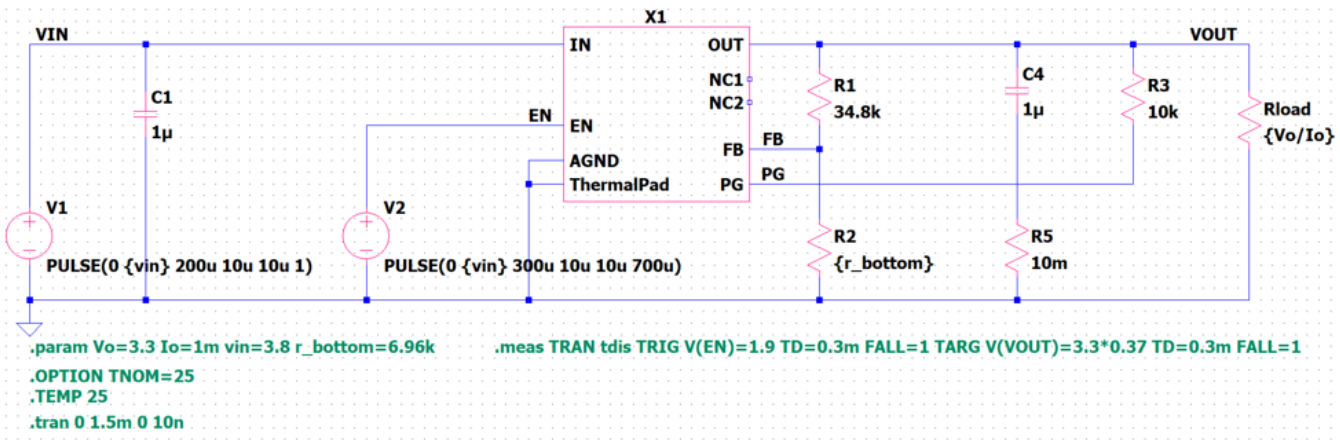
Active output discharge

Simulation results are following.
Explanatory notes — : simulated

Testbench

$\tau = (R_{PULLDOWN} \times R_L) / (R_{PULLDOWN} + R_L) \times C_{OUT}$

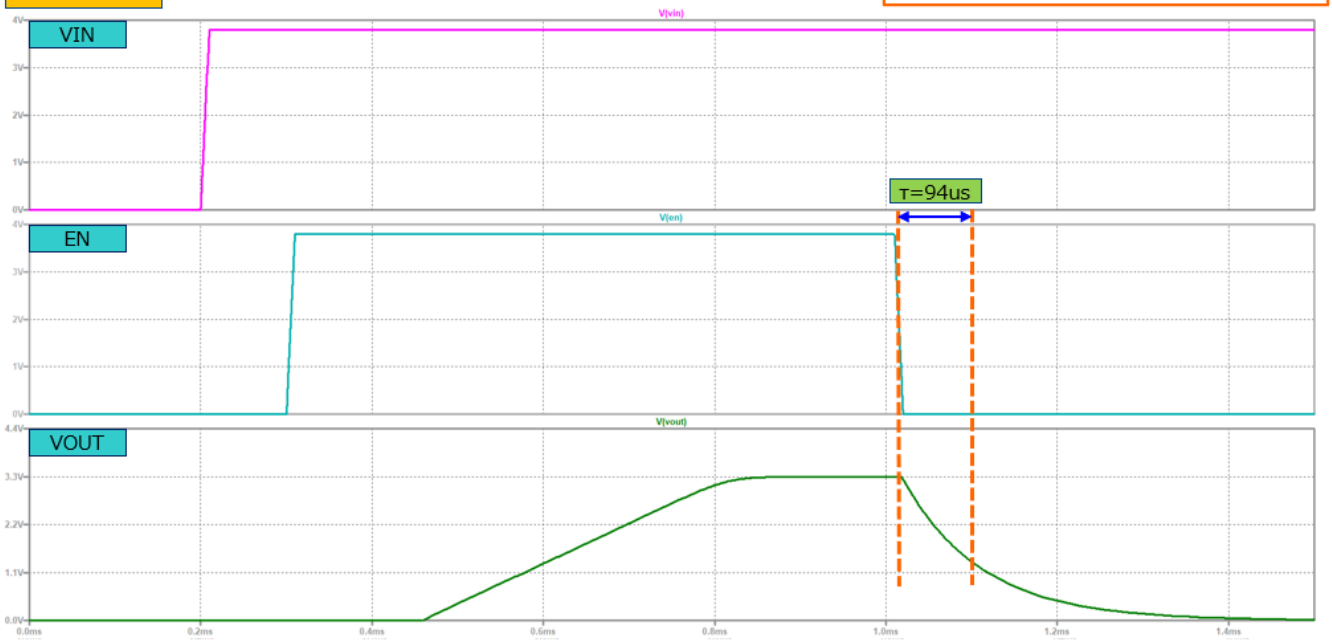


Active output discharge

Simulation results are following.
Explanatory notes — : simulated

Sim result

$\tau = (R_{PULLDOWN} \times R_L) / (R_{PULLDOWN} + R_L) \times C_{OUT}$



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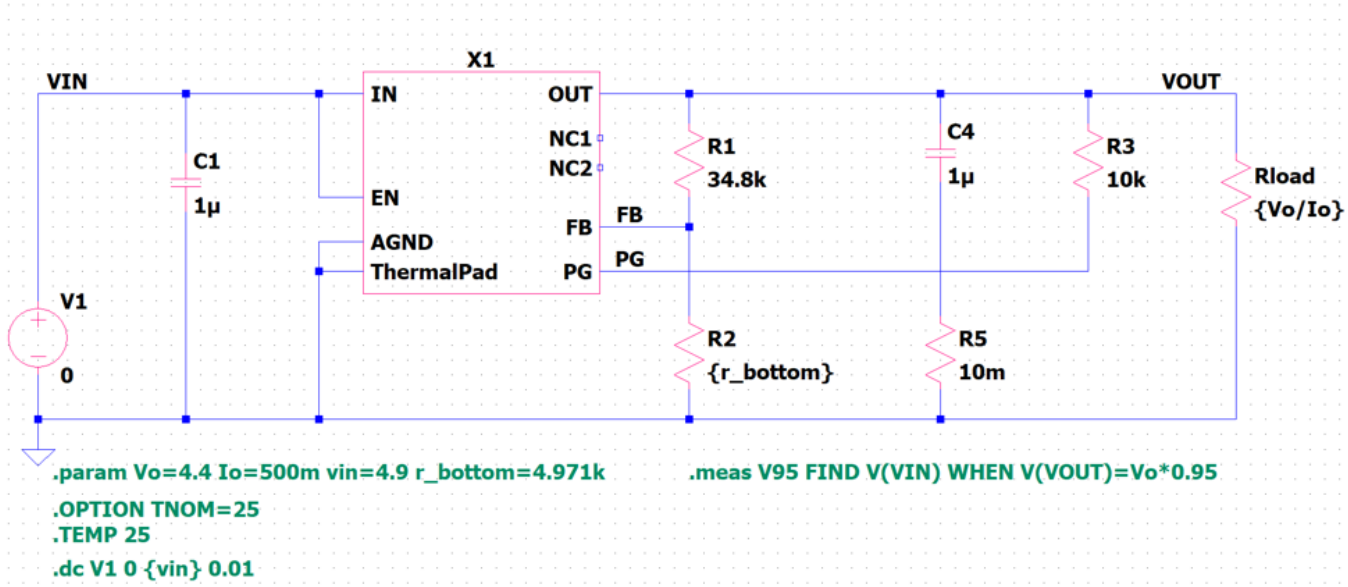
Low-Dropout Voltage (Input=0V~4.9V IOUT=0.5A)

Simulation results are following.
Explanatory notes — : simulated

Testbench

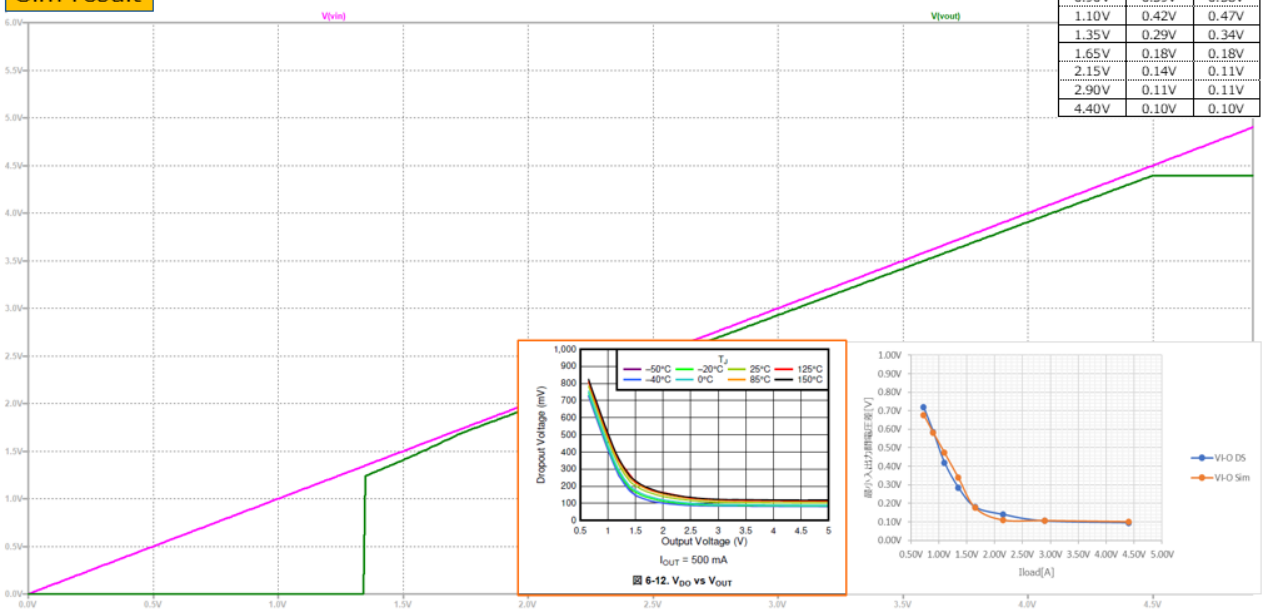


Low-Dropout Voltage (Input=0V~4.9V IOUT=0.5A)

Simulation results are following.
Explanatory notes — : simulated

Sim result

Out Vol	V_{I-O}	
	DS	Sim
0.73V	0.72V	0.68V
0.90V	0.59V	0.58V
1.10V	0.42V	0.47V
1.35V	0.29V	0.34V
1.65V	0.18V	0.18V
2.15V	0.14V	0.11V
2.90V	0.11V	0.11V
4.40V	0.10V	0.10V



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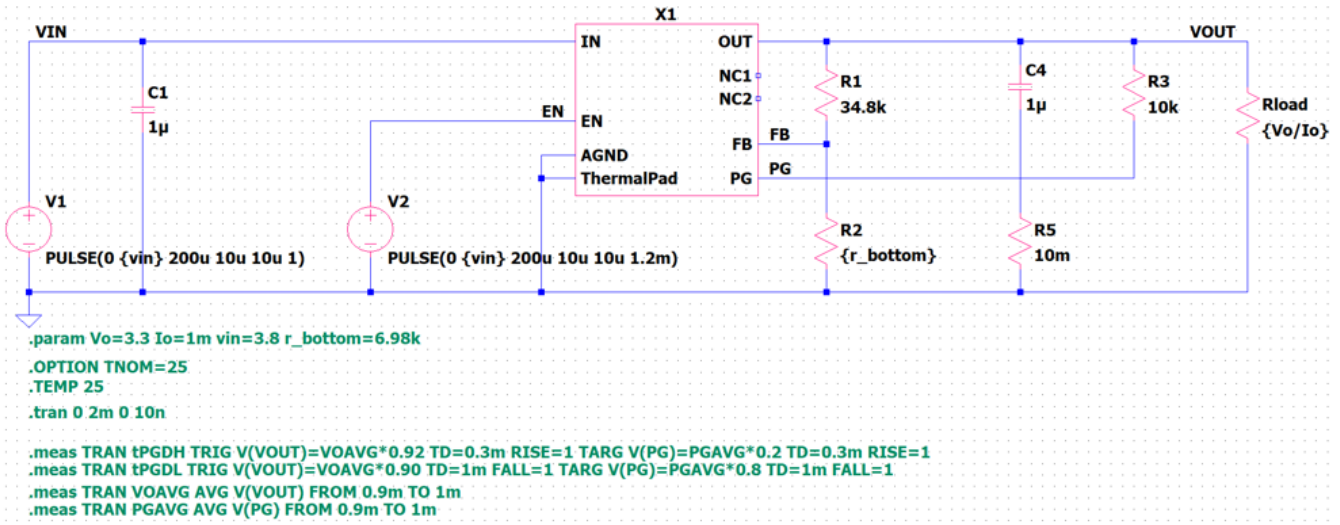
PG Delay Time

Simulation results are following.
Explanatory notes — : simulated

Parameter			MIN	TYP	MAX	UNIT
t_{PGDH}	PG delay time rising, time from 92% V_{OUT} to 20% of PG[1]		135	165	178	µs
		'B' version[2]	4.5	5	5.5	ms
t_{PGDL}	PG delay time falling, time from 90% V_{OUT} to 80% of PG[1]		1.5	7	10	µs

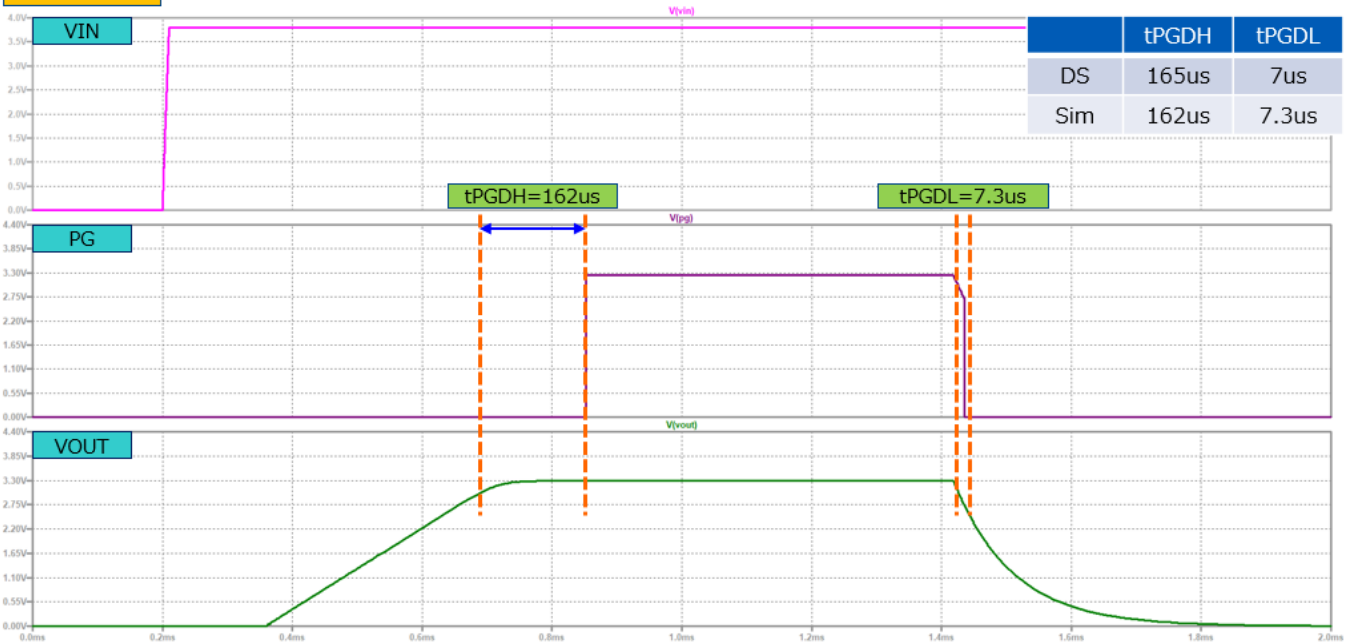
Testbench



PG Delay Time

Simulation results are following.
Explanatory notes — : simulated

Sim result



	tPGDH	tPGDL
DS	165us	7us
Sim	162us	7.3us

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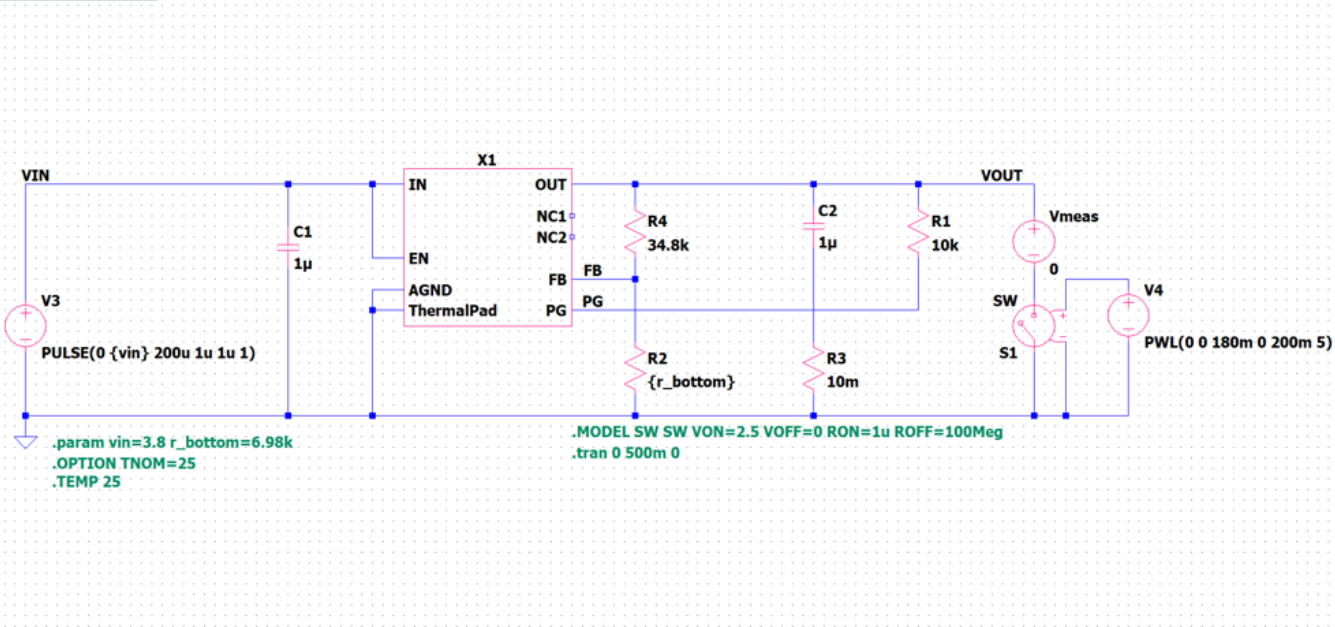
Current limit

Simulation results are following.
Explanatory notes — : simulated

Testbench



Current limit

Simulation results are following.
Explanatory notes — : simulated

Sim result

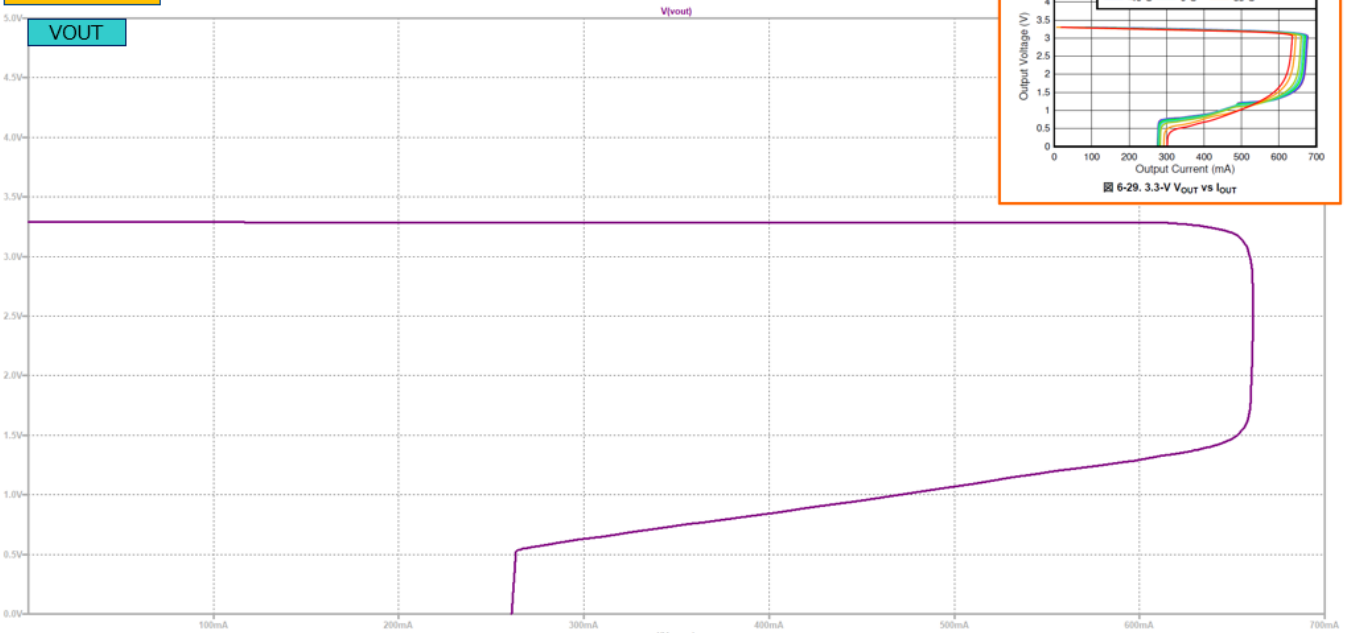


図 6-29. 3.3-V V_{OUT} vs I_{OUT}

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