LTspice Model
LDO
STMicroelectronics
L78L05ABUTR

Model Information

Model A macro model
Call Name MDC_L78L05ABUTR_LT
Pin Assign 1:VOUT 2:GND 3:VIN
File List Model Library MDC_L78L05ABUTR_LT01.lib
Model Report MDC_L78L05ABUTR_LT.pdf(this file)

Verified Simulator Version LTspiceXVII

Note

References
The information which was used for modeling is as follow:

[Data Sheet]
- ●Date/Version Rev.24
- ●Product name L78L05ABUTR
- ●Company name STMicroelectronics

[Characteristics listed]
- ●Characteristics VIN-VOUT,Vdrop,Ilimit
  Line-Reg,Road-Reg
  Ripple Rejection

Simulation Condition
This table shows the range of evaluated simulation range that was not occurs any convergence problems in this area.

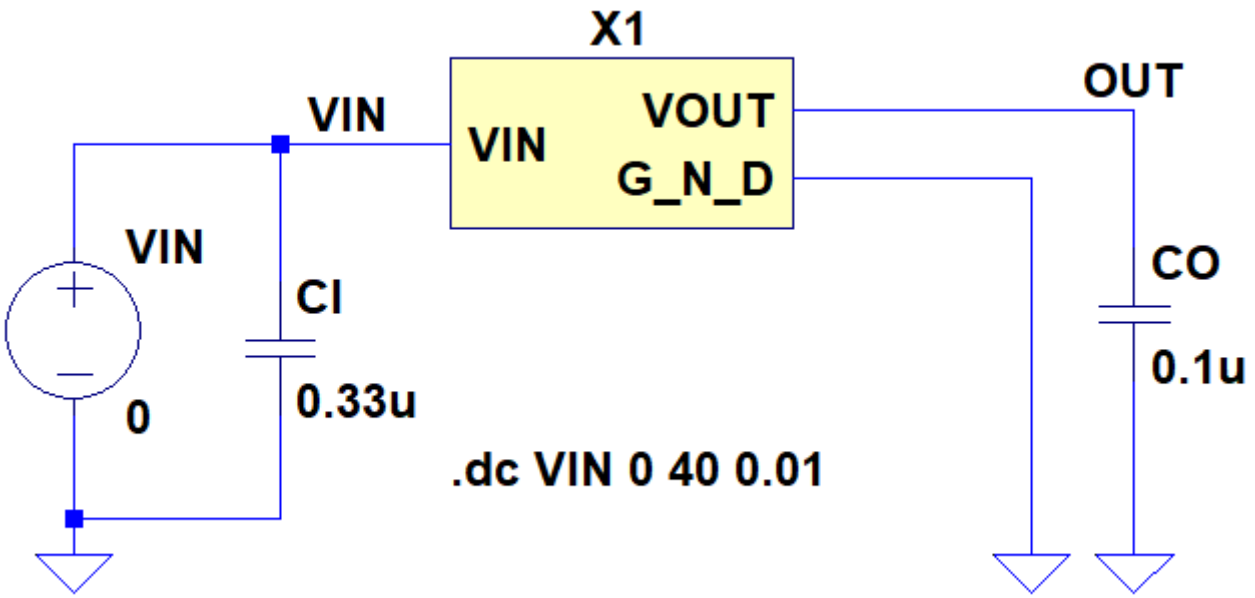
Item	Condition	Unit
Temperature	25	deg C

Model Functions Table

Functions	Implemented
VIN-VOUT	○
Vdrop	○
Ilimit	○
Line-Reglation	○
Load-Reglation	○
Ripple Rejection	○

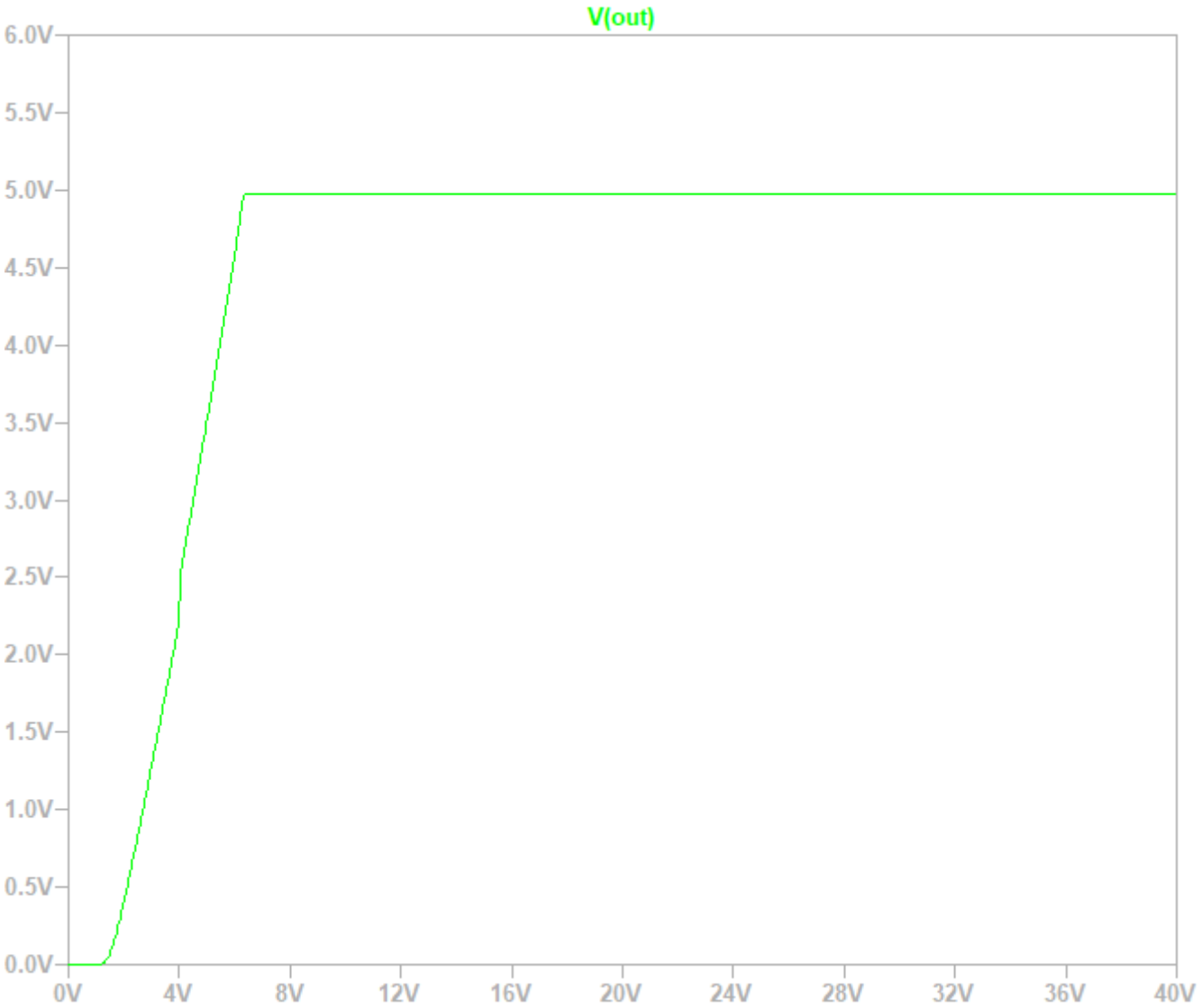
VIN-VOUT Testbench

Referred to Data Sheet



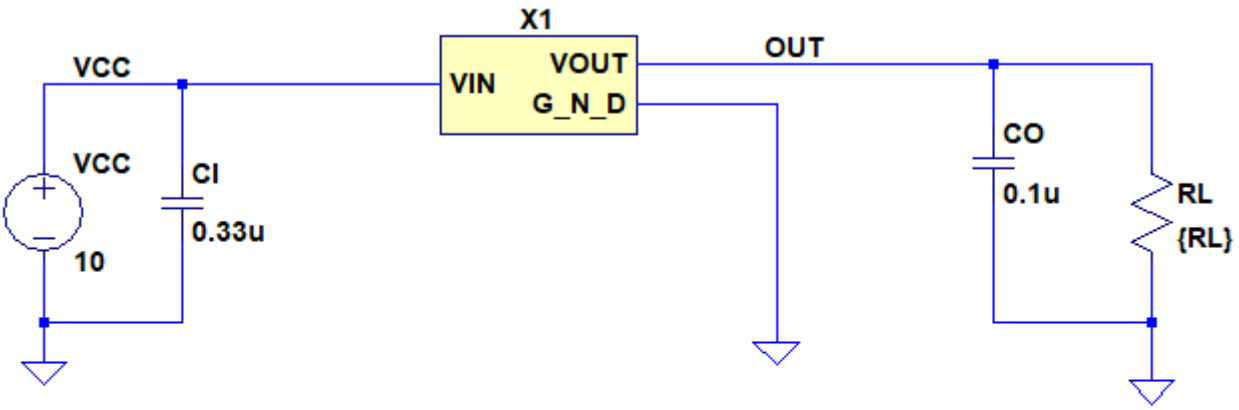
Simulation results are following.
Explanatory notes — : simulated

VIN-VOUT



Vdrop Testbench

Referred to Data Sheet



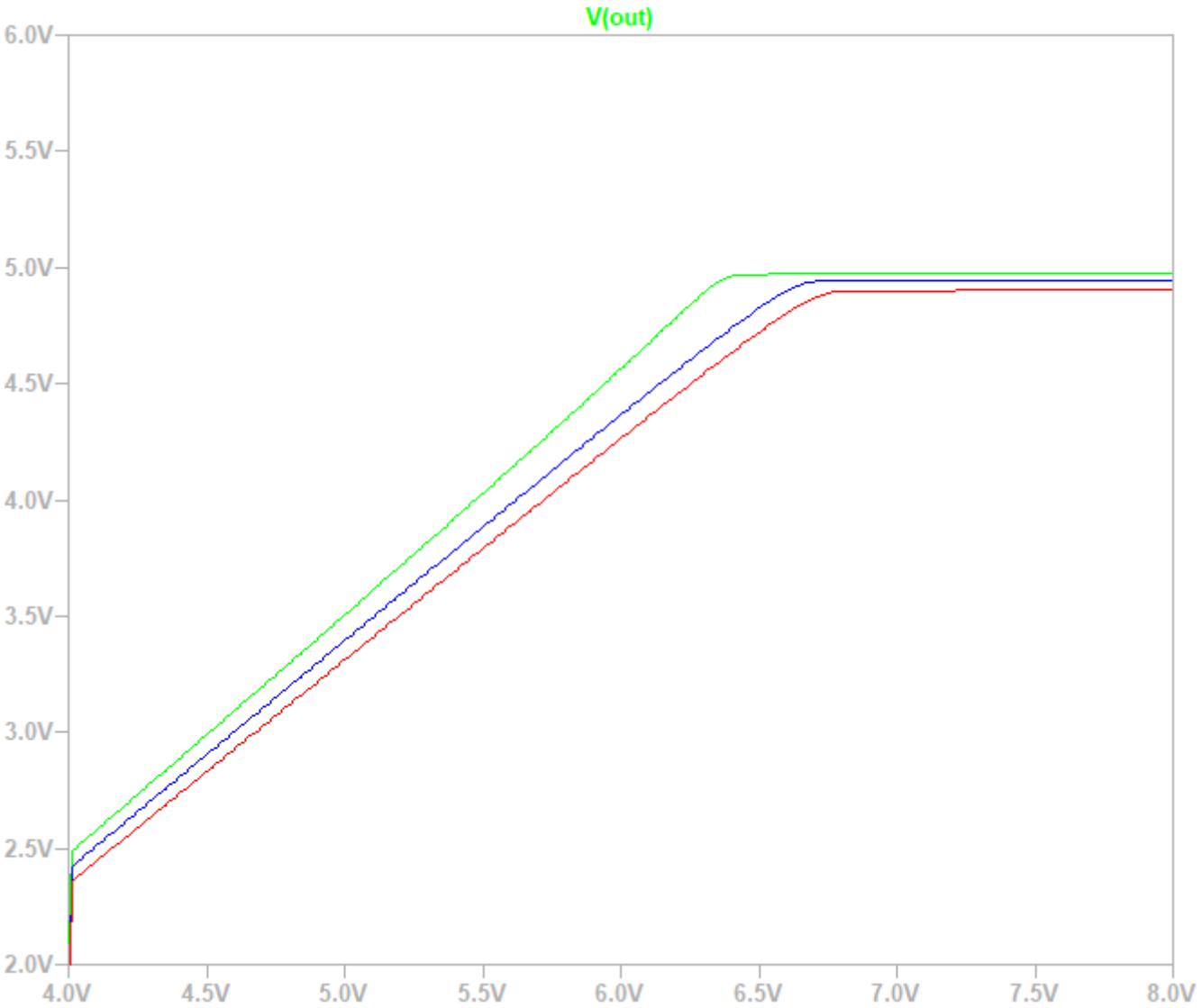
.param RL=VOUT/IOUT VOUT=5 IOUT=40m

.step param IOUT list 1m 40m 100m

.dc VCC 4 8 0.01

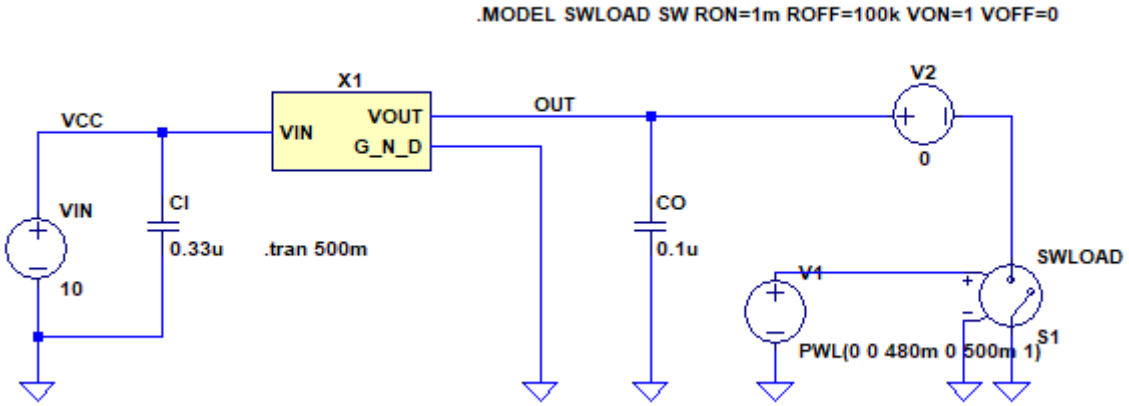
Simulation results are following.
Explanatory notes — : simulated

Vdrop



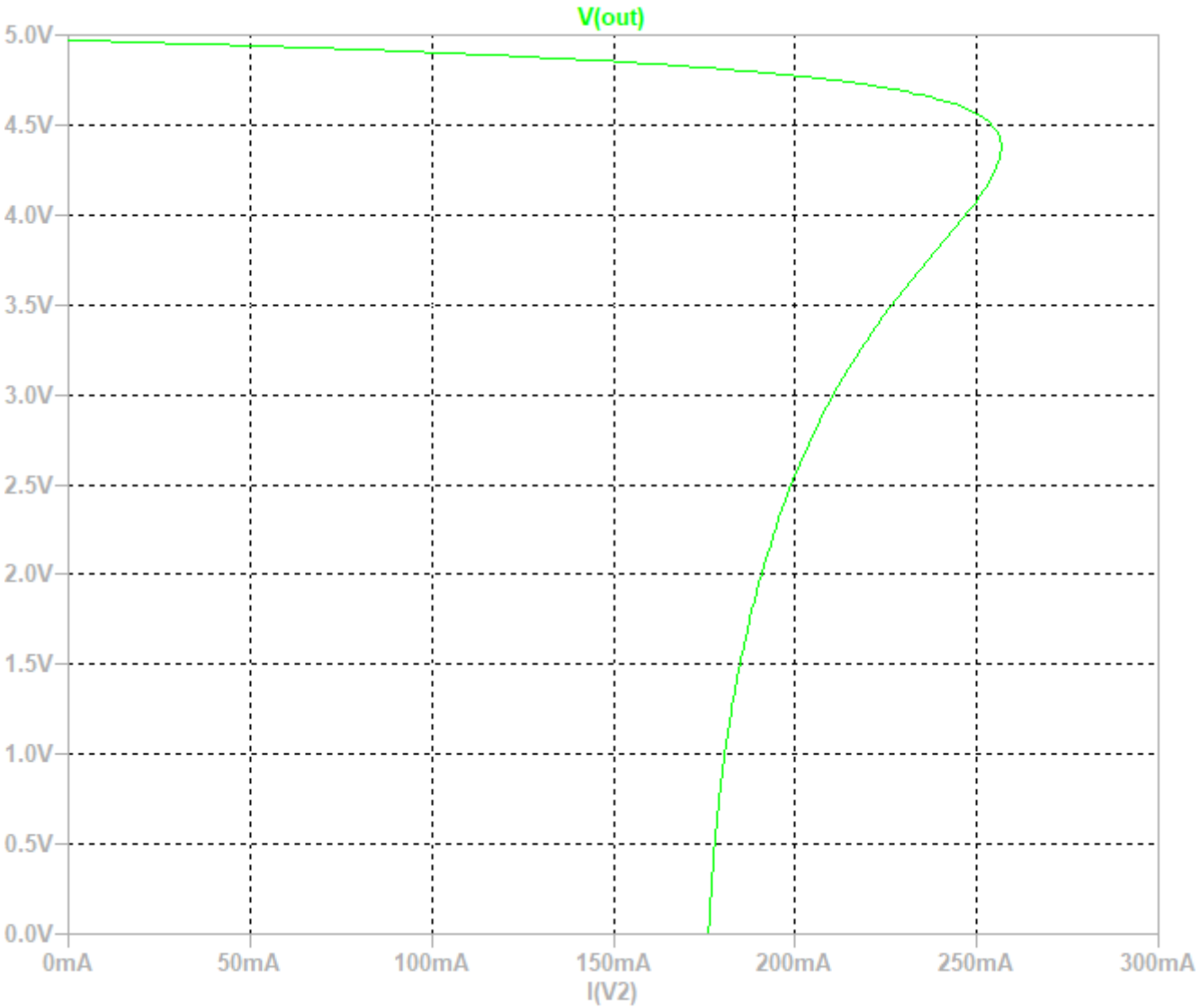
Ilimit Testbench

Referred to Data Sheet



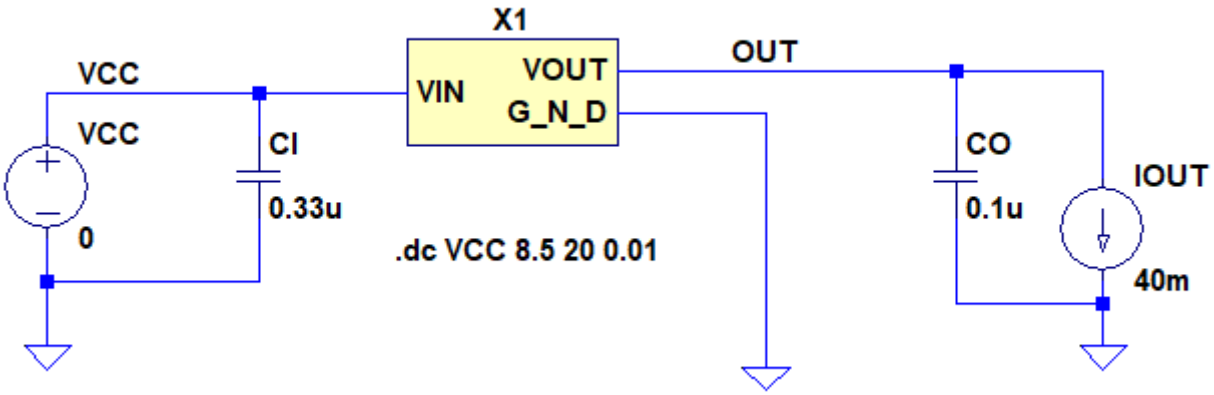
Simulation results are following.
Explanatory notes — : simulated

Ilimit



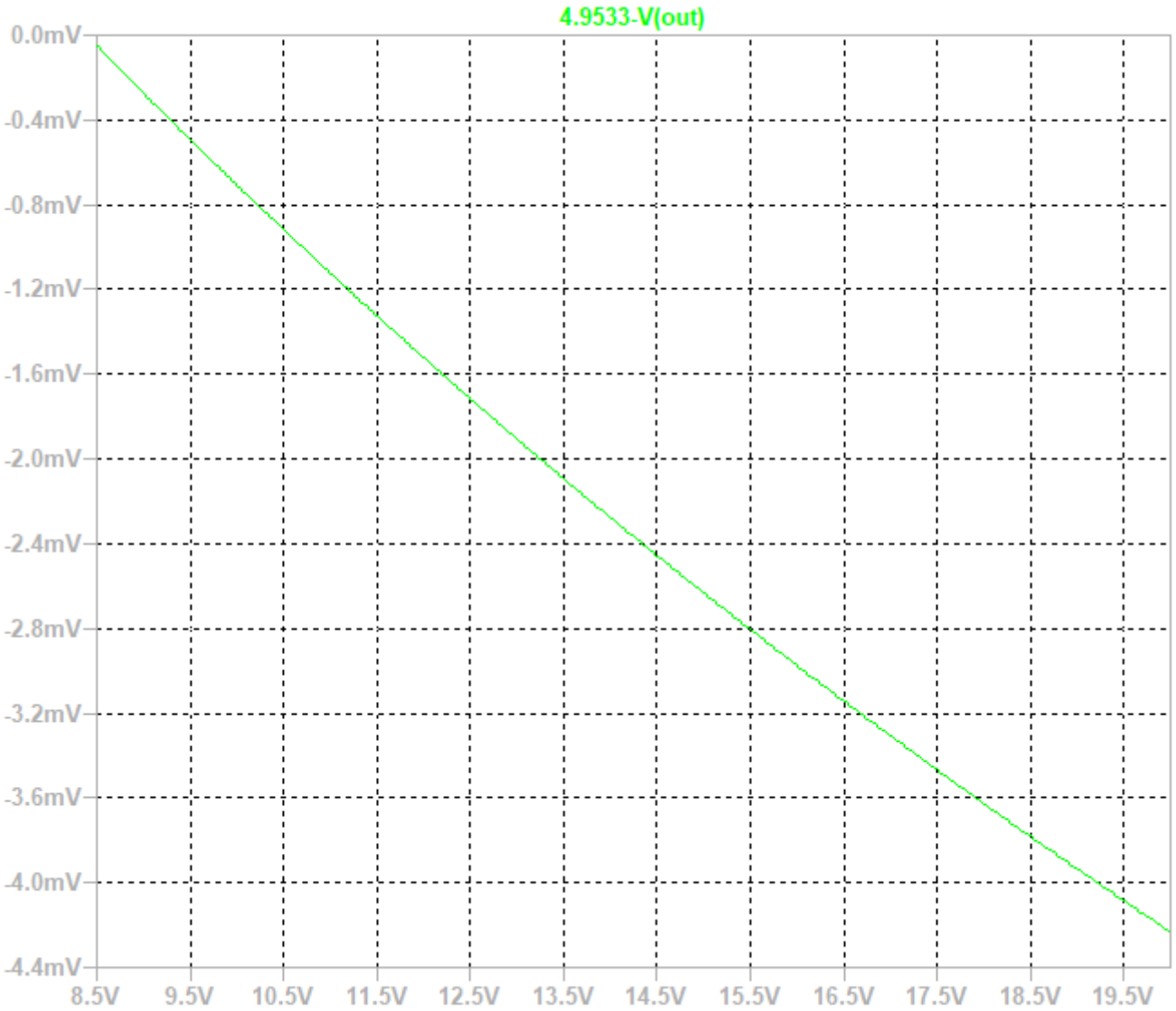
Line-Reg Testbench

Referred to Data Sheet



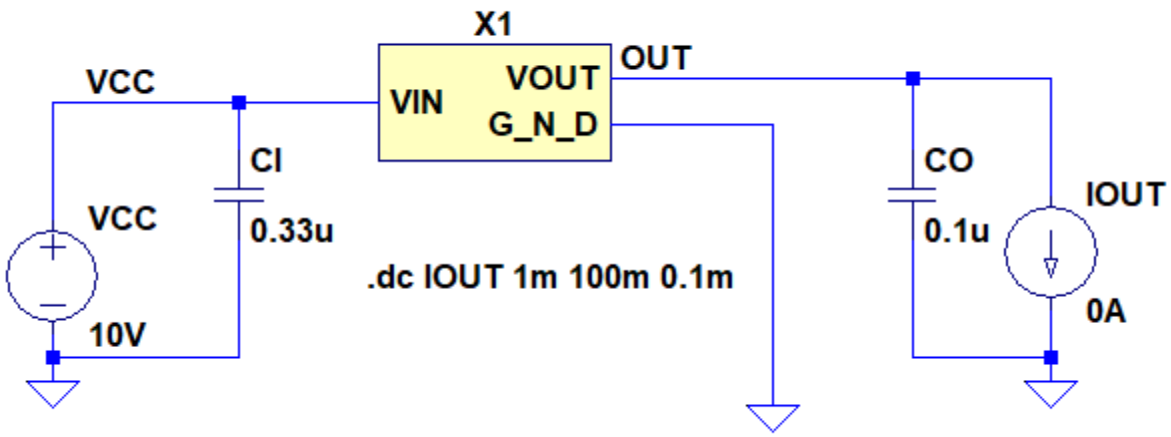
Simulation results are following.
Explanatory notes — : simulated

Line-Reg



Load-Reg Testbench

Referred to Data Sheet

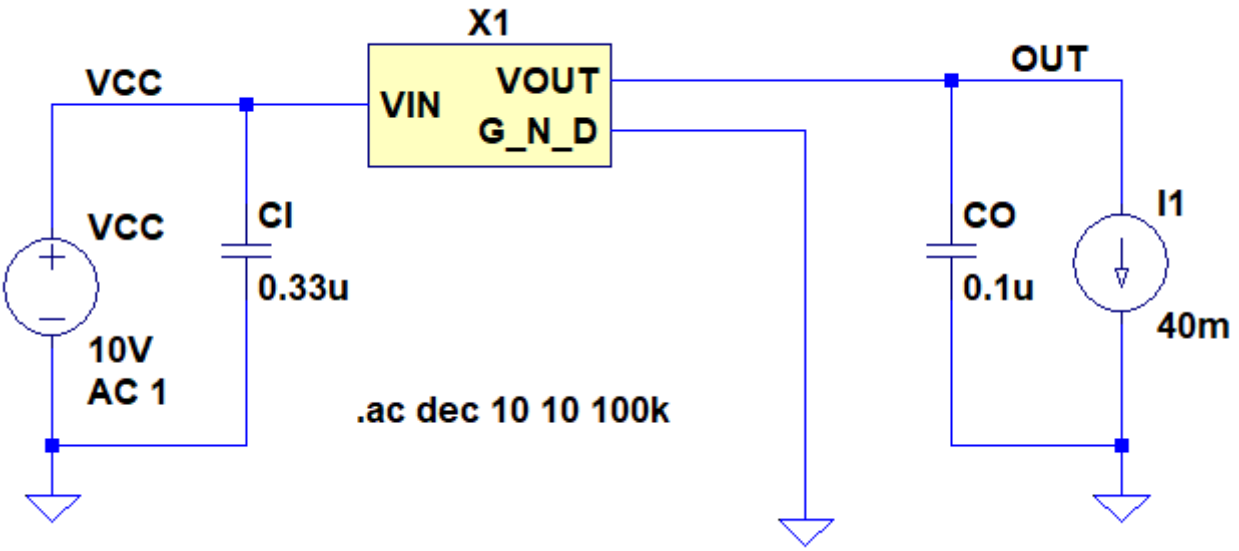


Simulation results are following.
Explanatory notes — : simulated

Load-Reg

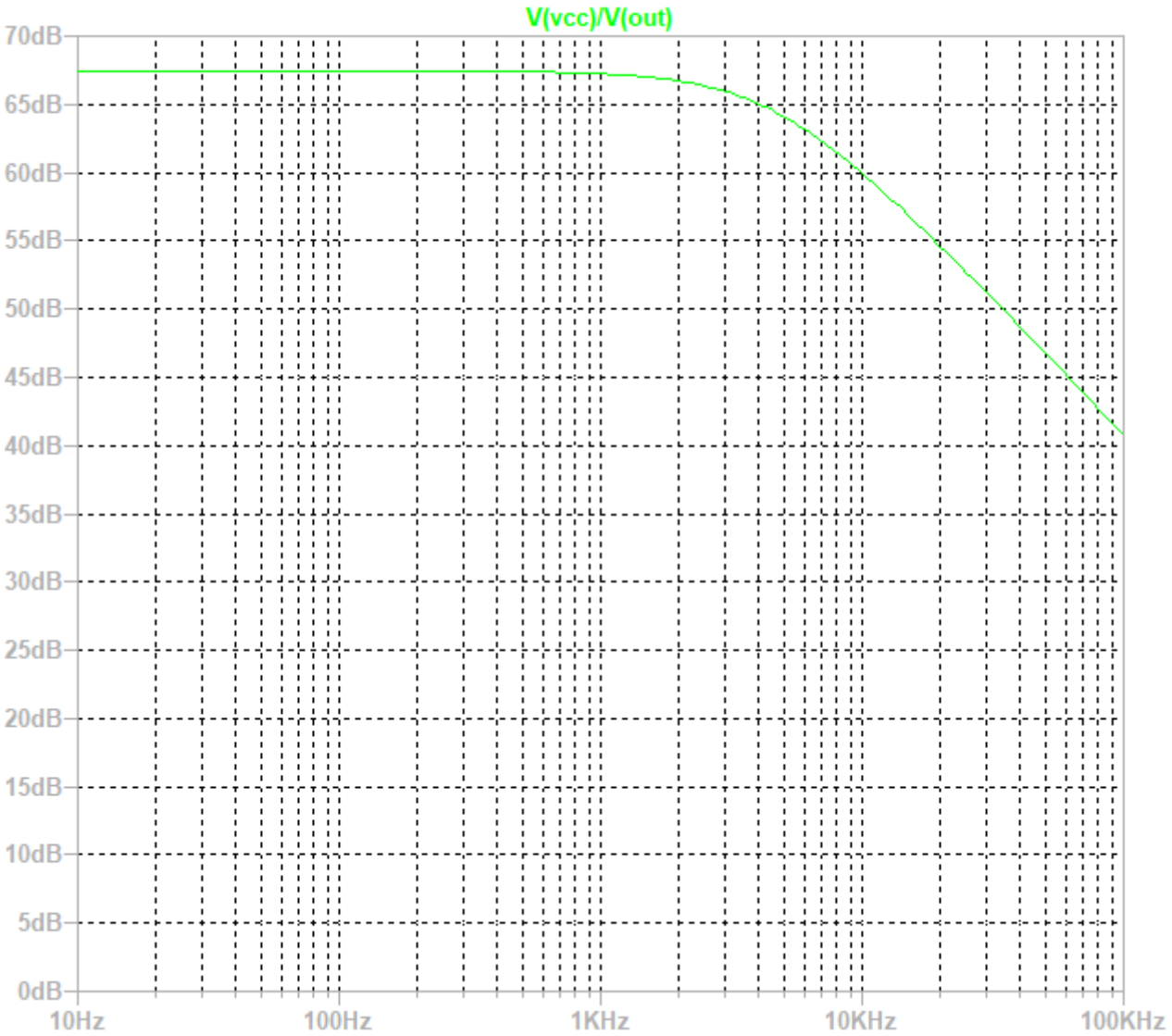
Ripple Rejection Testbench

Referred to Data Sheet



Simulation results are following.
Explanatory notes — : simulated

Ripple Rejection



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