LTspice Model
Photocoupler
LITE-ON Technology Corporation.
LTV-356T-TP1-B

Model Information

Model A macro model
Call Name MDC_LTV-356T-TP1-B_LT
Pin Assign 1:Anode 2:Cathode 3:Emitter 4:Collector
File List Model Library MDC_LTV-356T-TP1-B_LT.lib
Model Report MDC_LTV-356T-TP1-B_LT.pdf(this file)

Verified Simulator Version

Note

References

The information which was used for modeling is as follow:

[Data Sheet]

●Date/Version 10/27/2016 / RNC-OD-FC002/A4
●Product name LTV-356T
●Company name LITE-ON Technology Corporation.

[Characteristics listed]

●Characteristics

VCE(sat)-IF
IF-VF
CTR-IF
IC-VCE
Response Time-Load Resistance

Simulation Condition

This table shows the range of evaluated simulation range that was not occurs any convergence problems in this area.

Item	Condition	Unit
Temperature	25	deg C

○ : Implemented
× : Not Implemented
— : Not applicable

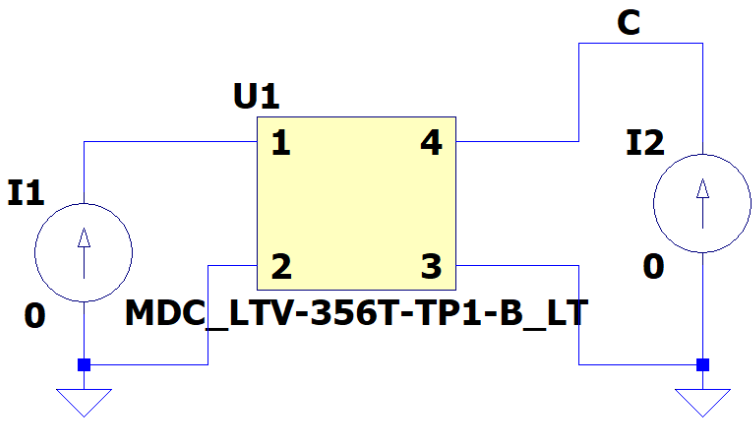
Model Functions Table

	RANK=1	
Functions	RANK	Implemented
IF-VF-Temp	1	○
Iout-Vout-IF	1	○
Iout-IF	1	—
Iout/IF-IF(CTR-IF)	1	○
CJ-VR	1	—
Propagation delay	1	○
Switching（Typ.）	1	○

VCE(sat)-IF Testbench

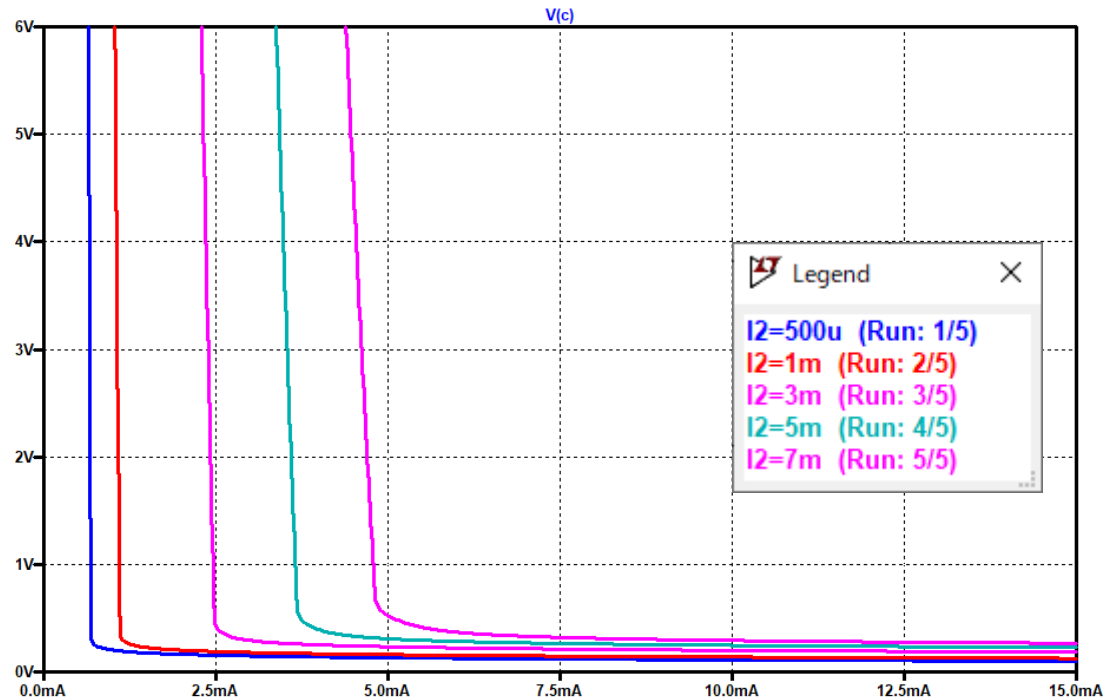
Referred to Data Sheet

```
.OPTION TNOM=25
.TEMP=25
.dc I1 0 15m 0.01m I2 list 0.5m 1m 3m 5m 7m
```



Simulation results are following.
Explanatory notes — : simulated

VCE(sat)-IF

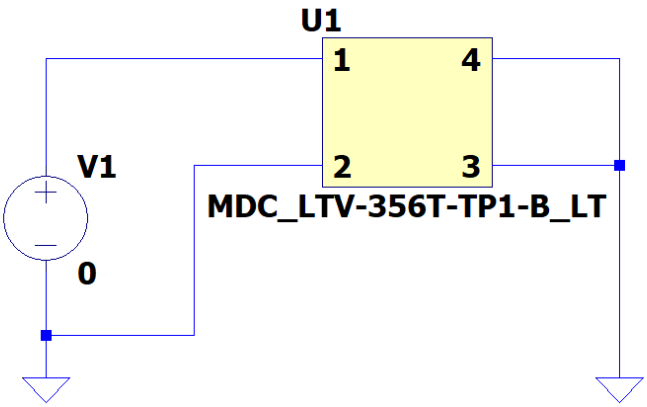


IF-VF Testbench

Referred to Data Sheet

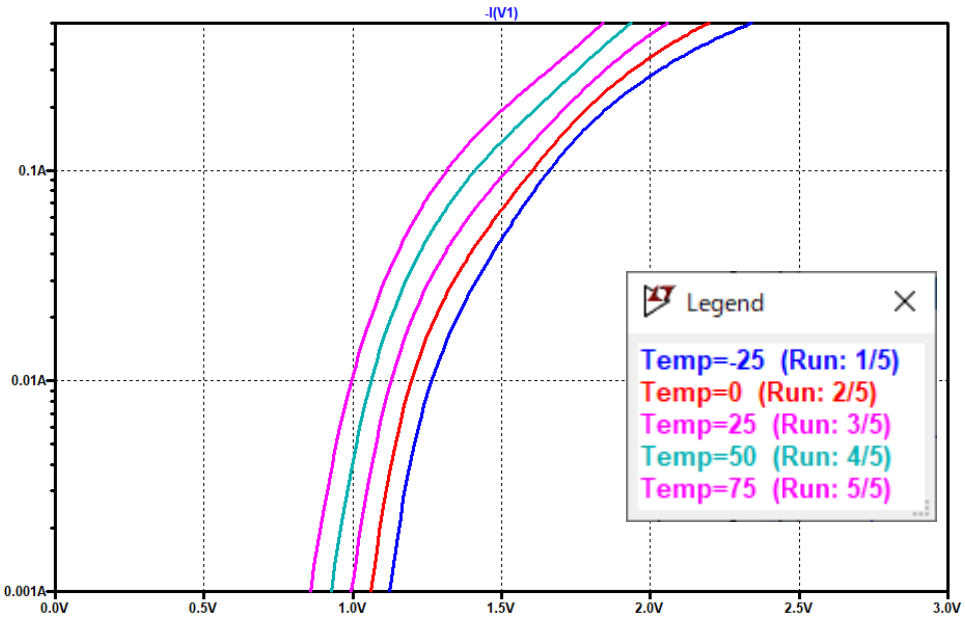
```
.OPTION TNOM=25
.TEMP -25 0 25 50 75

.dc V1 0 3 0.01
```



Simulation results are following.
Explanatory notes — : simulated

IF-VF

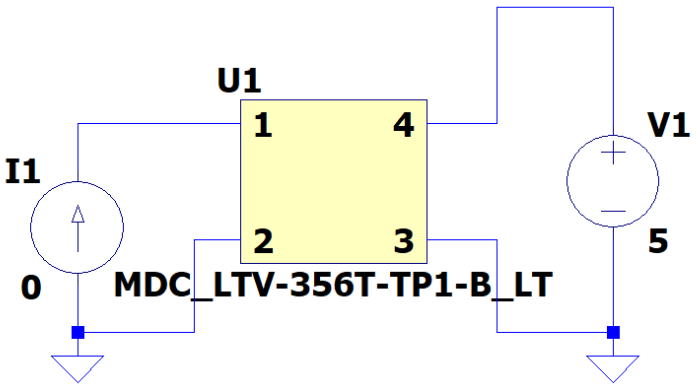


CTR-IF Testbench

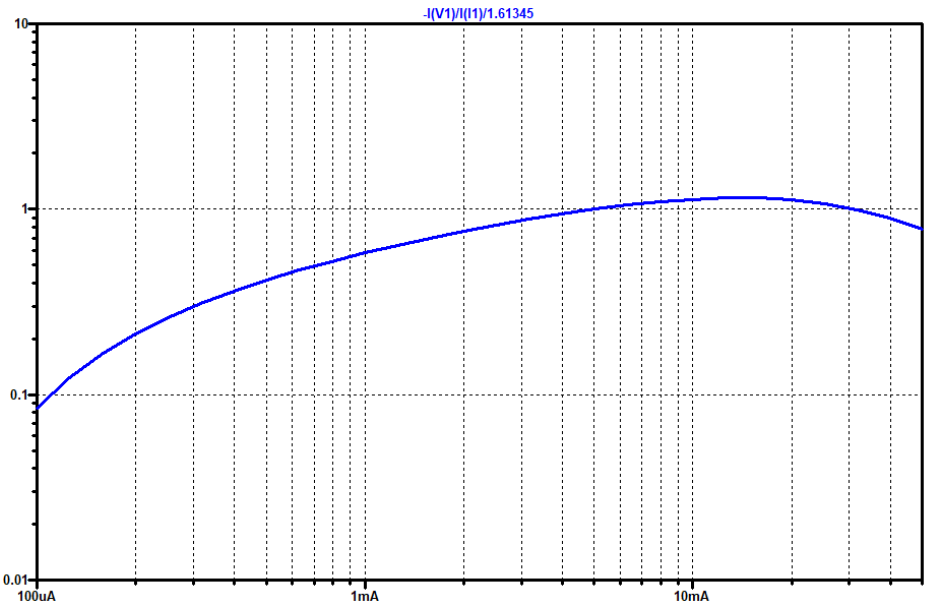
Referred to Data Sheet

```
.meas Norm FIND -I(V1)/I(I1) AT 5mA

.OPTION TNOM=25
.TEMP=25
.dc dec I1 0.1m 50m 10
```



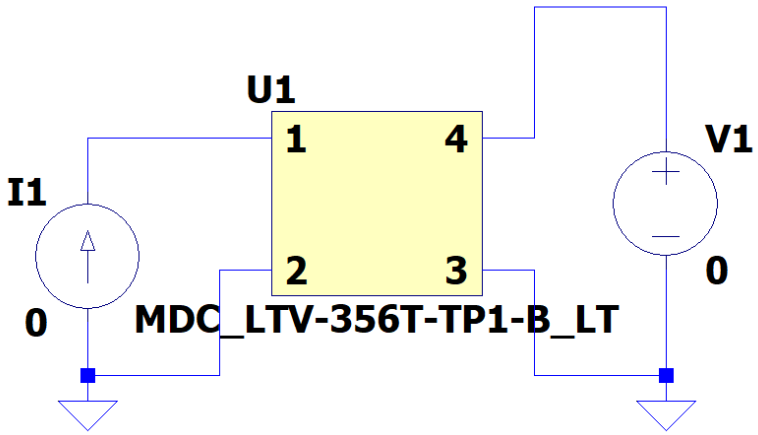
Simulation results are following.
Explanatory notes — : simulated



IC-VCE Testbench

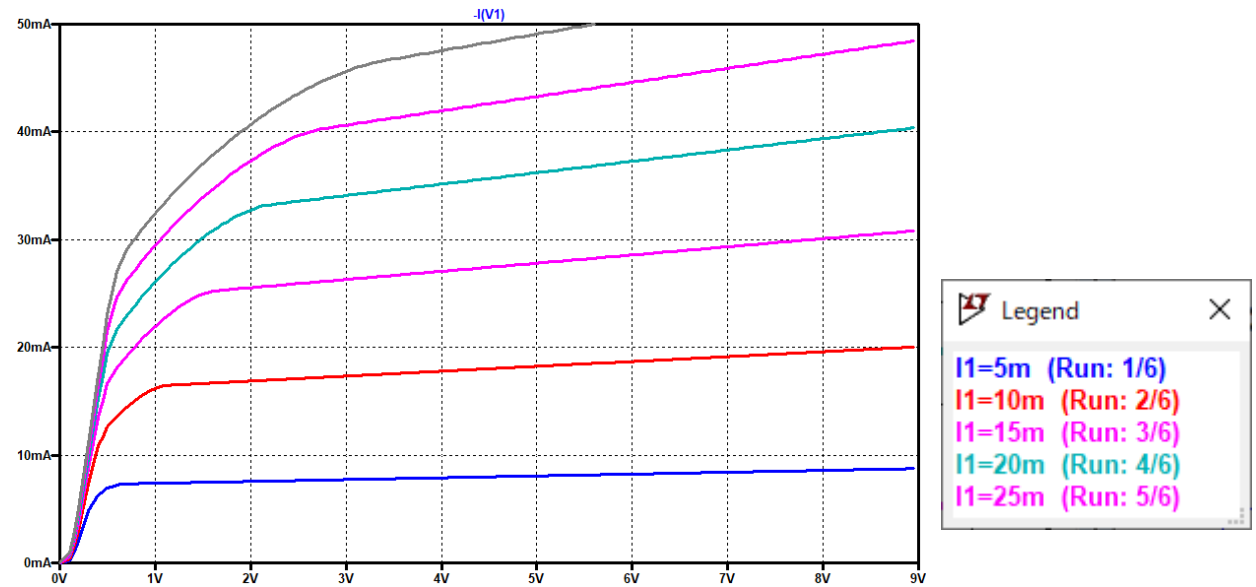
Referred to Data Sheet

```
.OPTION TNOM=25
.TEMP=25
.dc V1 0 9 0.1 I1 5m 30m 5m
```



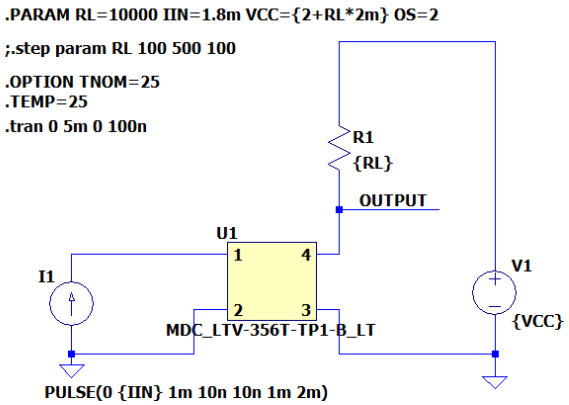
Simulation results are following.
Explanatory notes — : simulated

IC-VCE



ResponseT ime-Load Resistance Testbench

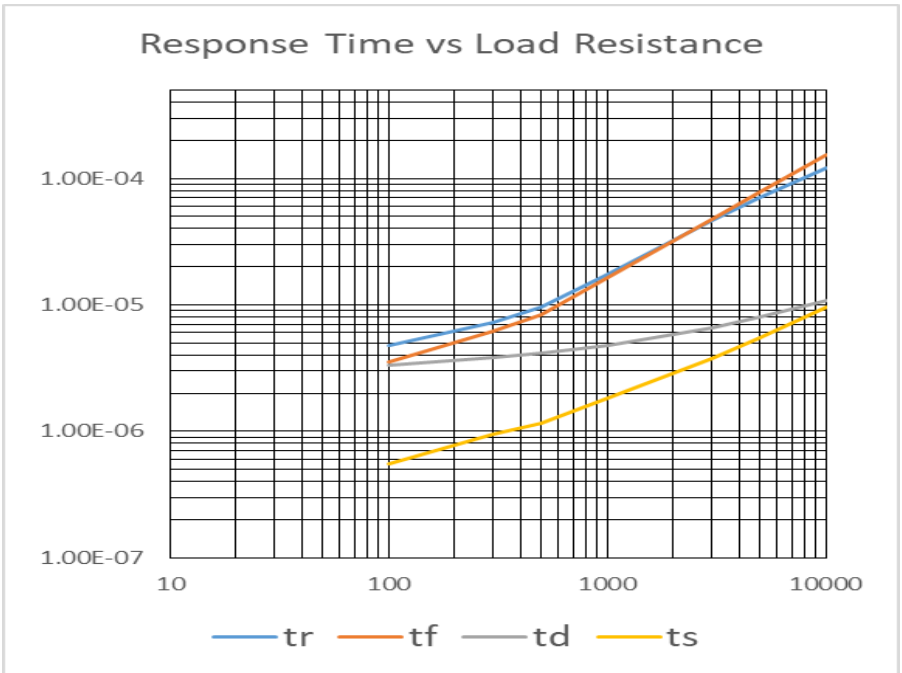
Referred to Data Sheet



.meas tr TRIG V(output)={VCC-{OS}}*0.9+{OS} FALL=2 TARG V(output)={VCC-{OS}}*0.1+{OS} FALL=2
.meas tff TRIG V(OUTPUT)={VCC-{OS}}*0.1+{OS} RISE=2 TARG V(OUTPUT)={VCC-{OS}}*0.9+{OS} RISE=2
.meas td FROM 3m TARG V(output)={VCC-{OS}}*0.9+{OS} FALL=2
.meas ts FROM 4m TARG V(output)={VCC-{OS}}*0.1+{OS} RISE=2

Simulation results are following.
Explanatory notes — : simulated

Response Time-Load Resistance



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