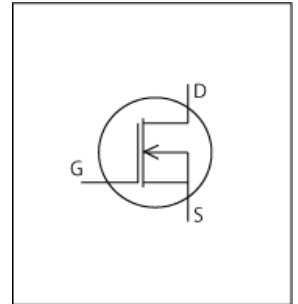


LTspice Model

NMOS

AOS

AONS62604



Model Information

Model A macro model based on BSIM3 model
Call Name MDC_AONS62604_LT
Pin Assign 1:S 2:S 3:S 4:G 5:D 6:D 7:D 8:D
File List Model Library MDC_AONS62604_LT01.lib
 Model Report MDC_AONS62604_LT.pdf (this file)

Verified Simulator Version LTspice version XVII
Note

References

The information which was used for modeling is as follow:

[Data Sheet]

- Date/Version Rev.1.0: January 2017
- Product name AONS62604
- Company name Alpha and Omega Semiconductor
- Characteristics IdVds[Vgs], IdVgs[Temp], Rds(on)Id[Vgs], Rds(on)Temp[Vgs], Rds(on)Vgs[Temp], IsVsd[Temp], VgsQg[Vdd], CapacitanceVds[Cname], SwitchingIdd[Tname], Trrlf[Ir], Qrrlf[Ir]

Simulation Range

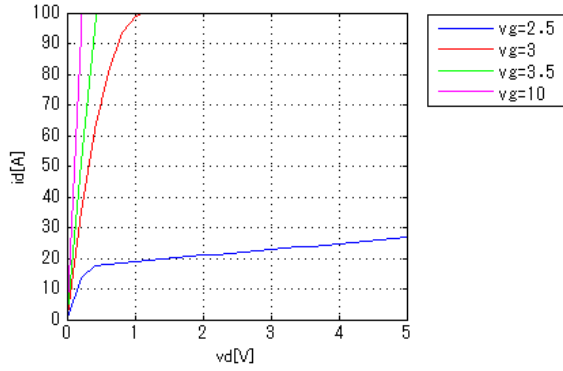
This table shows the range of evaluated simulation range that was not occurs any convergence problems in this area.

Item	Range			Unit
	Min.		Max.	
Drain-source voltage (DC)	0	to	60	V
Gate-source voltage (DC)	-20	to	20	V
Temperature	-55	to	150	deg C

Simulation results are following.
 Explanatory notes — : simulated

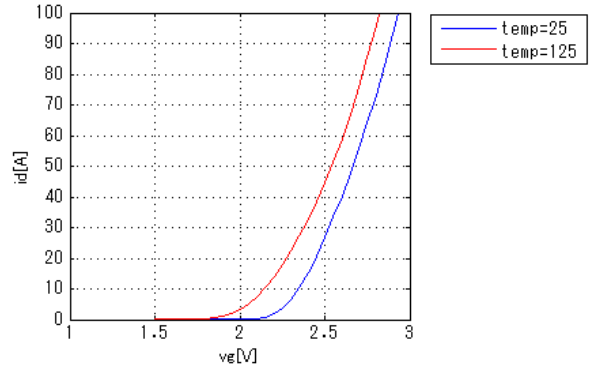
IdVds[Vgs]

Temp. = 25degC

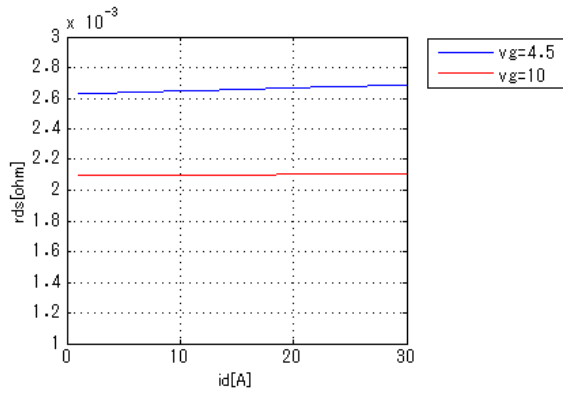


IdVgs[Temp]

Vds = 5V

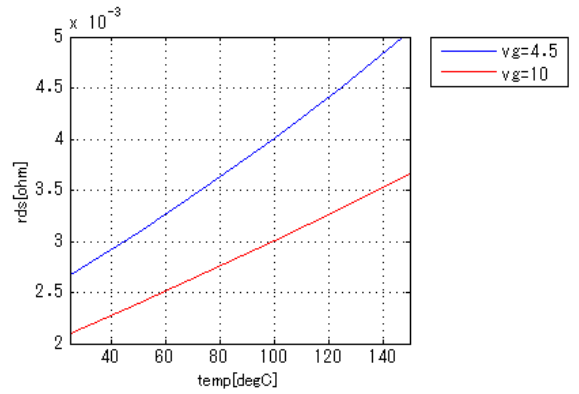


Rds(on)Id[Vgs]



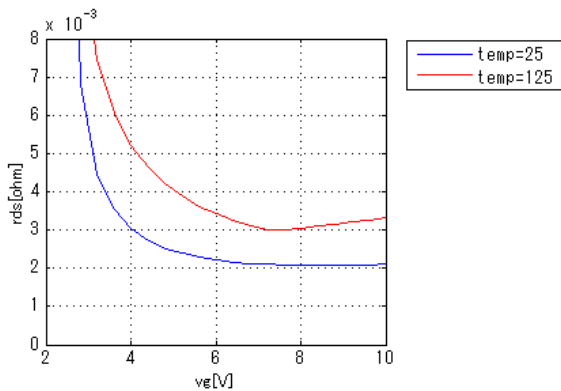
Rds(on)Temp[Vgs]

Id = 20A



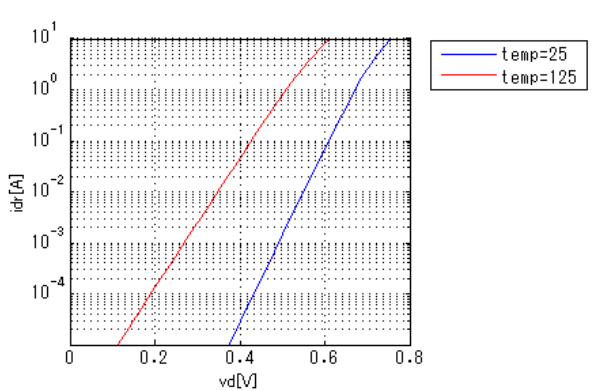
Rds(on)Vgs[Temp]

Id = 20A



IsVsd[Temp]

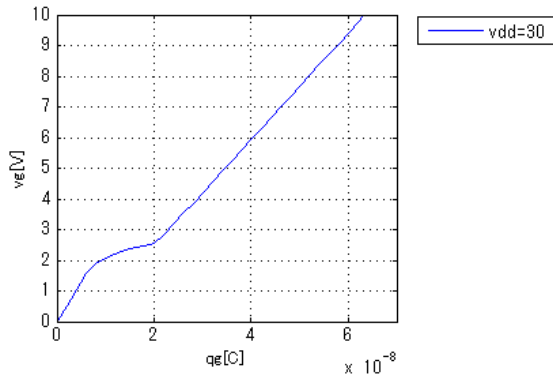
vg = 0V



Simulation results are following.
 Explanatory notes — : simulated

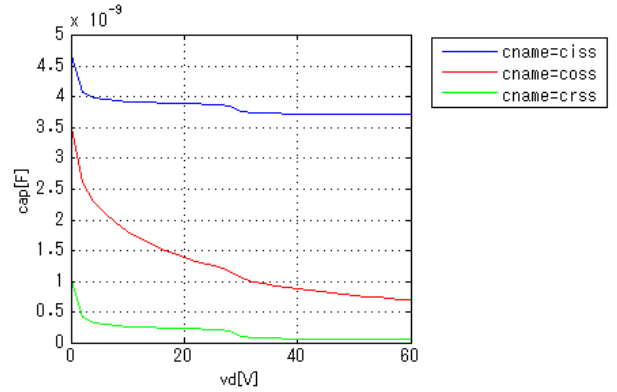
VgsQg[Vdd]

Id = A



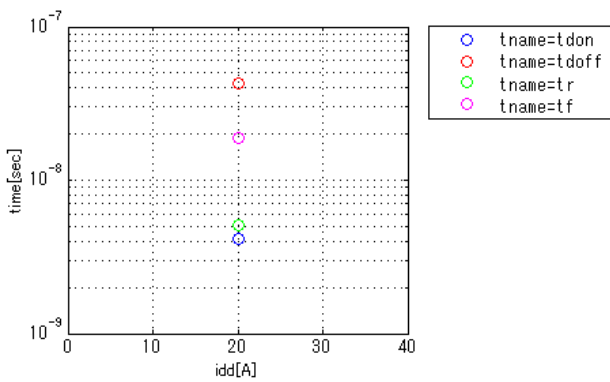
CapacitanceVds[Cname]

freq = 1000000Hz



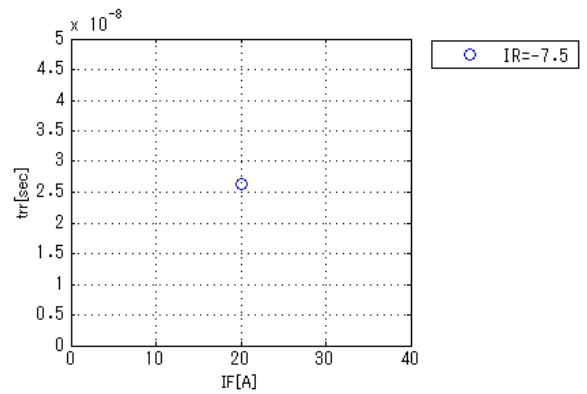
SwitchingIdd[Tname]

vvg = 10V, vdd = 30V, RGG = 3ohm



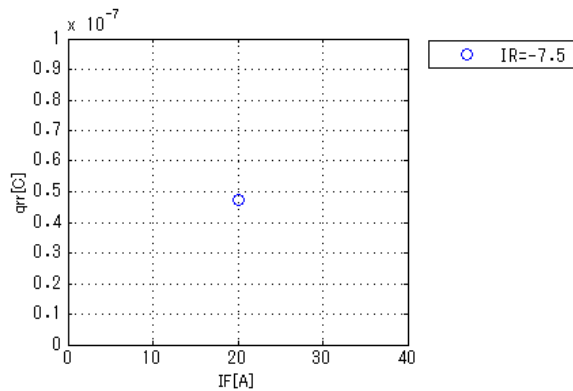
Trrlf[Ir]

vdd = 30V, didt = 500A/us, Temp = 25degC



Qrrlf[Ir]

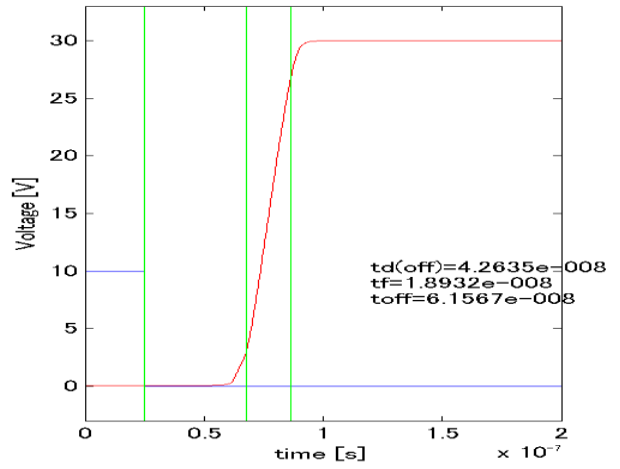
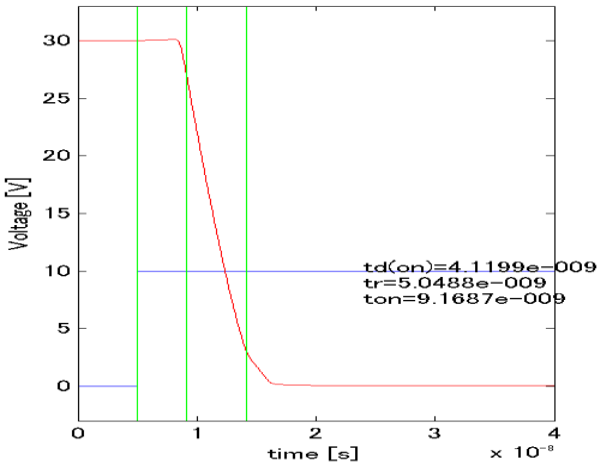
vdd = 30V, didt = 500A/us, Temp = 25degC



Simulation results are following.
 Explanatory notes — : simulated

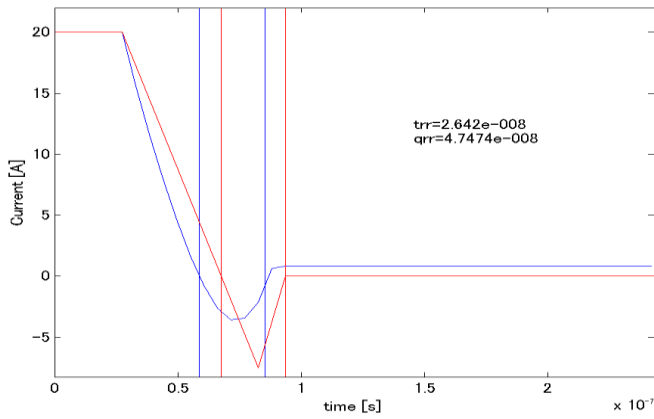
Switching Waveform

Blue : INPUT Red : OUTPUT



Trr Qrr Waveform

Red : Datasheet Blue : Simulation



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