LTspice Model
Logic IC
Toshiba Corporation
74VHC245FT

Model Information

Model	A macro model
Call Name	MDC_74VHC245FT_LT
Pin Assign	1:DIR 2:A1 3:A2 4:A3 5:A4 6:A5 7:A6 8:A7 9:A8 10:GND 11:B8 12:B7 13:B6 14:B5 15:B4 16:B3 17:B2 18:B1 19:_G 20:Vcc
File List	Model Library MDC_74VHC245FT_LT01.lib Model Report MDC_74VHC245FT_LT.pdf(this file)

Verified Simulator Version LTspice 17.1.15

Note

References

The information which was used for modeling is as follow:

[Data Sheet]

- ●Date/Version
- ●Product name 74VHC245FT
- ●Company name Toshiba Corporation

[Characteristics listed]

- ●Characteristics Vih, Vil, Voh, Vol, Ioz, Iin, Icc
  tpLH, tpHL, tpLZ, tpZL, tpHZ, tpZH
  Cin, Cout

Simulation Condition

This table shows the range of evaluated simulation range that was not occurs any convergence problems in this area.

Item	Condition			Unit
	Min	Typ	Max	
Power Supply Voltage	2.0		5.5	V
Temperature		25		deg C

Logic Gate

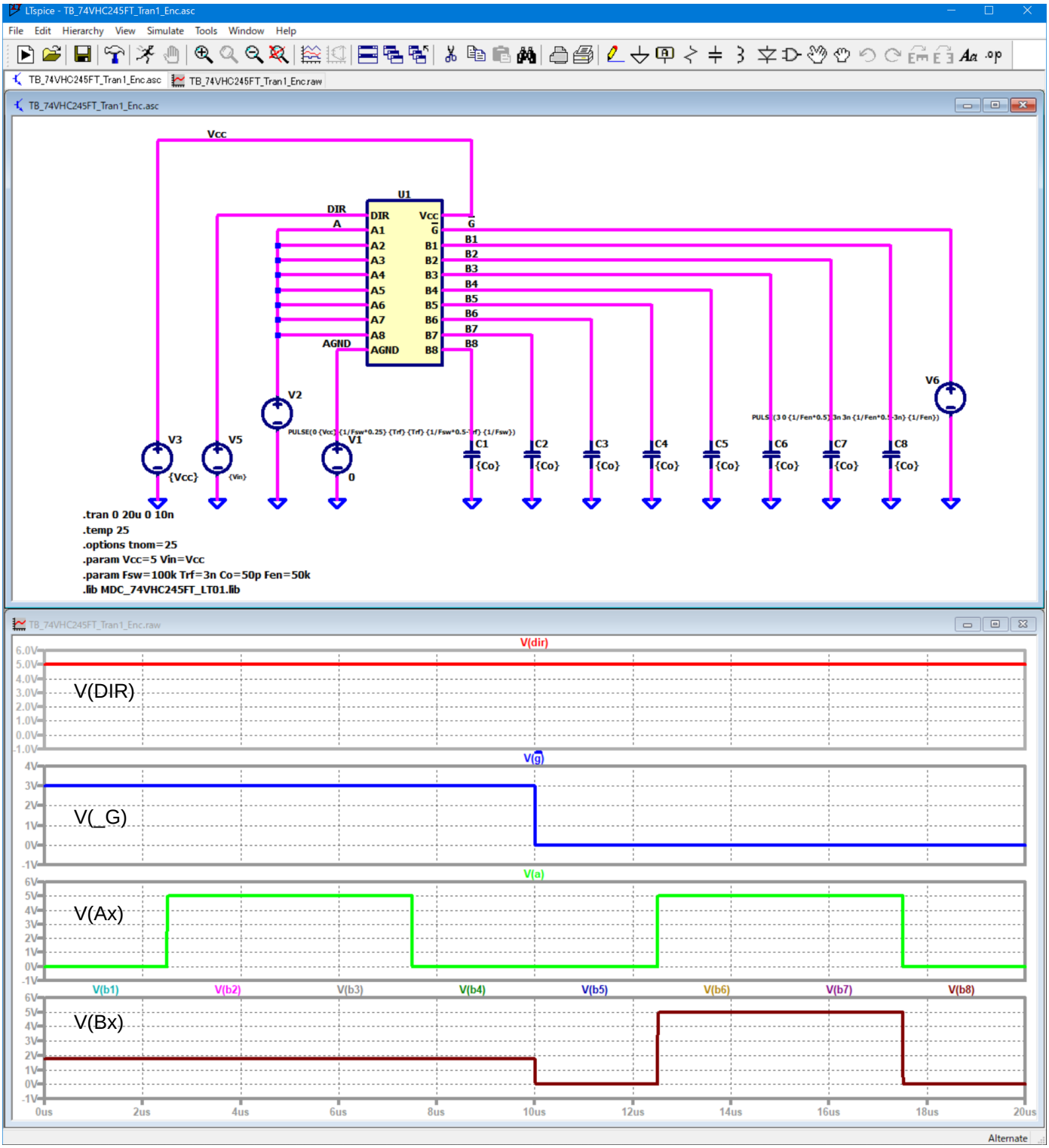
○ : Implemented
× : Not Implemented
— : Not applicable

Model Functions Table

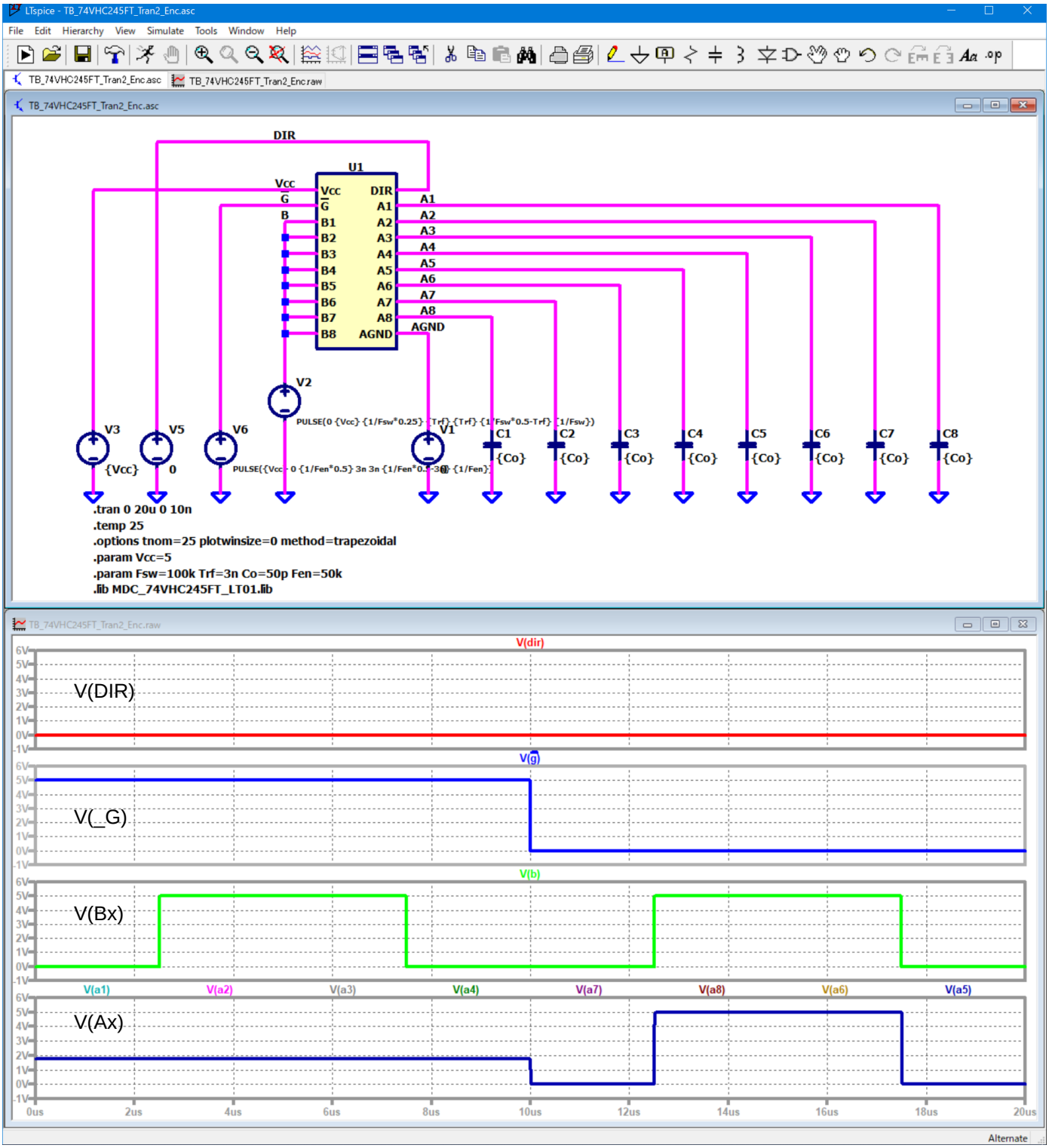
RANK=2

Functions	RANK	Implemented
Truth Table	1	○
Propagation Delay	1	○
CMOS/Open Drain Output	1	○
Schmitt trigger	1	○
Timing Chart	1	○
Input Protection	2	○
Output Protection	2	○
Power Supply Current	2	○

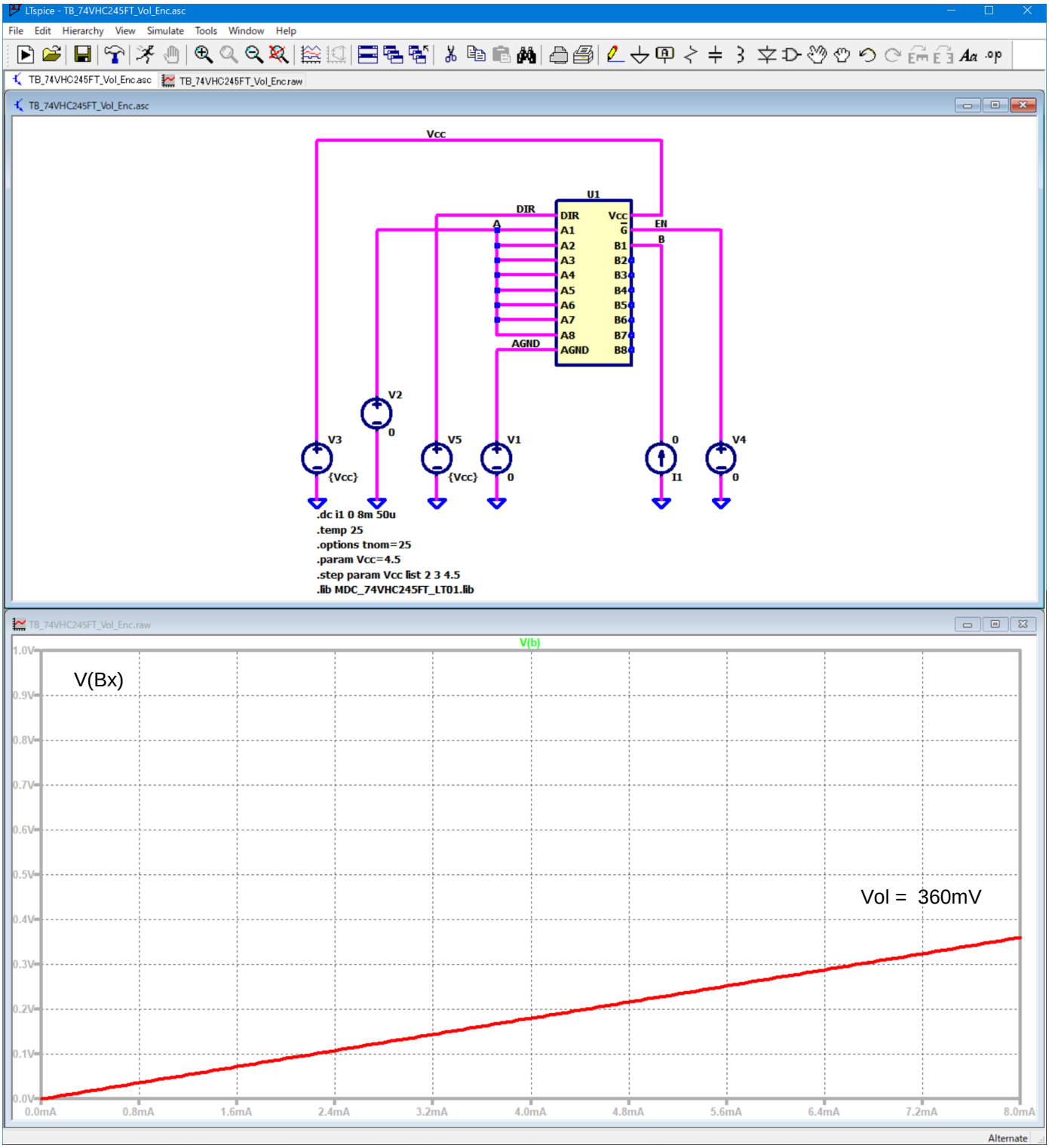
Testbench for truth table function (Vcc = 5[V], DIR = 5[V], Ax = 5[V] Freq. = 100[kHz],Co = 50[pF])



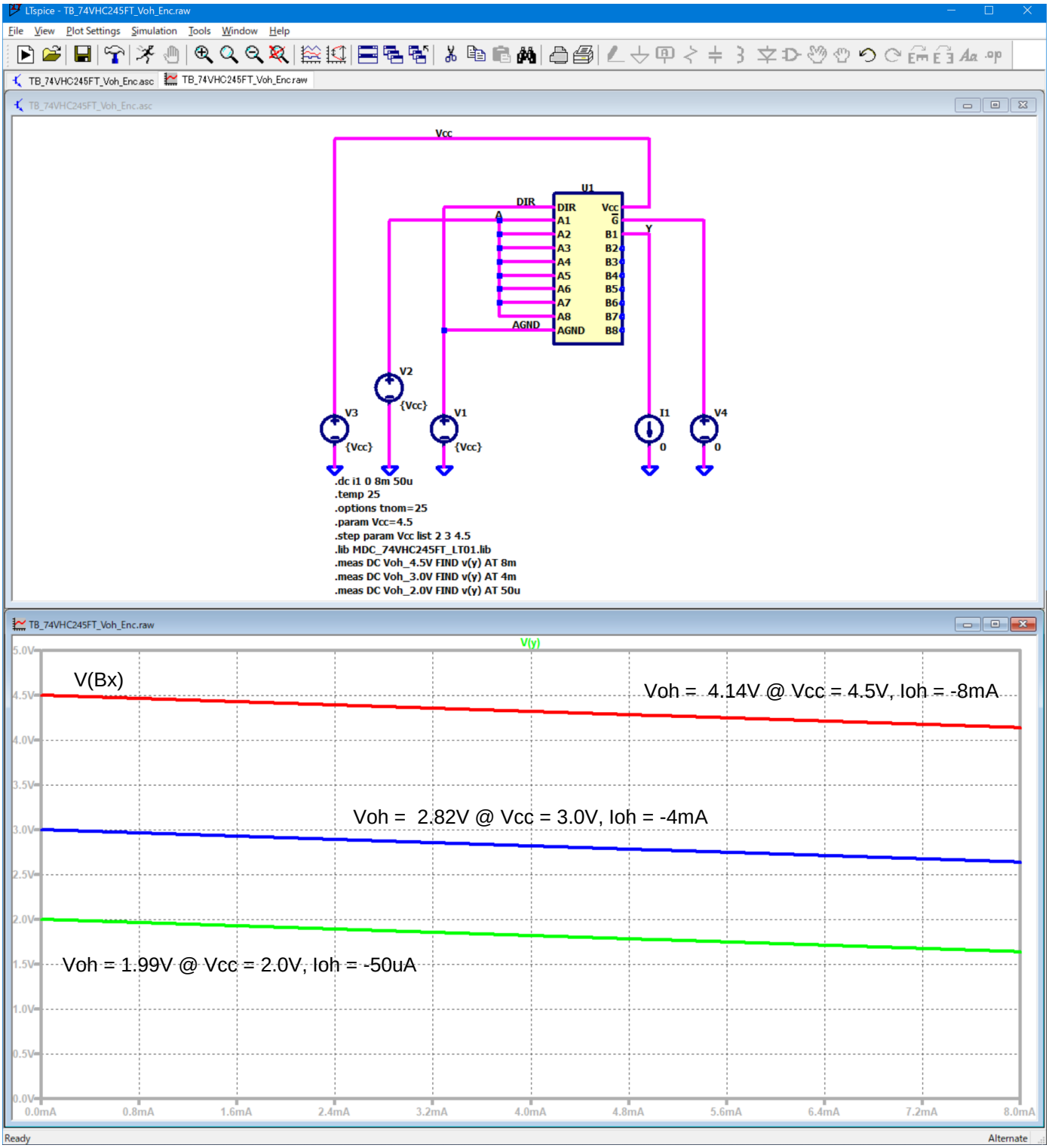
Testbench for truth table function (Vcc = 5[V], DIR = 0[V], Bx = 5[V] Freq. = 100[kHz],Co = 50[pF])



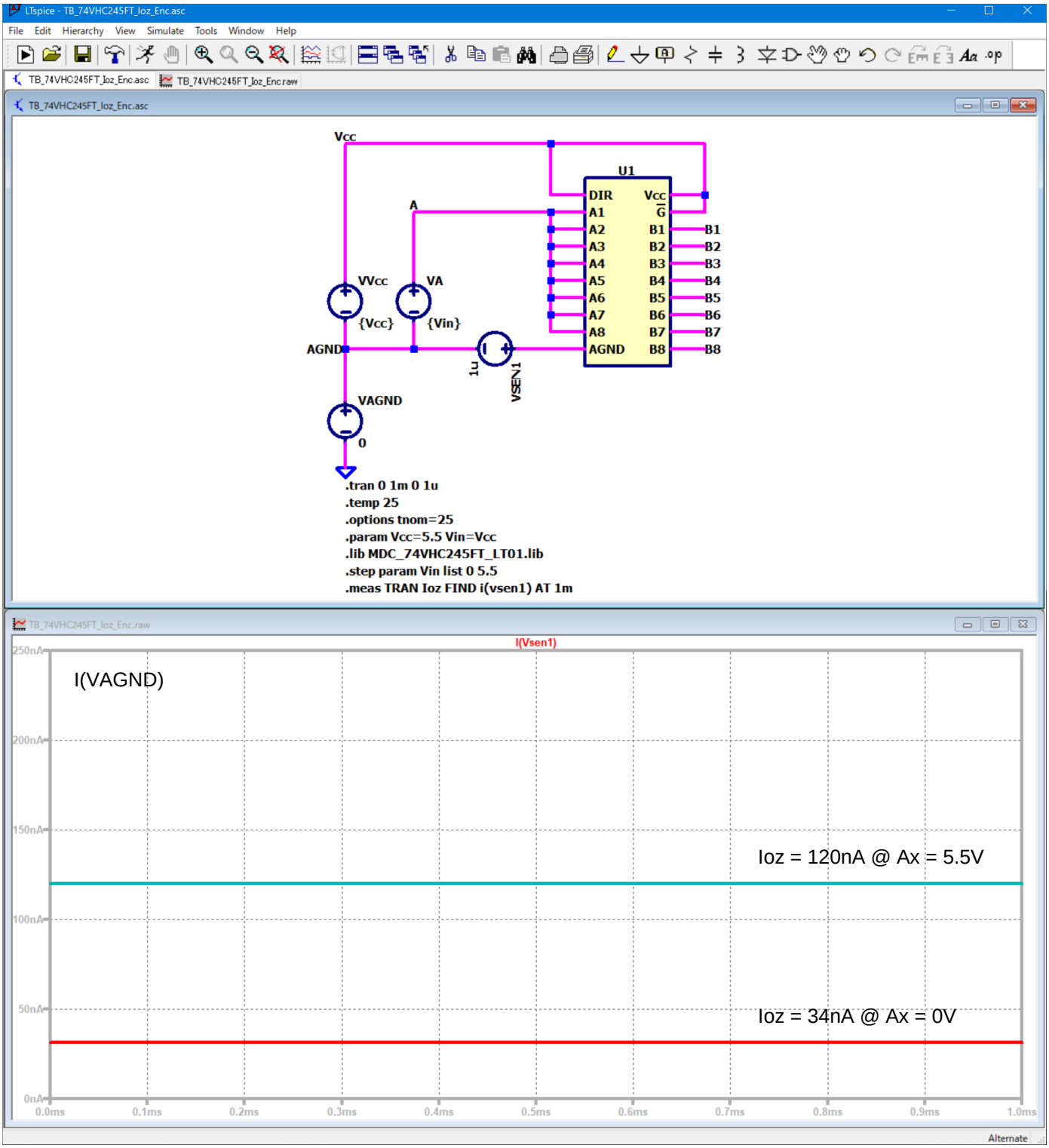
Testbench for Vol (Vcc = 5[V], DIR = 5[V], Ax = 0[V], Io = 8[mA])



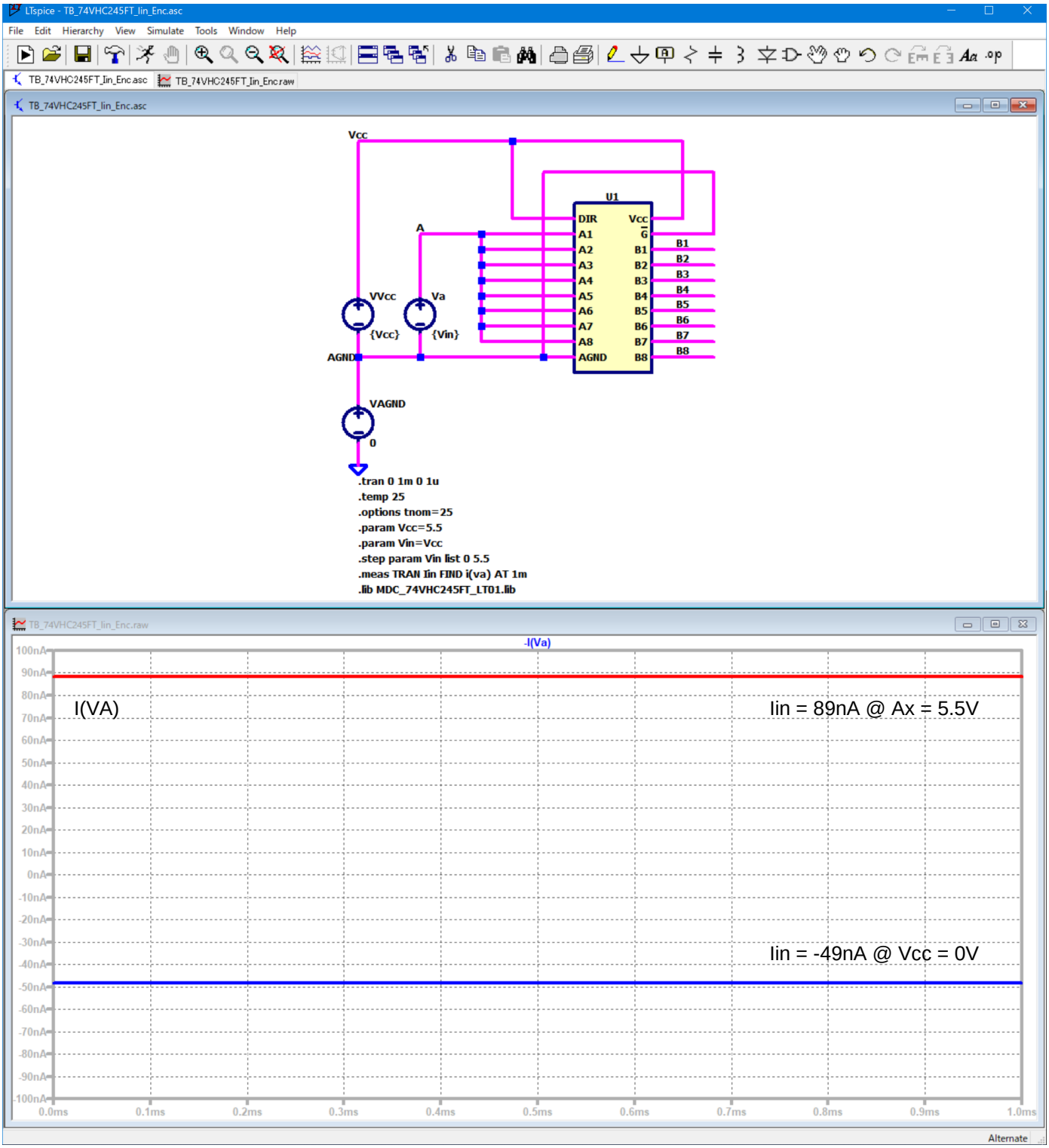
Testbench for Voh (Vcc = 5[V], DIR = 5[V], Ax = 5[V], Io = From -50[uA] to -8[mA])



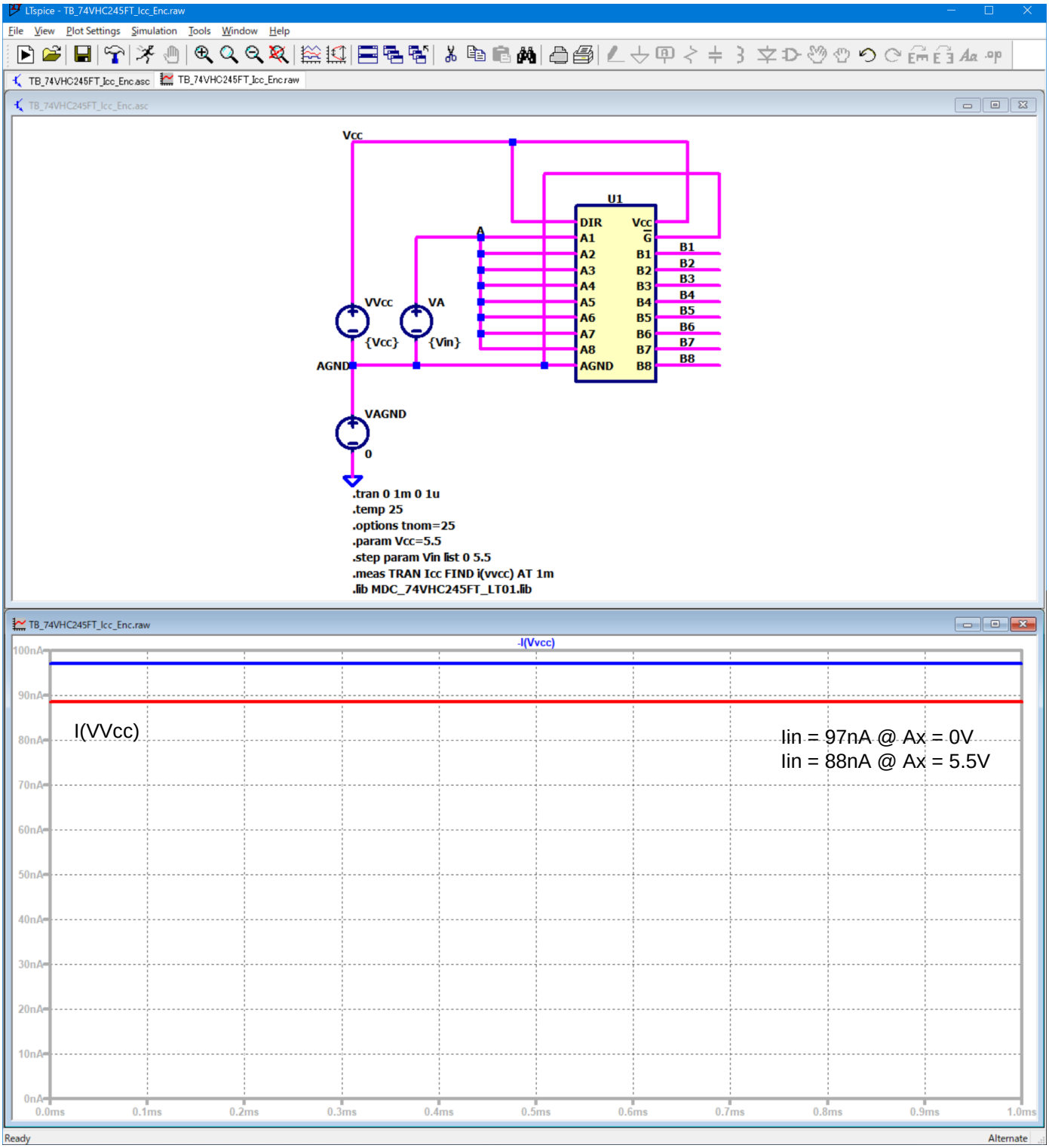
Testbench for Ioz (Vcc = 5.5[V], DIR = 5.5[V], Ax = 0[V] or 5.5[V], _G = 5.5[V])



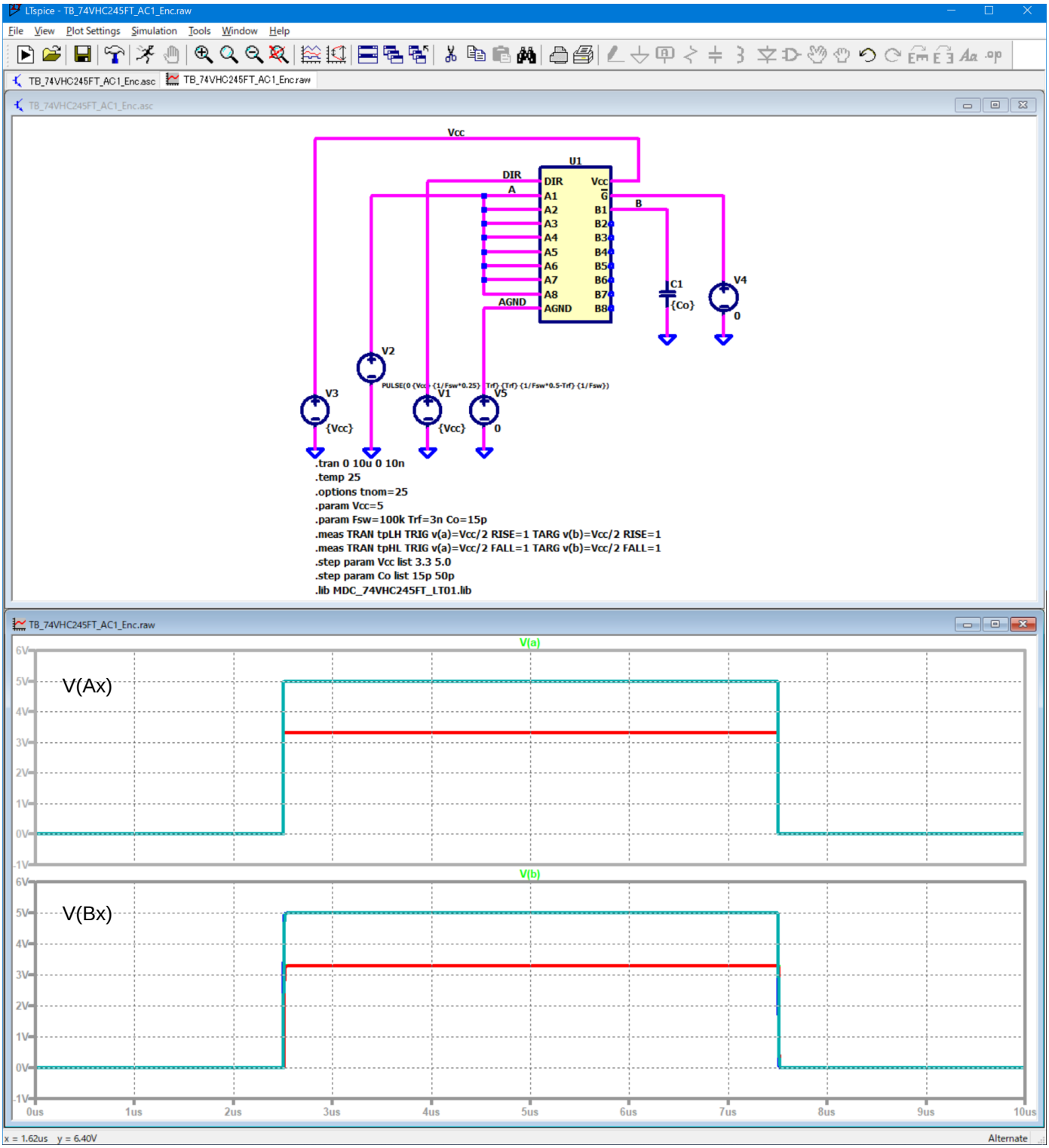
Testbench for Iin (Vcc = 5.5[V], DIR = 5.5[V], Ax = 0[V] or 5.5[V], _G = 0[V])



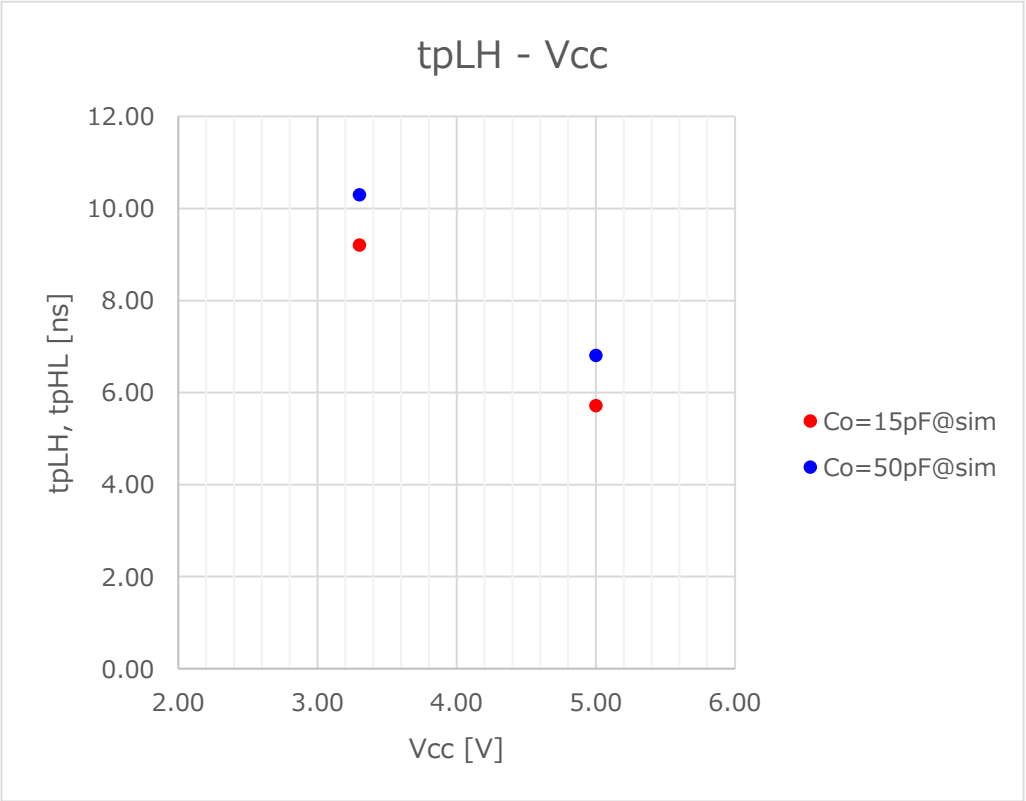
Testbench for Icc (Vcc = 5.5[V], DIR = 5.5[V], Ax = 0[V] or 5.5[V], _G = 0[V])

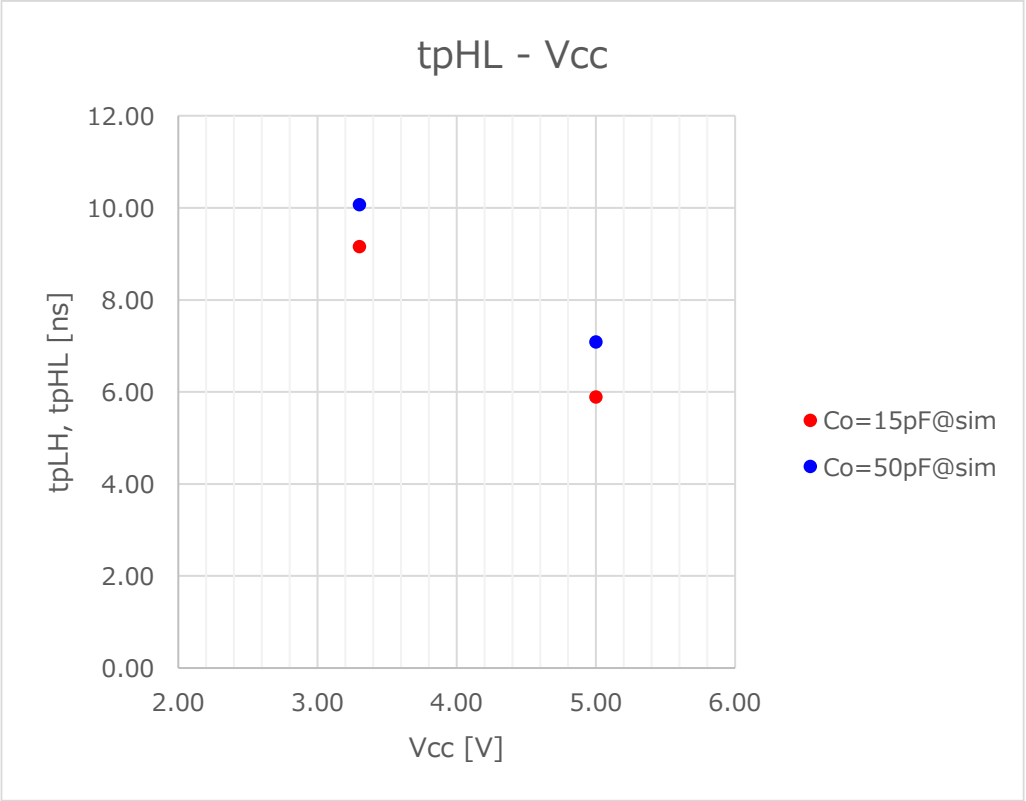


Testbench for tpLH, tpHL (Vcc = 3.3/5.0[V], DIR = 3.3/5.0[V], Ax = 3.3/5.0[V], _G = 3.3/5.0[V], Co = 15/50[pF])

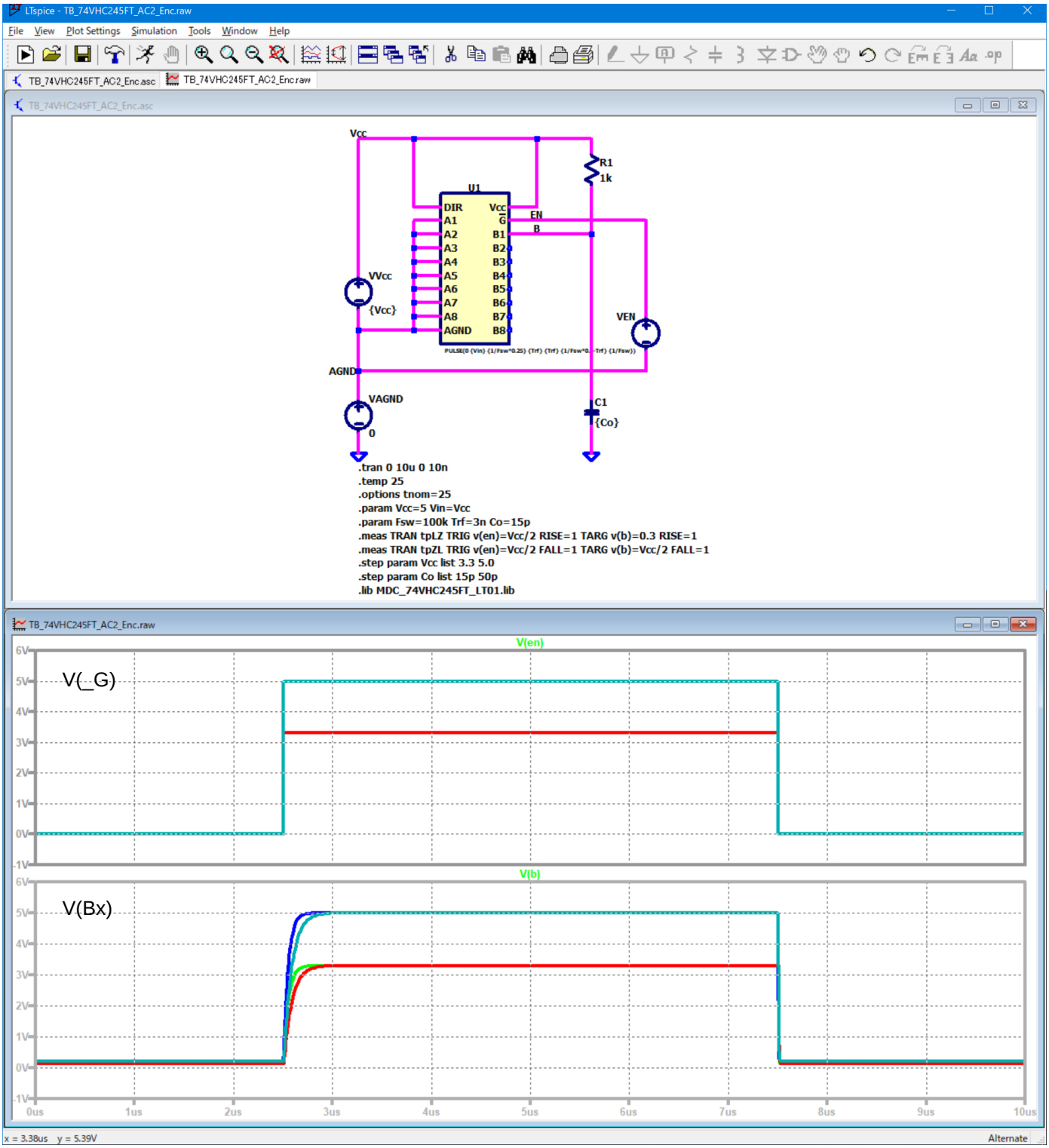


Testbench for tpLH, tpHL (Vcc = 3.3/5.0[V], DIR = 3.3/5.0[V], Ax = 3.3/5.0[V], _G = 3.3/5.0[V], Co = 15/50[pF])

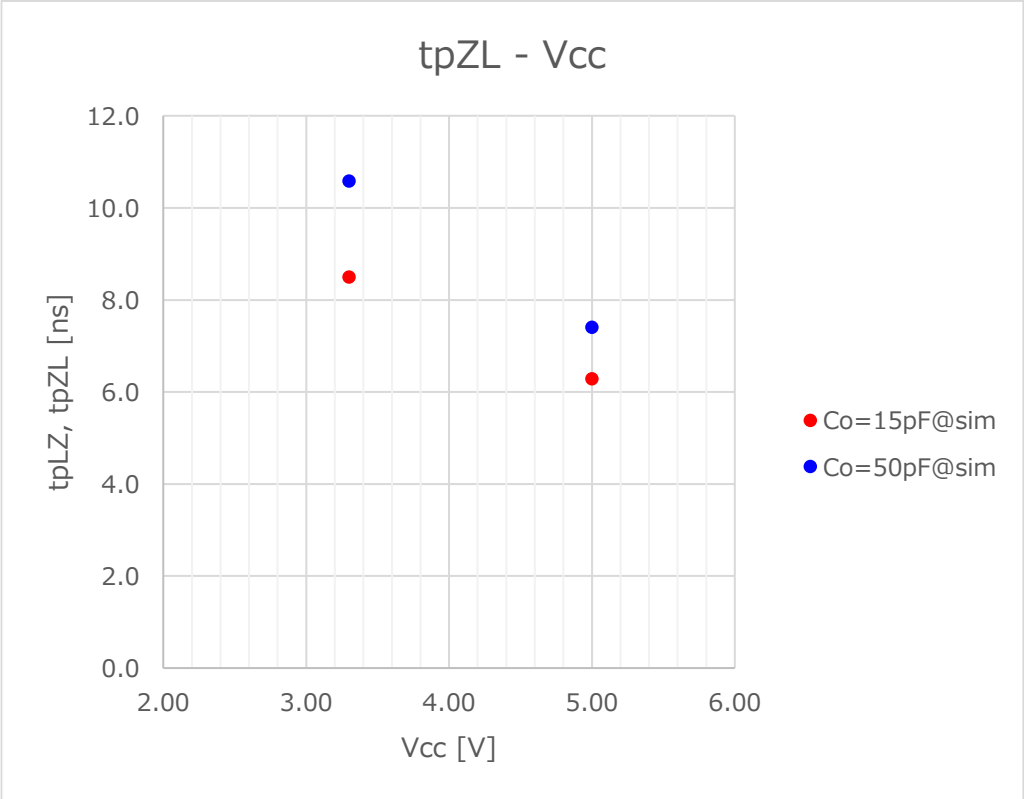


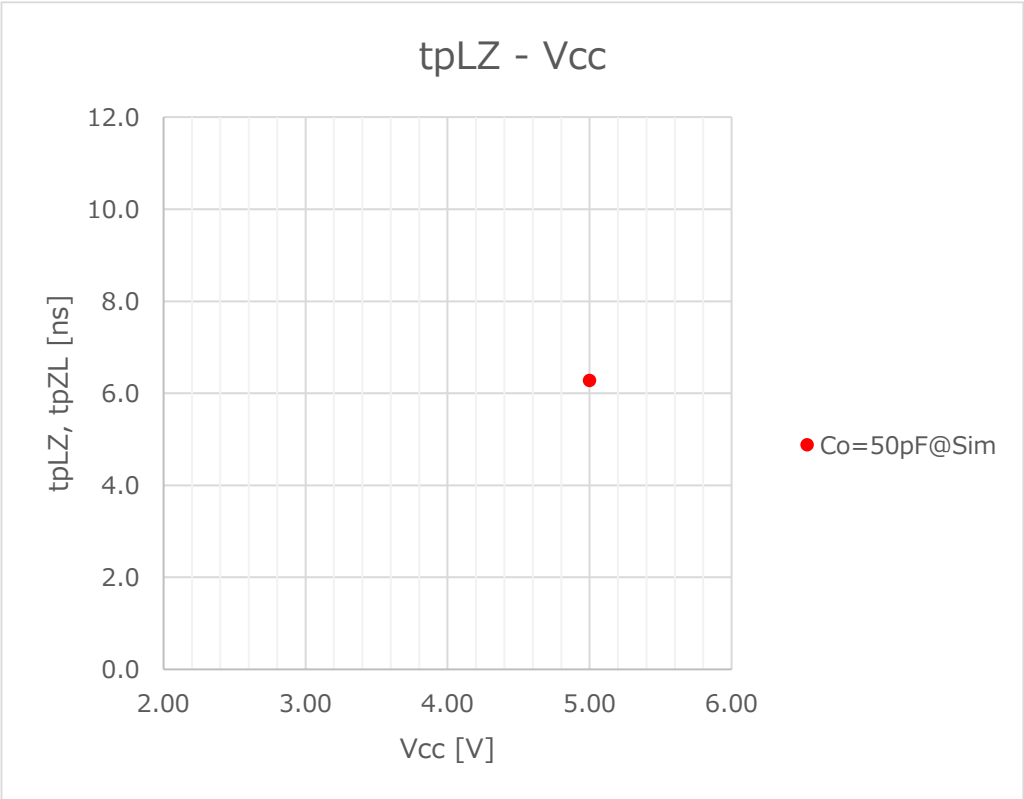


Testbench for tpZL, tpLZ (Vcc = 3.3/5.0[V], DIR = 3.3/5.0[V], Ax = 3.3/5.0[V], _G = 3.3/5.0[V], Co = 15/50[pF])

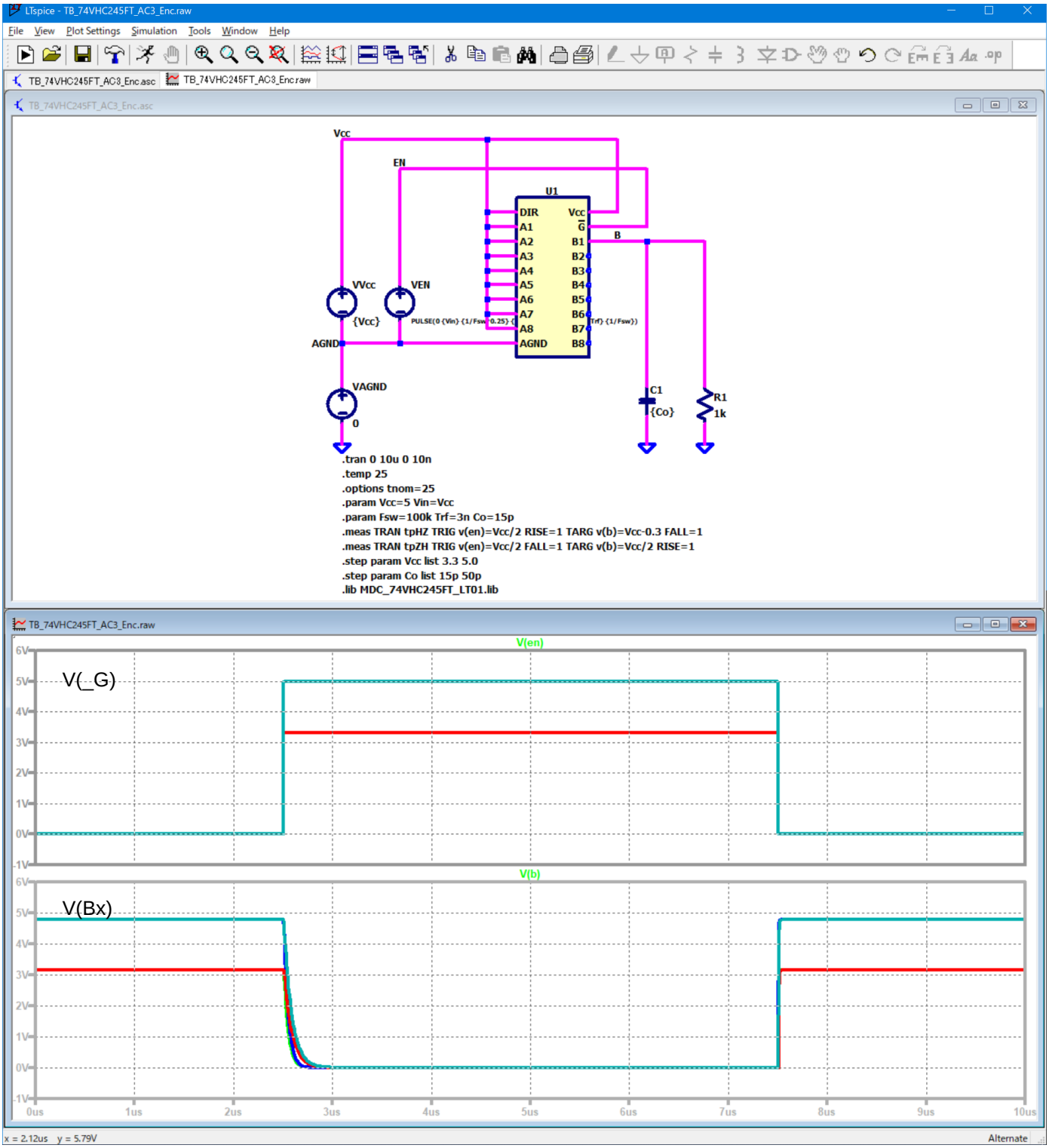


Testbench for tpLZ, tpZL (Vcc = 3.3/5.0[V], DIR = 3.3/5.0[V], Ax = 3.3/5.0[V], _G = 3.3/5.0[V], Co = 15/50[pF])

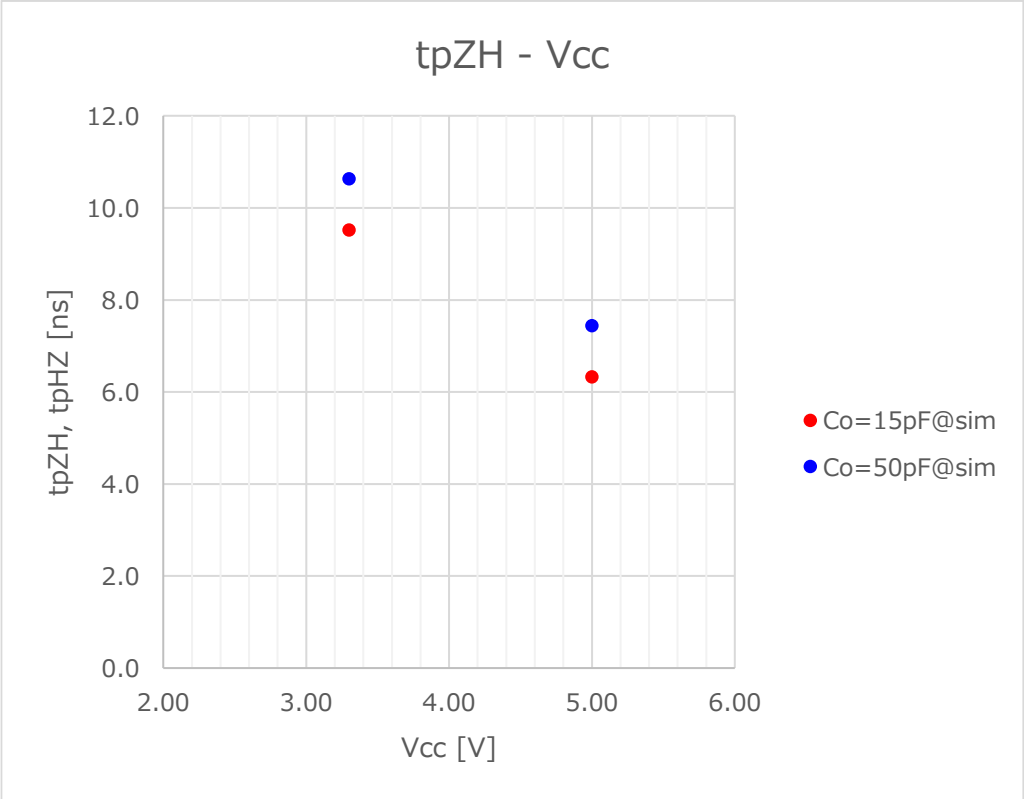


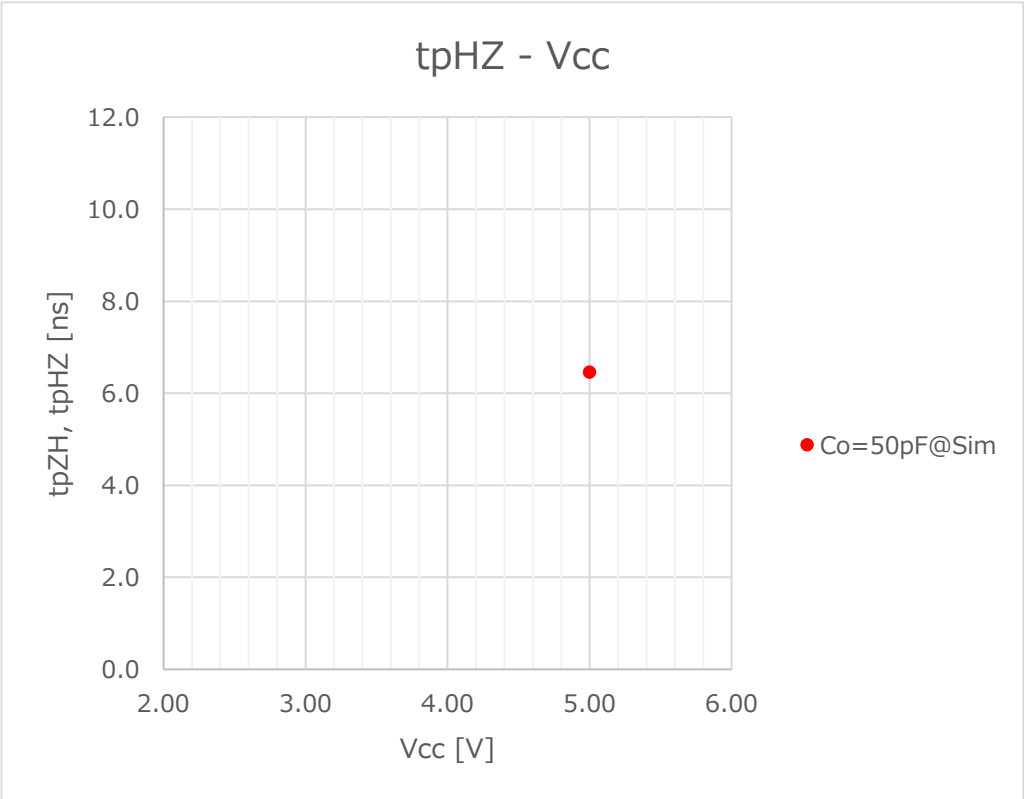


Testbench for tpZH, tpHZ



Testbench for tpHZ, tpZH





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