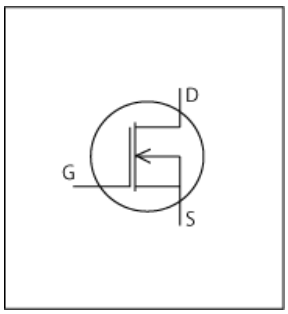
LTspice Model
NMOS
STM
STL50DN6F7



Model Information

Model	A macro model based on BSIM3 model	
Call Name	MDC_STL50DN6F7_LT	
Pin Assign	1:S2 2:G2 3:S1 4:G1 5:D1 6:D1 7:D2 8:D2	
File List	Model Library	MDC_STL50DN6F7_LT01.lib
	Model Report	MDC_STL50DN6F7_LT.pdf (this file)
Verified Simulator Version		LTspice version XVII
Note		

References

The information which was used for modeling is as follow:

[Data Sheet]

- ●Date/Version: November 2015 Rev 2
- ●Product name: STL50DN6F7
- ●Company name: STMicroelectronics N.V.
- ●Characteristics: IdVds[Vgs],IdVgs[Temp],VgsQg[Vdd],Rds(on)Id[Vgs],CapacitanceVds[Cname],VthTemp[Id],Rds(on)Temp[Vgs],BvTemp[ir],VsdIs[Temp],SwitchingIdd[Tname],SwitchingWaveform,TrrIf[Ir],QrrIf[Ir],TrrQrrWaveform

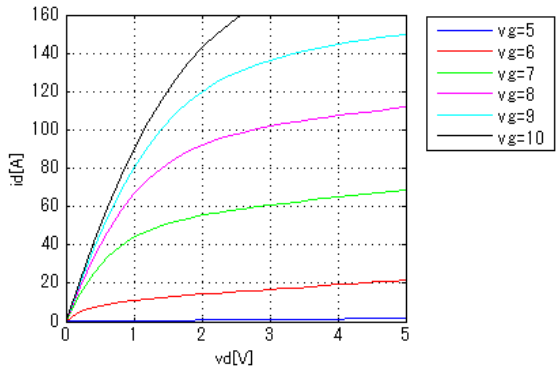
Simulation Range

This table shows the range of evaluated simulation range that was not occurs any convergence problems in this area.

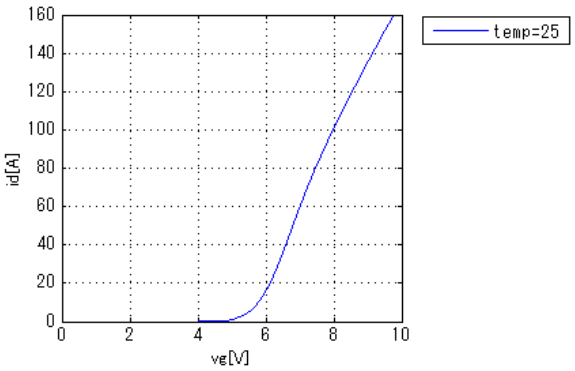
Item	Range			Unit
	Min.		Max.	
Drain-source voltage (DC)	0	to	60	V
Gate-source voltage (DC)	-20	to	20	V
Temperature	-55	to	175	deg C

Simulation results are following.
Explanatory notes — : simulated

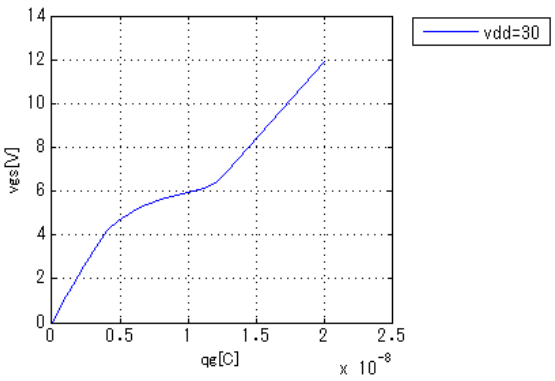
IdVds[Vgs]
Temp. = 25degC



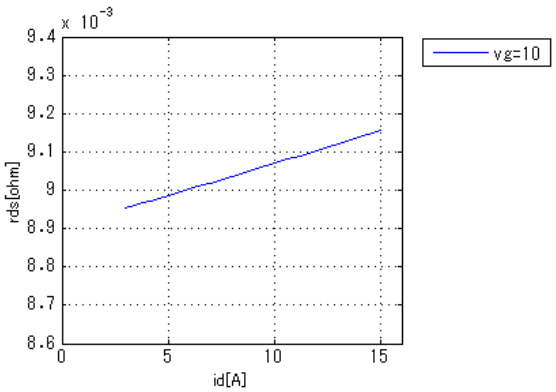
IdVgs[Temp]
Vds = 3V



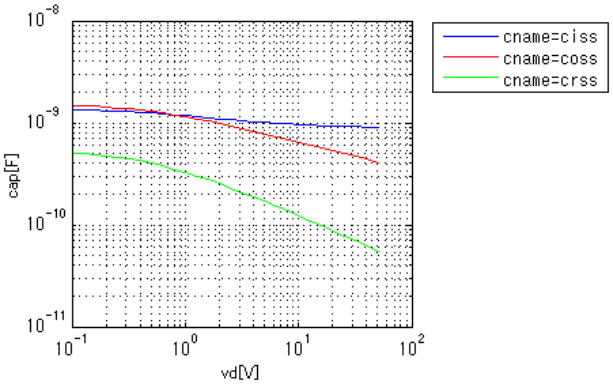
VgsQg[Vdd]
Id = 15A



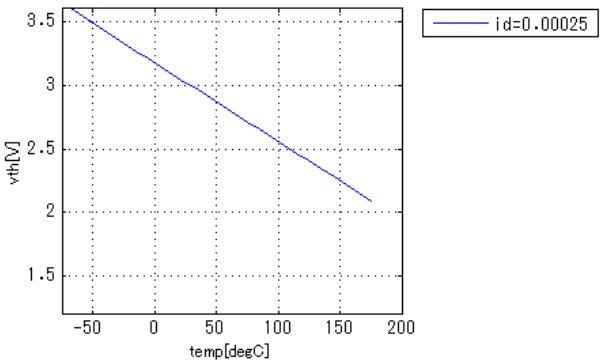
Rds(on)Id[Vgs]



CapacitanceVds[Cname]
freq = 1000000Hz



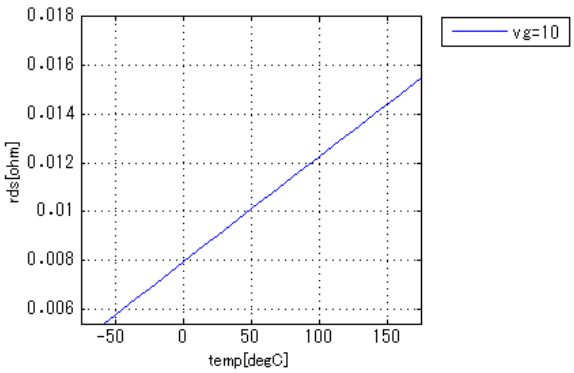
VthTemp[Id]
Vd = Vg



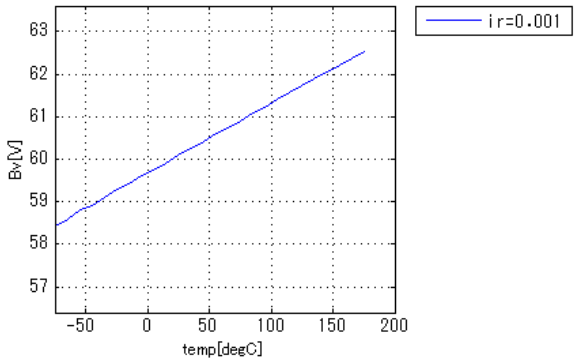
Simulation results are following.
Explanatory notes — : simulated

Rds(on)Temp[Vgs]

Id = 7.5A

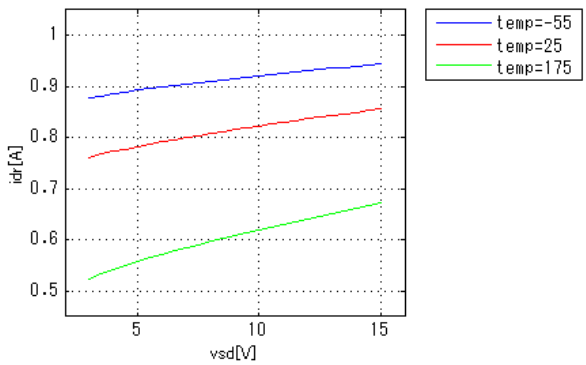


BvTemp[ir]



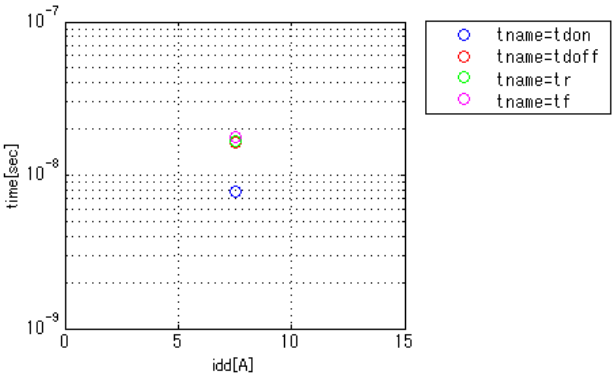
VsdIs[Temp]

vg = 0V



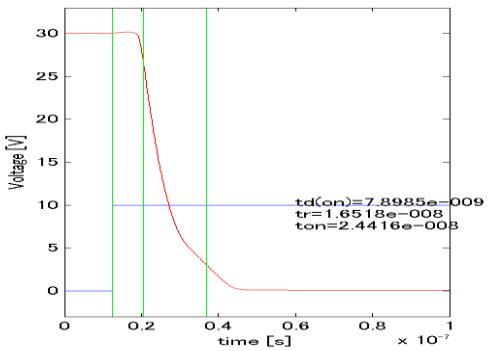
SwitchingIdd[Tname]

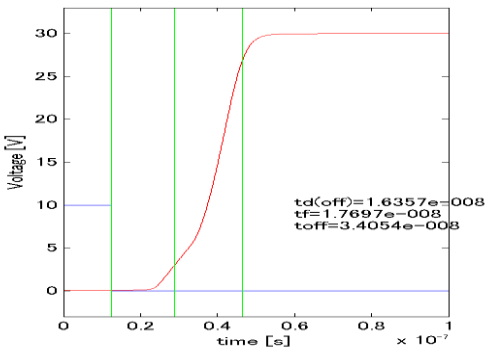
vgg = 10V, vdd = 30V, RGG = 4.7ohm



SwitchingWaveform

Blue : INPUT Red : OUTPUT

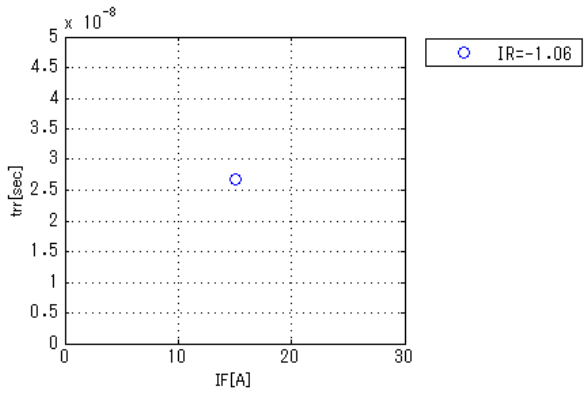




Simulation results are following.
Explanatory notes — : simulated

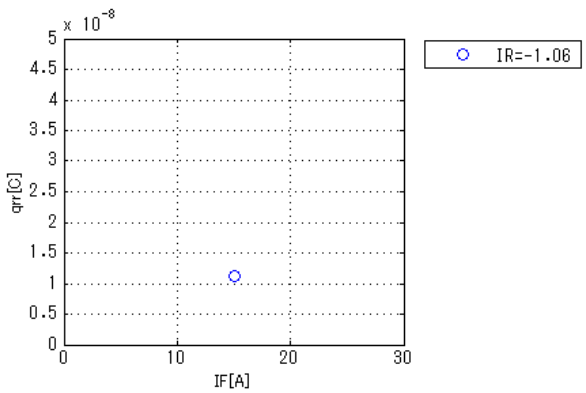
TrrIf[Ir]

vdd = 48V, didt = 100A/us

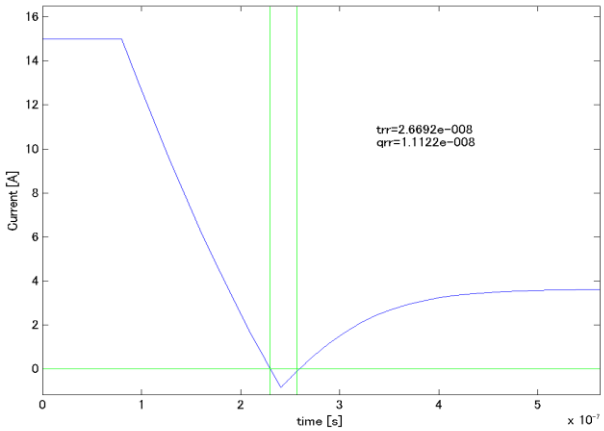


QrrIf[Ir]

vdd = 48V, didt = 100A/us



TrrQrrWaveform



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Modeling Design Technology

MoDeCH Inc.

Head Office
Location: Taiju-Seimei-Hachioji Bldg., 5-15 Yokoyama-cho, Hachioji-Shi, Tokyo 192-0081, Japan
Tel:+81-42-656-3360
E-Mail:model-on-support@modech.co.jp
URL:http://www.modech.com/en/