PSpice Model
N-Channel
FAIRCHILD
J201

Model Information

Model	A macro model
Call Name	MDC_J201_PS
Pin Assign	1:G 2:S 3:D
File List	Model Library MDC_J201_PS.lib
	Model Report MDC_J201_PS.pdf

Verified Simulator Version

Note

References

The information which was used for modeling is as follow:

[Data Sheet]

●Date/Version
●Product name   J201
●Company name   FAIRCHILD

[Characteristics listed]

●Characteristics   IdVgs[Temp],IdVds[Vgs],VGS(off),IDSS,
CibVe,CobVc,fTIc[Vce]

Simulation Condition

This table shows the range of evaluated simulation range that was not occurs any convergence problems in this area.

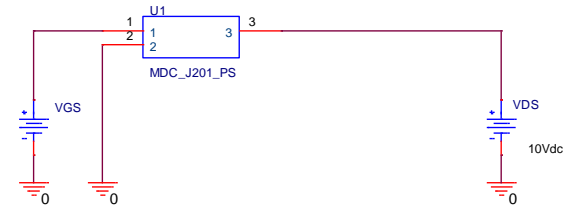| Item	Condition	Unit
Temperature	25	deg C

JFET

Model Functions Table

Functions	RANK=1	
	RANK	Implemented
ID-VDS-VGS	1	○
ID-VGS	1	○
VGS(off)-IDSS	1	○
yfs-IDSS	1	○
RDS(on)-IDSS	1	—
Crs Capacitance	1	○
Cis Capacitance	1	○

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Simulation results are following.
Explanatory notes ― : simulated

IdVgs[Temp] Testbench

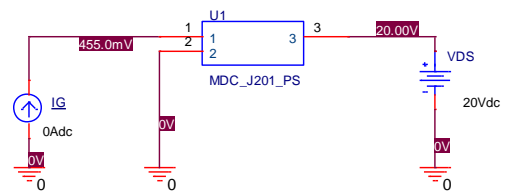## IdVds[Vgs] Testbench

IdVgs[Temp] Data Sheet

green:-55℃
red:25℃
blue:125℃

IdVds[Vgs] Data sheet

green:0V
red:-0.5V
blue:-1.0V
yellow:-1.5V
pink:-2.0V
light blue:-2.5V
orange:-3.0V
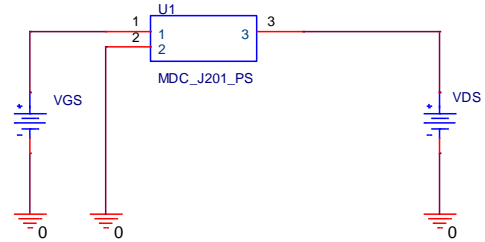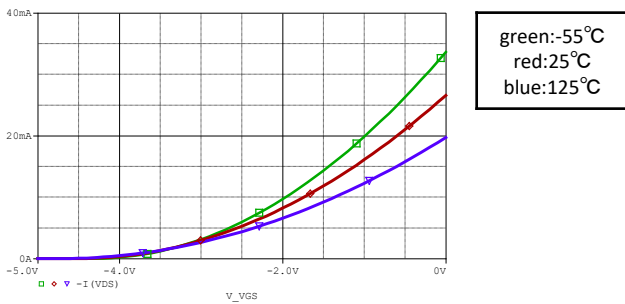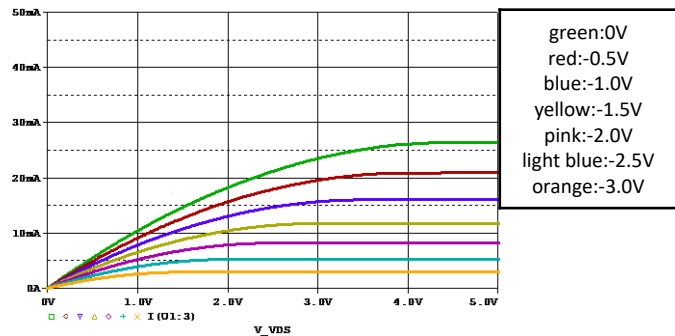
VGS(off) Testbench

CONDITIONS	MIN.	TYP.	MAX.	UNIT
Vds = 20 V, Id = 10 nA	-0.3	-	-1.5	V

IDSS Testbench

CONDITIONS	MIN.	TYP.	MAX.	UNIT
Vds = 20 V, Igs = 0	0.2	-	1.0	mA
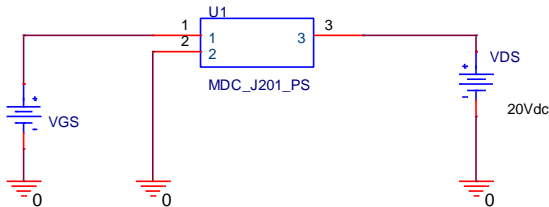
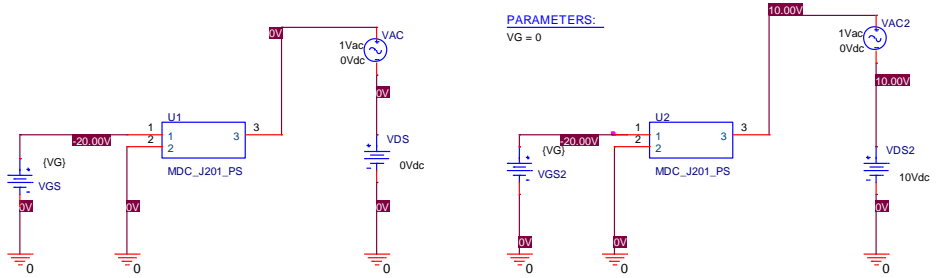## VGS(off) Data Sheet

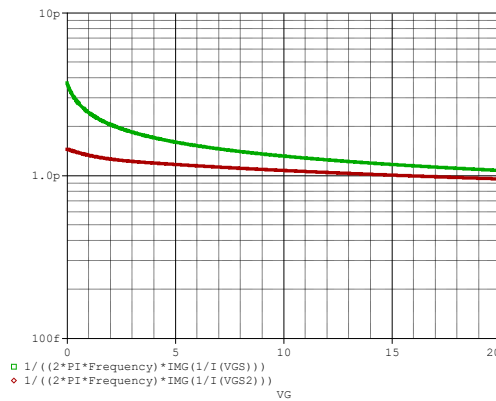## IDSS Data Sheet

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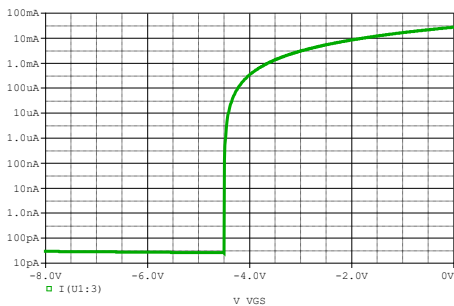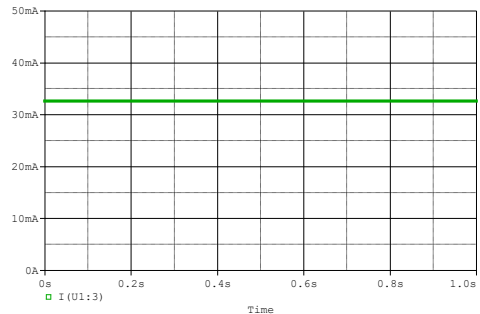
Simulation results are following.
Explanatory notes 　 ― : simulated

Crs Capacitance Testbench

Crs Capacitance Data Sheet

red:VDS=10V
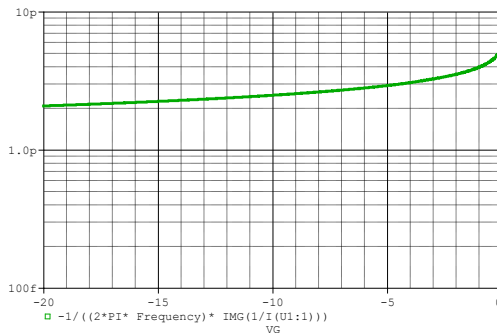green:VDS=0V

□ 1/((2*PI*Frequency)*IMG(1/I(VGS)))
◇ 1/((2*PI*Frequency)*IMG(1/I(VGS2)))
VG

Cis Capacitance Testbench
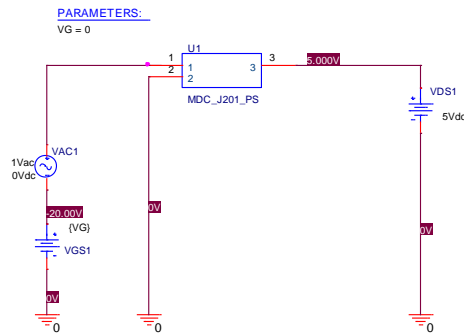
Cis Capacitance Data Sheet

VDS=5V

□ -1/((2*PI* Frequency)* IMG(1/I(U1:1)))
VG

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