

PSpice Model BRT (Bias Resistor Transistor) Isahaya RT1N14HC

Model Information

 Model
 A macro model based on Gummel-Poon model

 Call Name
 MDC_RT1N14HC_PS

 Pin Assign
 1:B 2:E 3:C

 File List
 Model Library
 MDC_RT1N14HC_PS01.lib

 Model Report
 MDC_RT1N14HC_PS.pdf (this file)

Verified Simulator Version Note

PSpice version 17.2

References

The information which was used for modeling is as follow:

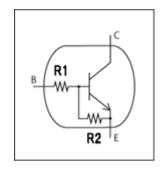
[Data Sheet]
Date/Version
Product name
Company name
Characteristics

2016.11 RT1N14HC Isahaya Electronics Corporation HFEICTEMP,VIONICTEMP,ICVIOFFTEMP,VCESATICTEM P,FTIEVCE

Simulation Range

This table shows the range of evaluated simulation range that was not occurs any convergence problems in this area.

Item	Range			Unit
	Min.		Max.	
Collector-emitter voltage (DC)	0	to	50	V
R1	10	to	10	kOhm
R2	5	to	5	kOhm
Temperature	-55	to	150	deg C



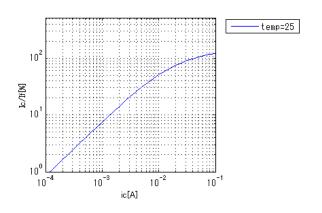
Modech

BRT		O : Implemented × : Not Implemented — : Not applicable	
Model Functions Table	RANK=1		
Functions	RANK	Implemented	
VIN(on)-Iout(Temp)	1	0	
Iout-VIN(off)(Temp)	1	0	
Iout-Vo-Iin	1	—	
DC_Current_Gain-Iout	1	0	
VOUT(on)-Iout(Temp)	1	—	
VOUT(sat)-Iin(Temp)	1	0	
Capacitance	1	—	
Transition Frequency	1	0	
Switching(Typ.)	1	_	

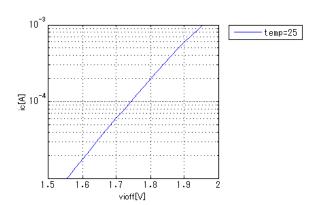


Simulation results are following. Explanatory notes -: simulated

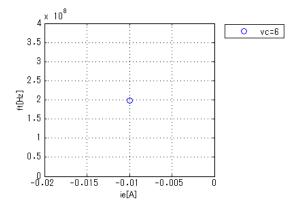
HFEICTEMP



ICVIOFFTEMP

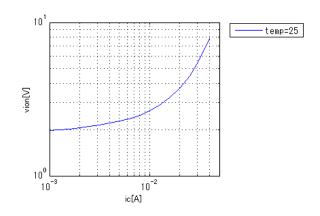


FTIEVCE

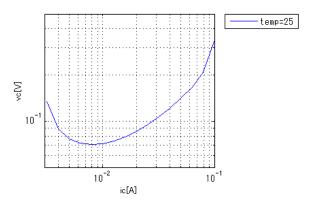


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VIONICTEMP



VCESATICTEMP





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