

LTspice Model

Switching Regulator IC for Boost Converter

NewJRC(Nisshinbo Micro Devices)

NJW4133GM1

Model Information

Model An original macro model
Call Name MDC_NJW4133GM1_LT
Pin Assign 1:SW 2:V+ 3:EN_SYNC 4:OVP 5:FB 6:RT 7:COMP 8:GND

File List Model Library MDC_NJW4133GM1_LT.lib
 Model Report MDC_NJW4133GM1_LT.pdf (this file)
Verified Simulator Version LTspice version XVII
Note

References

The information which was used for modeling is as follow:

[Data Sheet]

- Date/Version 01.Sep.2021/Ver.2.0
- Product name NJW4133
- Company name NewJRC(Nisshinbo Micro Devices)

[Characteristics listed]

- Characteristics Frequency-RT
UVLO

Simulation Condition

This table shows the range of evaluated simulation range that was not occurs any convergence problems in this area.

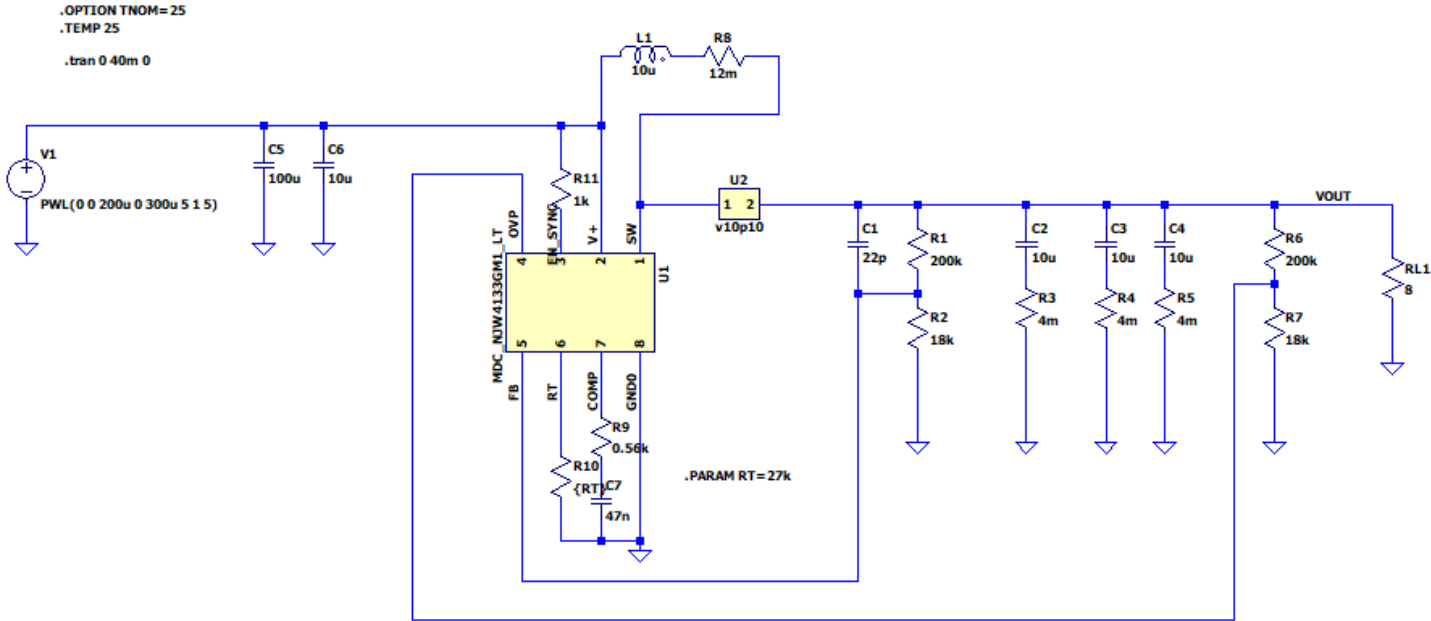
Item	Condition	Unit
Temperature	25	deg C

○ : Implemented
× : Not Implemented
— : Not applicable

Model Functions Table
RANK=1

Functions	RANK	Implemented
Control Method(PWM,PFM)	1	—
Enable Function	1	○
Soft Start	1	○
Line Regulation	1	—
Load Regulation	1	—
Variable OSC Frequency	1	○
UVLO	1	○
Line Transient	2	—
Load Regulation	2	—
Light Load Current Mode	2	—
Spread Spectrum	2	—
Over Current Protection	2	×
Over Voltage Protection	2	×
Forward/Flyback Other Device in Circuit	3	—
Brown IN/OUT Function	—	—
ZT Pin OVP Function	—	—

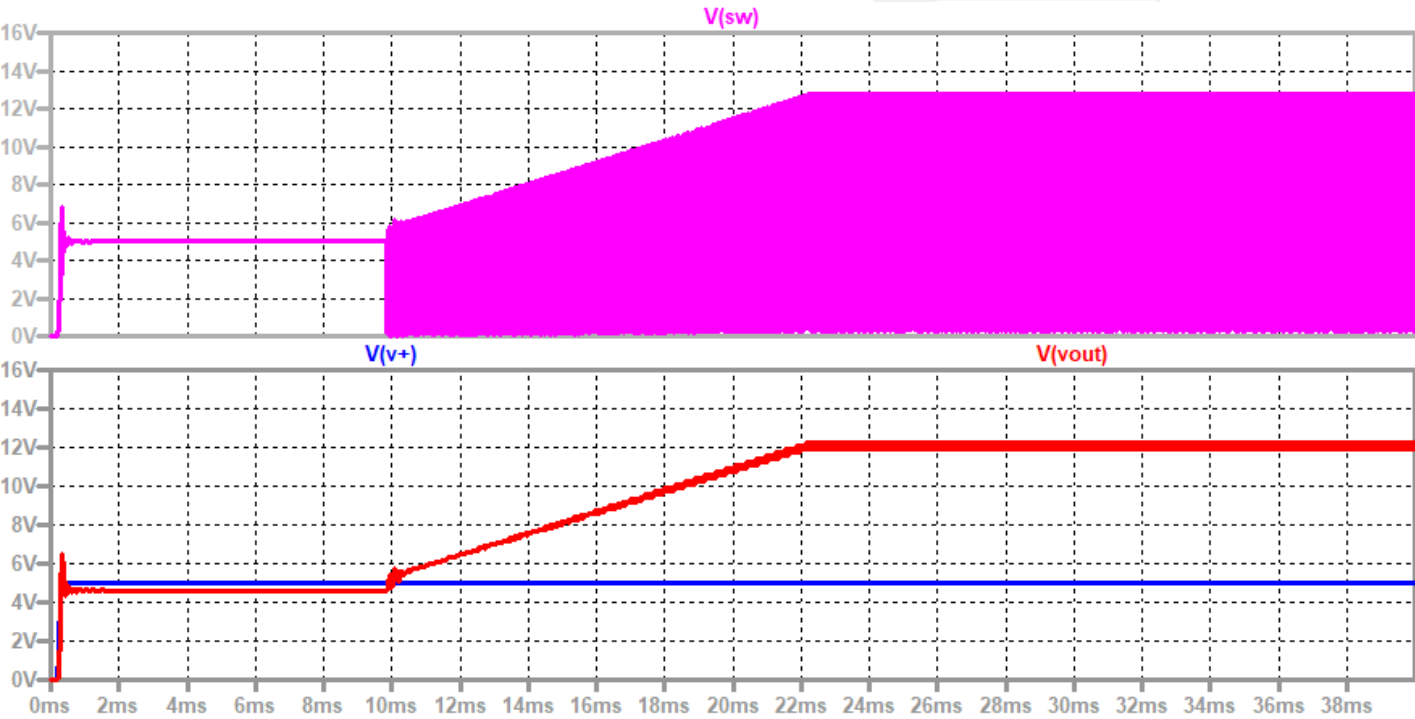
Frequency-RT Testbench
Referred to Data Sheet



Simulation results are following.
Explanatory notes — : simulated

Diff(Cursor2 - Cursor1)	
Horz:	9.9282297us
Freq:	100.72289KHz

Frequency-RT .PARAM RT=82k

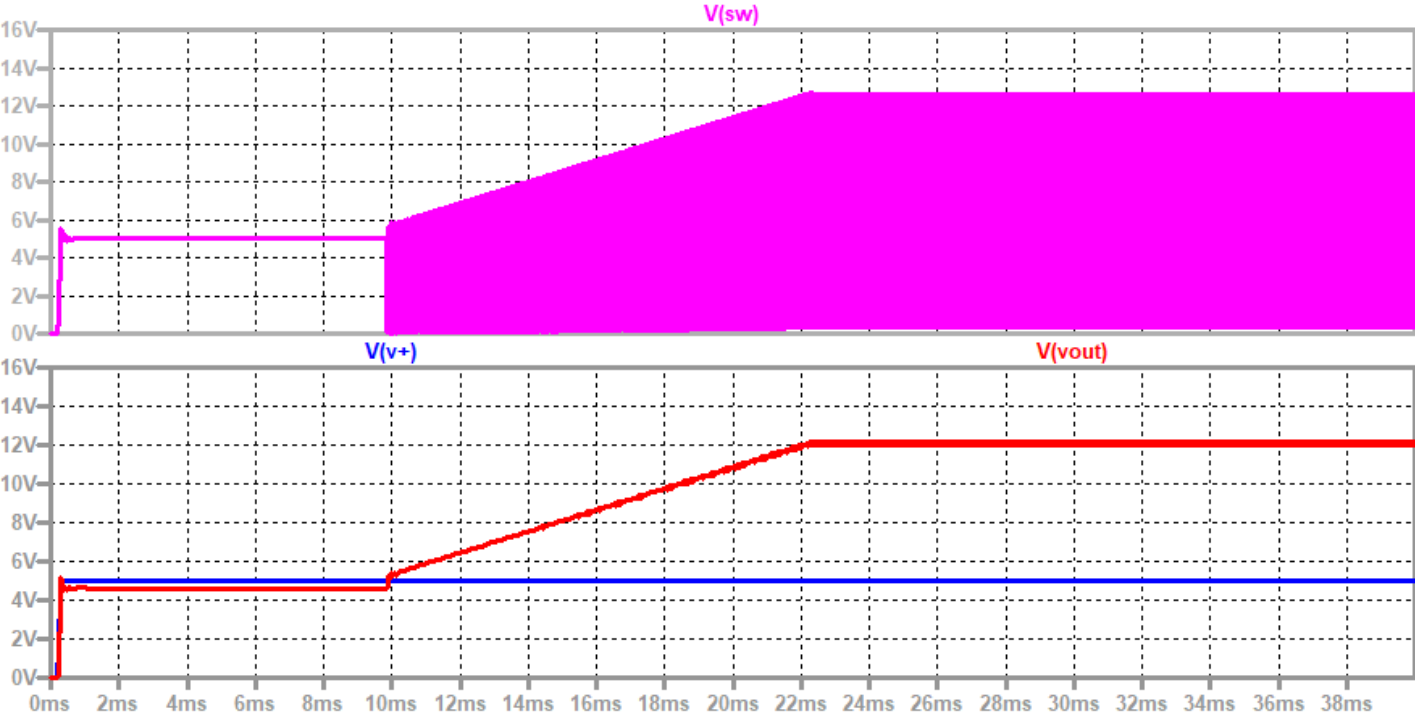


Simulation results are following.
Explanatory notes — : simulated

Diff (Cursor2 - Cursor1)	
Horz:	3.2535885us
Freq:	307.35294KHz

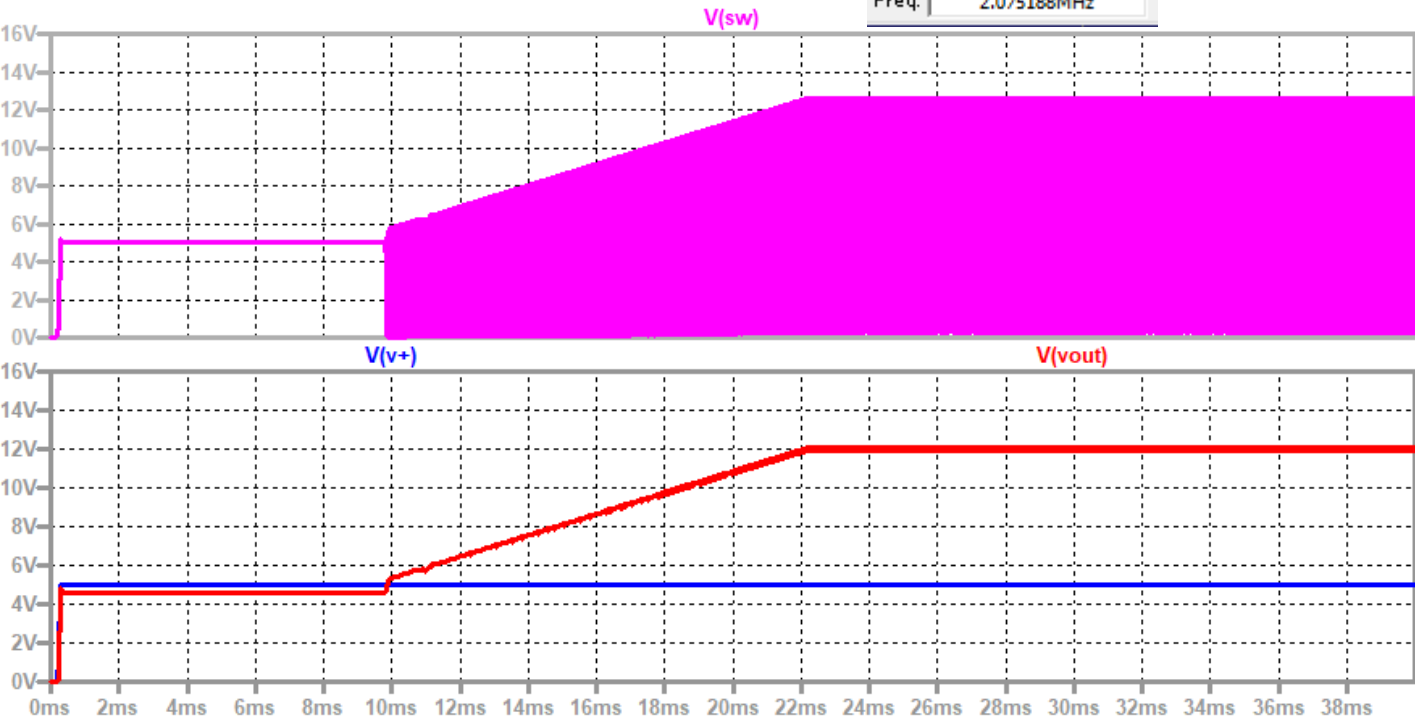
Frequency-RT

.PARAM RT=27k



.PARAM RT=2.32k

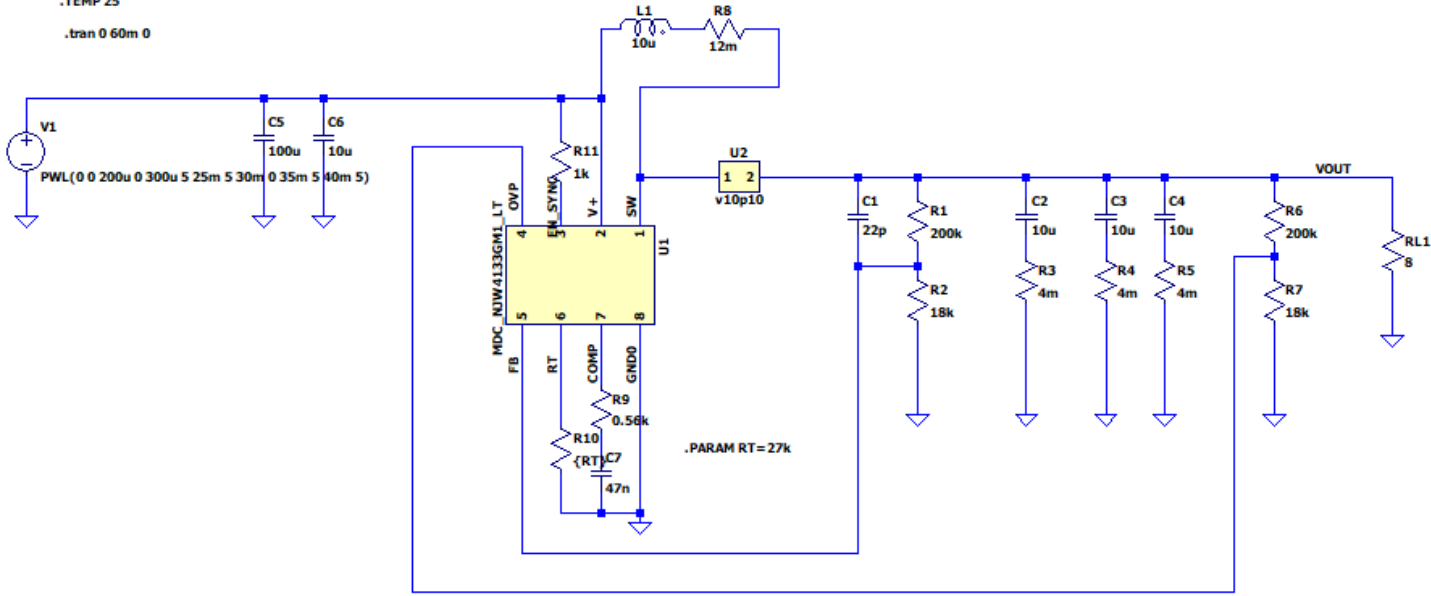
Diff (Cursor2 - Cursor1)	
Horz:	481.88406ns
Freq:	2.075188MHz



UVLO Testbench

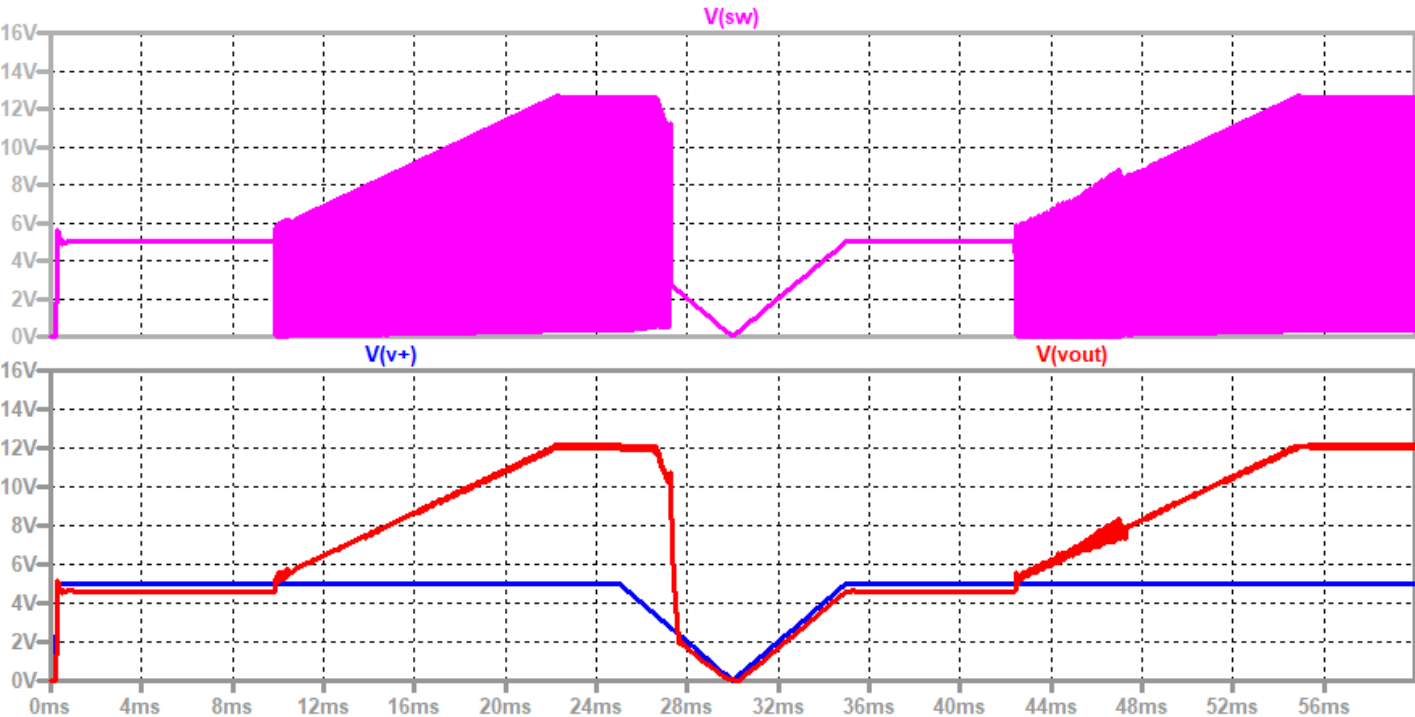
Referred to Data Sheet

```
.OPTION TNOM=25
.TEMP 25
.tran 0 60m 0
```



Simulation results are following.
 Explanatory notes — : simulated

UVLO



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