



LTspice Model NMOS Infineon IAUC120N04S6N009

Model Information

Model Call Name	A macro model based or MDC_IAUC120N04S6N0		
Pin Assign	1:S 2:S 3:S 4:G 5:D 6:D	7:D 8:D	
-	Model Library Model Report	MDC_IAUC120N04S6N009_LT01.lib MDC_IAUC120N04S6N009_LT.pdf (this file	e)

Verified Simulator Version Note

LTspice version XVII

References

The information which was used for modeling is as follow:

[Data Sheet]	•
Date/Version	2018-09-27 Rev. 1.0
Product name	IAUC120N04S6N009
Company name	Infineon Technologies AG
Characteristics	IdVds[Vgs],Rds(on)Id[Vgs],IdVgs[Temp],Rds(on)Temp[Id],Vt
	hTemp[Id],Ciss,Coss,Crss,IsVsd[Temp],VgsQg[Vdd],tdon,td
	off,tf,tr,trr,qrr

Simulation Range

This table shows the range of evaluated simulation range that was not occurs any convergence problems in this area.

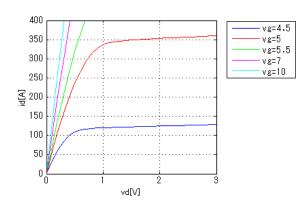
Item	Range			Unit
	Min.		Max.	
Drain-source voltage (DC)	0	to	40	V
Gate-source voltage (DC)	0	to	20	V
Temperature	-55	to	175	deg C



Simulation results are following. Explanatory notes -: simulated

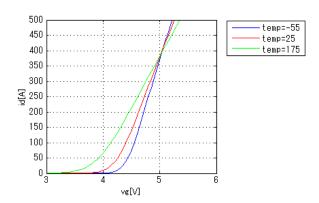
ldVds[Vgs]

Temp. = 25deg C



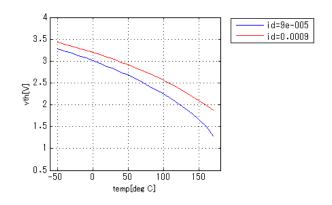
ldVgs[Temp]

Vds = 6V



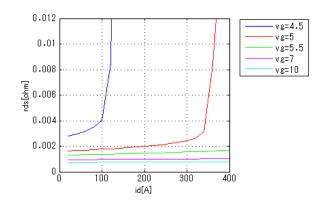
VthTemp[Id]

Vd = Vg



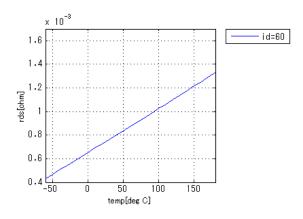
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Rds(on)Id[Vgs]

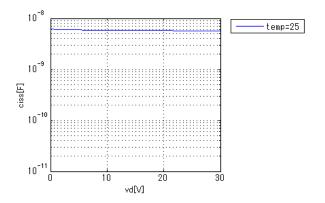


Rds(on)Temp[Id]

Vgs = 10V



Ciss Freq. = 1MHz

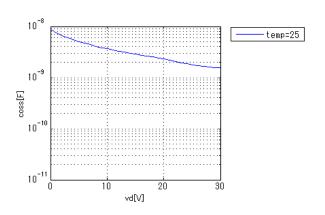




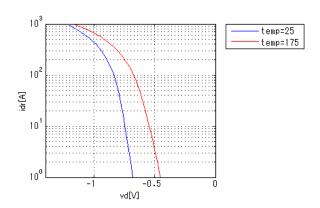
Simulation results are following. Explanatory notes — : simulated

Coss



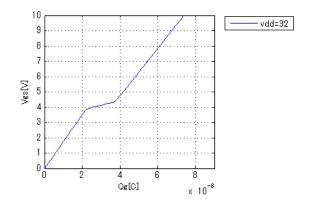


IsVsd[Temp]



VgsQg[Vdd]

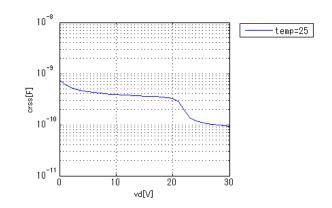
Id = 40A



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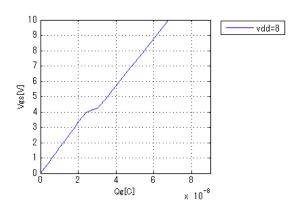
Crss

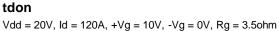
Freq. = 1MHz

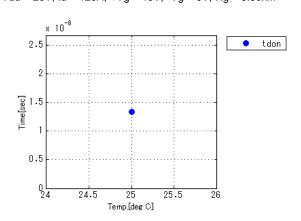


VgsQg[Vdd]

ld = 40A





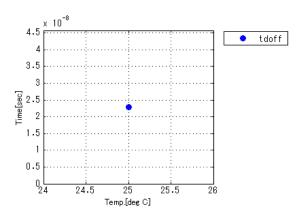




Simulation results are following. Explanatory notes — : simulated

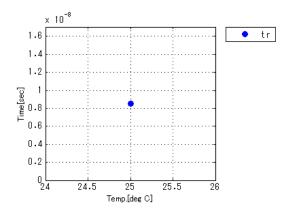
tdoff

Vdd = 20V, Id = 120A, +Vg = 10V, -Vg = 0V, Rg = 3.5ohm



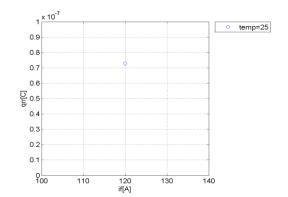
tr

Vdd = 20V, Id = 120A, +Vg = 10V, -Vg = 0V, Rg = 3.5ohm





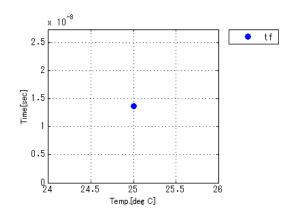
ir=2.43A



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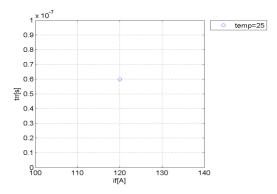
tf

Vdd = 20V, Id = 120A, +Vg = 10V, -Vg = 0V, Rg = 3.5ohm



trr

ir=2.43A





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