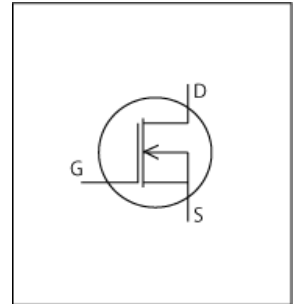


LTspice Model

NMOS

Infineon

IRFU4510PBF



Model Information

Model A macro model based on BSIM3 model
Call Name MDC_IRFU4510PBF_LT
Pin Assign 1:D 2:G 3:S
File List Model Library MDC_IRFU4510PBF_LT01.lib
 Model Report MDC_IRFU4510PBF_LT.pdf (this file)

Verified Simulator Version LTspice version XVII
Note

References

The information which was used for modeling is as follow:

[Data Sheet]

- Date/Version 05/02/12
- Product name IRFU4510PBF
- Company name Infineon Technologies AG
- Characteristics IdVds[Vgs], IdVds[Vgs]02, IdVgs[Temp], Rds(on)Temp[Id], CapacitanceVds[Cname], VgsQg[Vdd], IsVsd[Temp], BvTemp[ir], VthTemp[Id], SwitchingIdd[Tname], Trrlf[Ir], Qrrlf[Ir], SwitchingWaveform, TrrQrrWaveform

Simulation Range

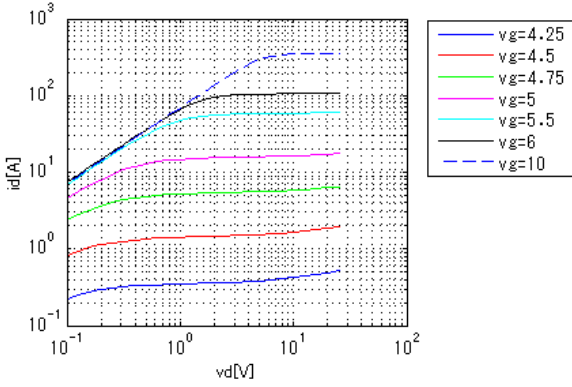
This table shows the range of evaluated simulation range that was not occurs any convergence problems in this area.

Item	Range			Unit
	Min.		Max.	
Drain-source voltage (DC)	0	to	100	V
Gate-source voltage (DC)	-20	to	20	V
Temperature	-55	to	175	deg C

Simulation results are following.
 Explanatory notes — : simulated

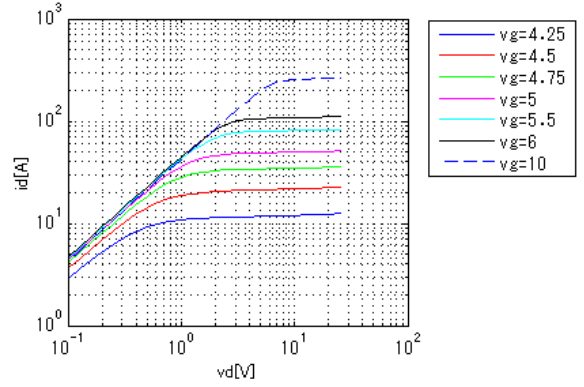
IdVds[Vgs]

Temp. = 25degC



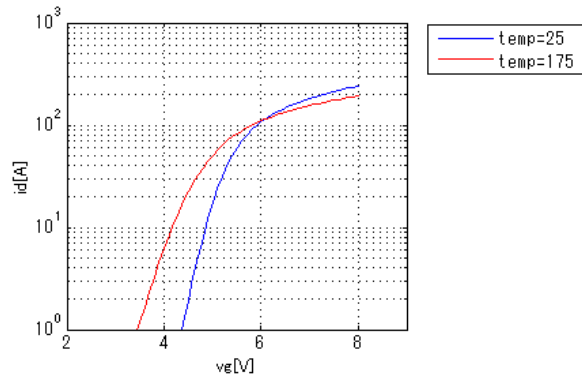
IdVds[Vgs]02

Temp. = 175degC



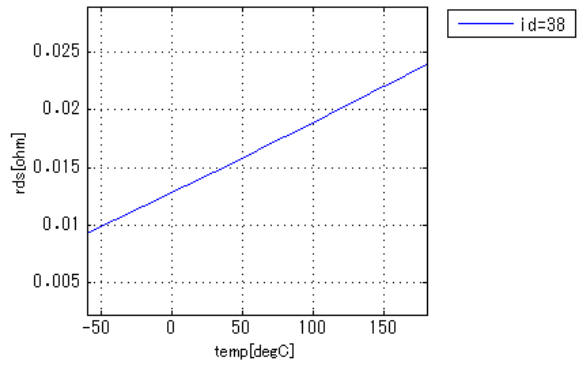
IdVgs[Temp]

Vds = 25V



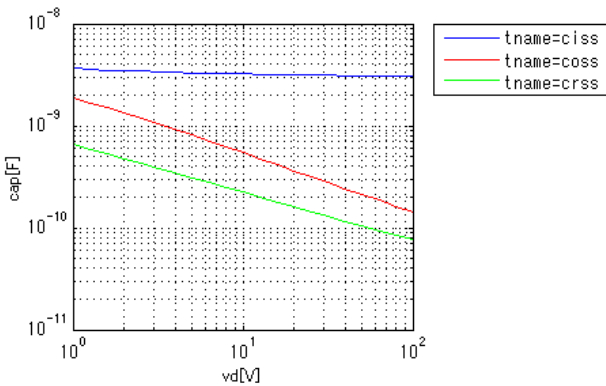
Rds(on)Temp[Id]

Vgs = 10V



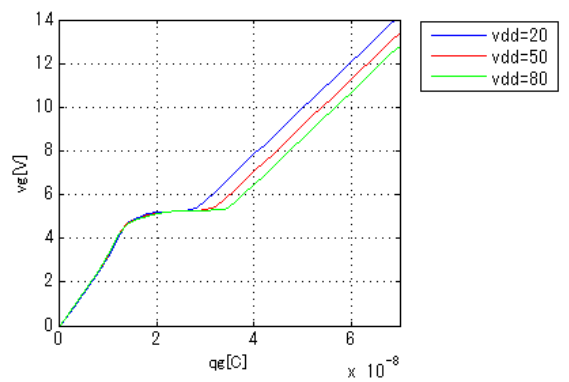
CapacitanceVds[Cname]

freq = 1000000Hz



VgsQg[Vdd]

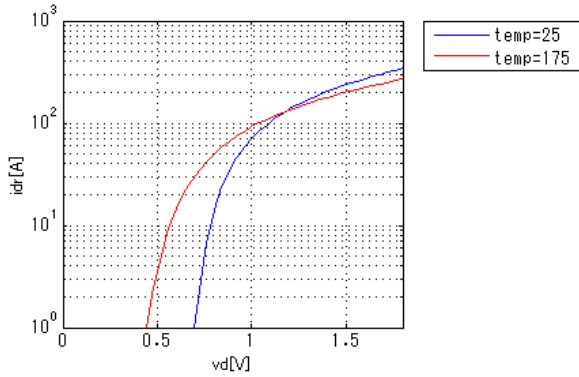
Id = 38A



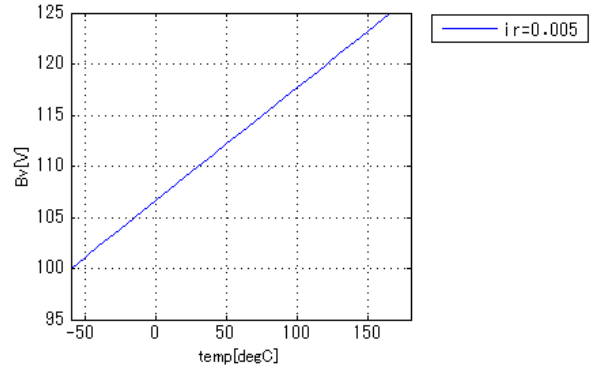
Simulation results are following.
 Explanatory notes — : simulated

IsVsd[Temp]

vg = 0V

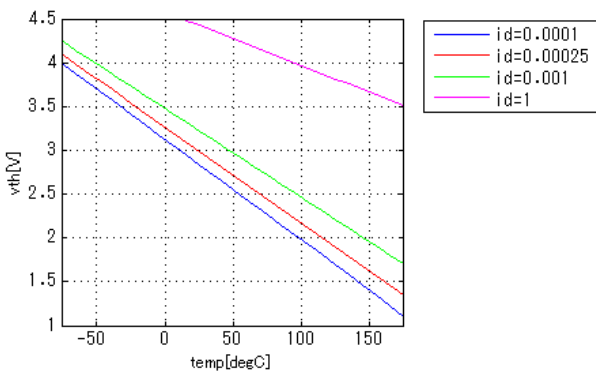


BvTemp[ir]



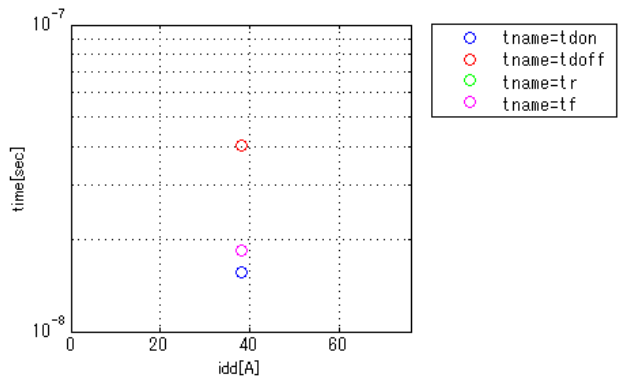
VthTemp[Id]

Vd = Vg



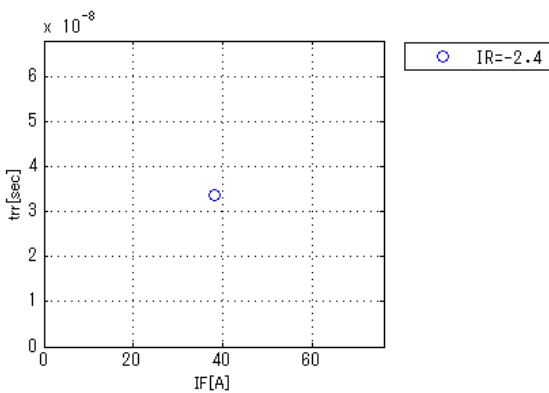
SwitchingIdd[Tname]

vgg = 10V, vdd = 65V, RGG = 7.5ohm



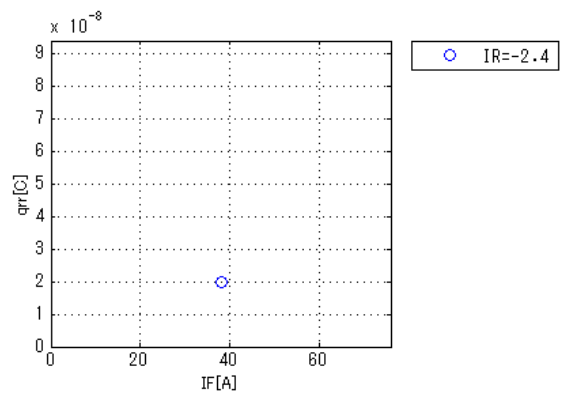
Trrlf[Ir]

vdd = 86V, didt = 100A/us



Qrrlf[Ir]

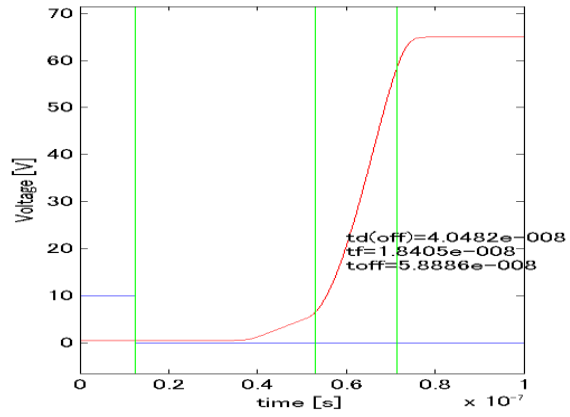
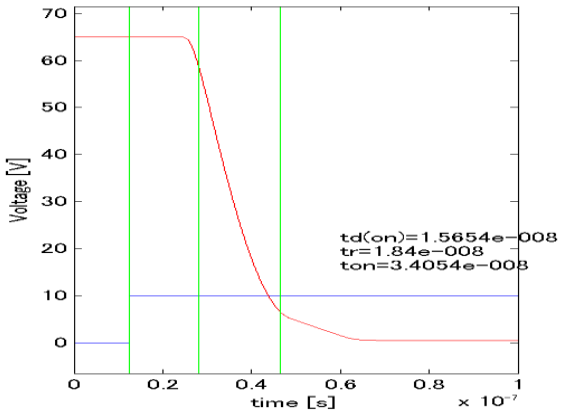
vdd = 86V, didt = 100A/us



Simulation results are following.
 Explanatory notes — : simulated

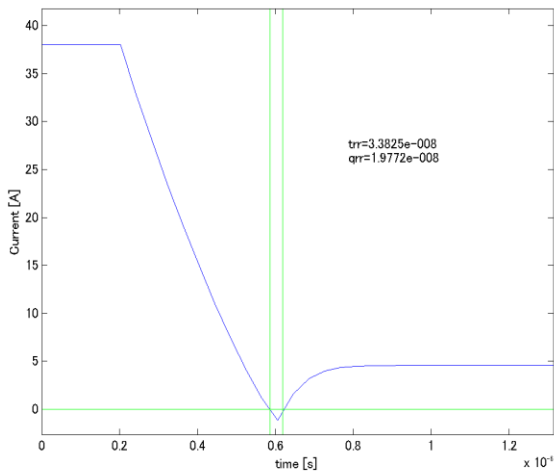
SwitchingWaveform

Blue : INPUT Red : OUTPUT



TrrQrrWaveform

vdd = 86V, didt = 100A/us



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