MoDeCH

Global Design Infrastructure Innovation

DC/DC Converter IC SPICE Model Report

Product Type：MP9942GJ

2020.01.29-J
2020.09.30-E

http://www.modech.com/

Agenda

- 1. Model Specifications
- 2. Verification Conditions
- 3. Results of Verification

1. Model Specifications

- 1.1 Supported features of the model
- 1.2 Characteristics of the model
- 1.3 Terminal definitions

1.1 Supported features of the model

Functions	Device	Model
Internal Regulator	○	○
Power Save Mode for Light Load Condition	○	○
Enable/SYNC control	○	○
Under-Voltage Lockout	○	○
Internal Soft-Start	○	○
Over-Current Protection and Hiccup	○	-
Thermal Shutdown	○	-
Floating Driver and Bootstrap Charging	○	○
Startup and Shutdown	○	○
Power Good	○	○

1.2.1 Target fitting characteristics (1)

Red rectangle shows target modeling characteristics

ELECTRICAL CHARACTERISTICS

V_{IN} = 12V, T_J = +25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Supply Current (Shutdown)	I_{SHDN}	V_{EN} = 0V			8	µA
Supply Current (Quiescent)	I_Q	V_{EN} = 2V, V_{FB} = 1V		0.5	0.7	mA
HS Switch-ON Resistance	R_{ON_HS}	V_{BST-SW}=5V		90	155	mΩ
LS Switch-ON Resistance	R_{ON_LS}	V_{CC} =5V		55	105	mΩ
Switch Leakage	I_{LKG_SW}	V_{EN} = 0V, V_{SW} =12V			1	µA
Current Limit	I_{LIMIT}	Under 40% Duty Cycle	3	4.2	5.5	A
Oscillator Frequency	f_{SW}	V_{FB}=750mV	320	410	500	kHz
Fold-Back Frequency	f_{FB}	V_{FB}<400mV	70	100	130	kHz
Maximum Duty Cycle	D_{MAX}	V_{FB}=750mV, 410kHz	92	95		%
Minimum ON Time(5)	t_{ON_MIN}			70		ns
Sync Frequency Range	f_{SYNC}		0.2		2.4	MHz
Feedback Voltage	V_{FB}		780	792	804	mV
Feedback Current	I_{FB}	V_{FB}=820mV		10	100	nA
EN Rising Threshold	V_{EN_RISING}		1.15	1.4	1.65	V
EN Falling Threshold	$V_{EN\_FALLING}$		1.05	1.25	1.45	V
EN Threshold Hysteresis	V_{EN_HYS}			150		mV
EN Input Current	I_{EN}	V_{EN}=2V		4	6	µA
		V_{EN}=0		0	0.2	µA

All fitting is done for typical and Ta=25°C

1.2.2 Target fitting characteristics (2)

Red rectangle shows target modeling characteristics

VIN Under-Voltage Lockout Threshold-Rising	$INUV_{RISING}$		3.3	3.5	3.7	V
VIN Under-Voltage Lockout Threshold-Falling	$INUV_{FALLING}$		3.1	3.3	3.5	V
VIN Under-Voltage Lockout Threshold-Hysteresis	$INUV_{HYS}$			200		mV
VCC Regulator	V_{CC}	I_{CC}=0mA	4.6	4.9	5.2	V
VCC Load Regulation		I_{CC}=5mA		1.5	4	%
Soft-Start Period	t_{SS}	V_{OUT} from 10% to 90%	0.55	1.45	2.45	ms
Thermal Shutdown (5)	T_{SD}		150	170		°C
Thermal Hysteresis (5)	T_{SD_HYS}			30		°C
PG Rising Threshold	PG_{Vth_RISING}	as percentage of V_{FB}	86.5	90	93.5	%
PG Falling Threshold	$PG_{Vth\_FALLING}$	as percentage of V_{FB}	80.5	84	87.5	%

All fitting is done for typical and Ta=25℃

1.2.3 Target fitting characteristics (3)

Red rectangle shows target modeling characteristics

ELECTRICAL CHARACTERISTICS *(continued)*

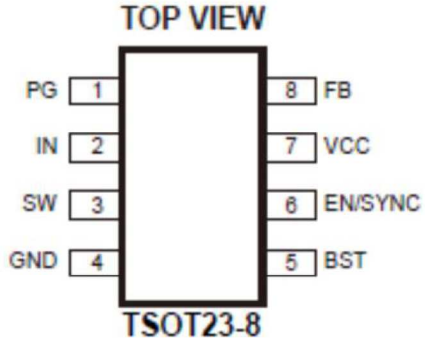
V_{IN} = 12V, T_J = +25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
PG Threshold Hysteresis	PG_{Vth_HYS}	as percentage of V_{FB}		6		%
PG Rising Delay	PG_{Td_RISING}		40	90	160	µs
PG Falling Delay	$PG_{Td\_FALLING}$		30	55	95	µs
PG Sink Current Capability	V_{PG}	Sink 4mA		0.1	0.3	V
PG Leakage Current	I_{LKG_PG}			10	100	nA

All fitting is done for typical and Ta=25℃

1.3 Terminal Conditions

PACKAGE REFERENCE



PIN FUNCTIONS

Package Pin #	Name	Description
1	PG	Power Good. The output of this pin is an open drain and goes high if the output voltage exceeds 90% of the nominal voltage.
2	IN	Supply Voltage. The MP9942 operates from a 4V to 36V input rail. Requires C1 to decouple the input rail. Connect using a wide PCB trace.
3	SW	Switch Output. Connect with a wide PCB trace.
4	GND	System Ground. This pin is the reference ground of the regulated output voltage, and PCB layout requires special care. For best results, connect to GND with copper traces and vias.
5	BST	Bootstrap. Requires a capacitor connected between SW and BST pins to form a floating supply across the high-side switch driver. A 20Ω resistor placed between SW and BST cap is strongly recommended to reduce SW spike voltage.
6	EN/SYNC	Enable/Synchronize. EN/SYNC high to enable the MP9942. Apply an external clock to the EN/SYNC pin to change the switching frequency.
7	VCC	Bias Supply. Decouple with 0.1μF-to-0.22μF capacitor. Select a capacitor that does not exceed 0.22μF
8	FB	Feedback. Connect to the tap of an external resistor divider from the output to GND, to set the output voltage. The frequency fold-back comparator lowers the oscillator frequency when the FB voltage is below 660mV to prevent current limit runaway during a short-circuit fault condition.

2. Verification Conditions

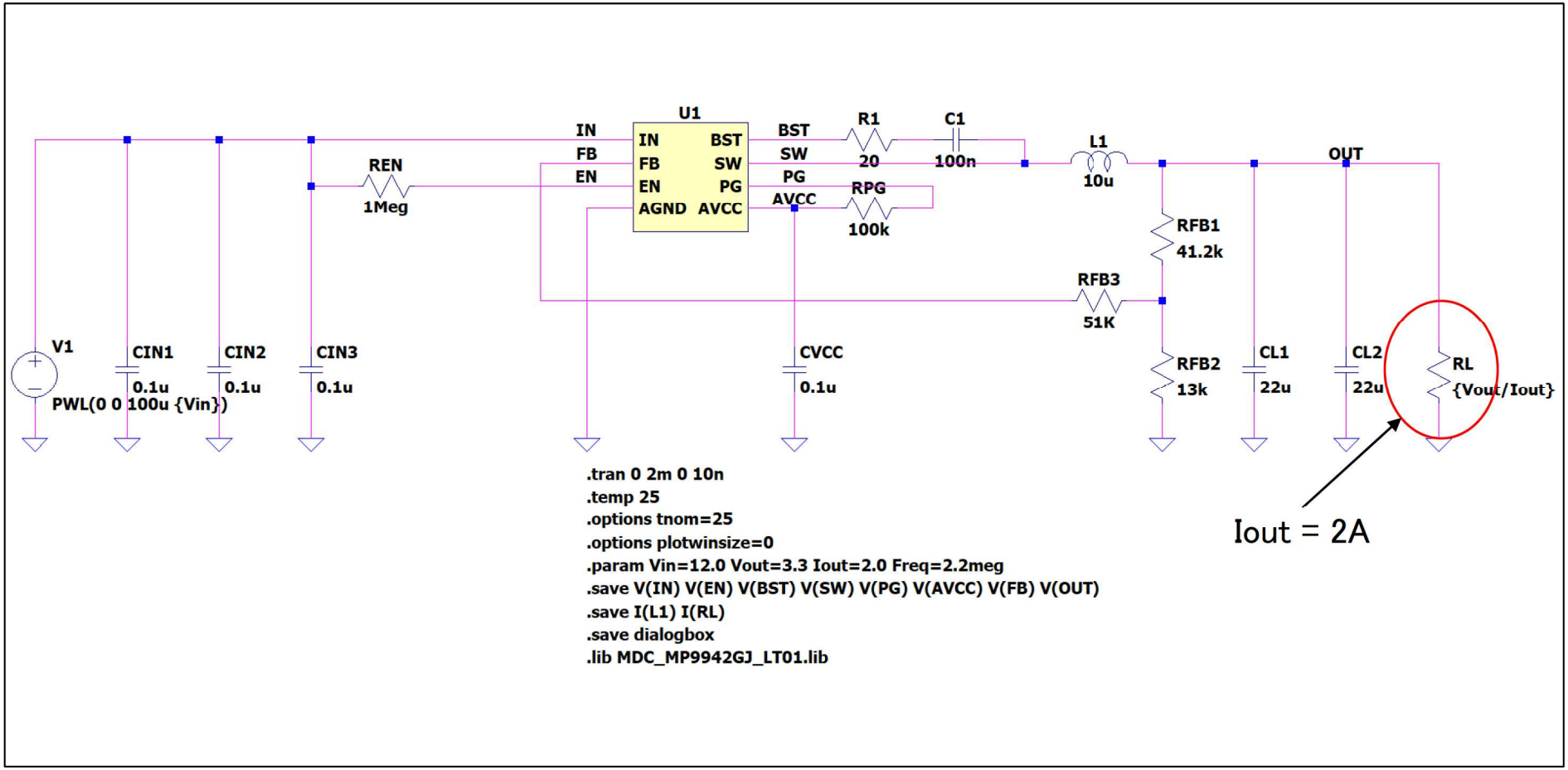
- Supported Simulator
  - LTspice XVII

- TNOM
  - 25℃

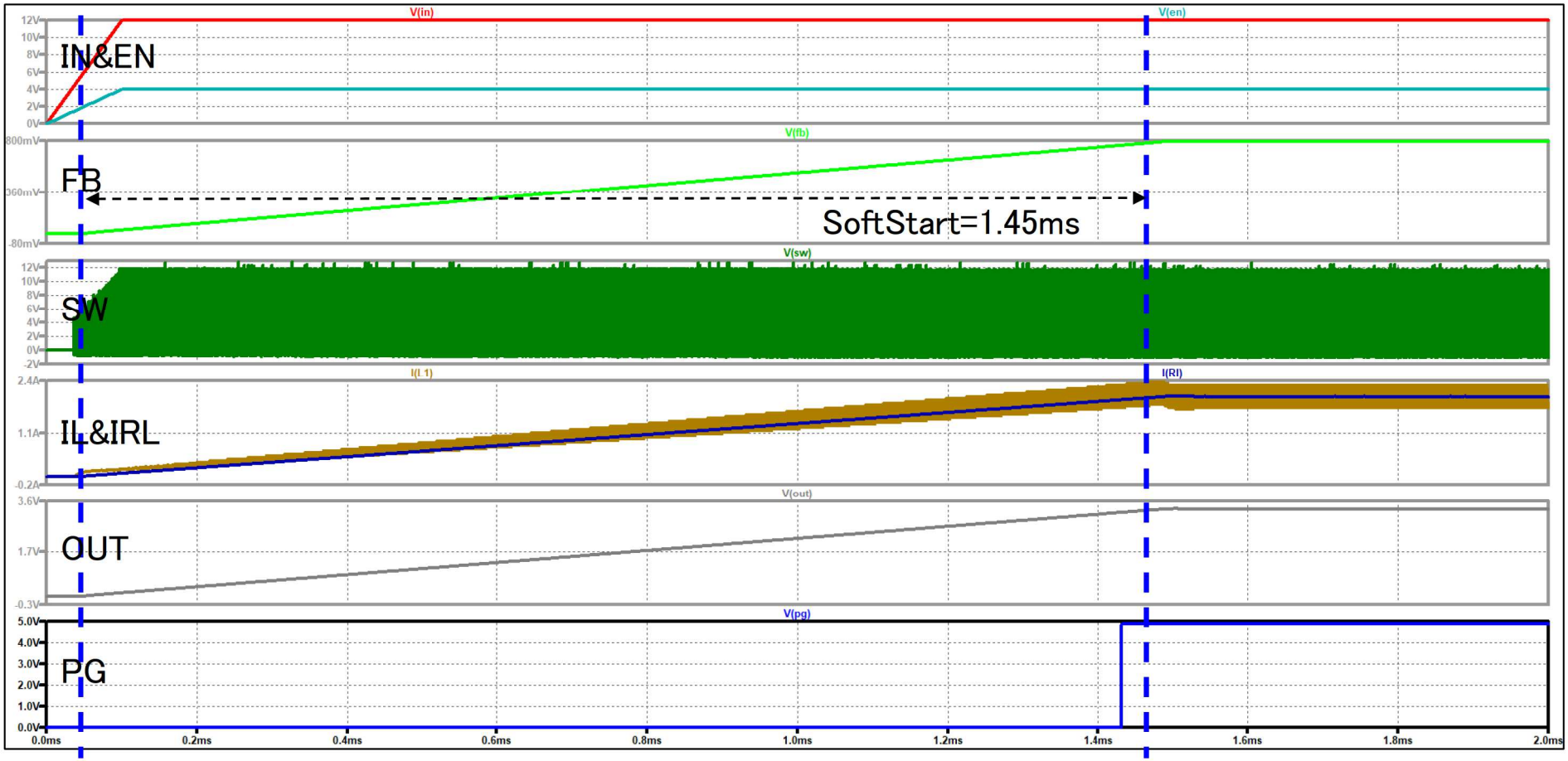
3. Result of Verifications

- 3.1 Normal Mode Operation
- 3.2 Internal Power-Save Mode
- 3.3 Synchronizes External Clock
- 3.4 UVLO
- 3.5 EN
- 3.6 Line Regulation
- 3.7 Load Regulation

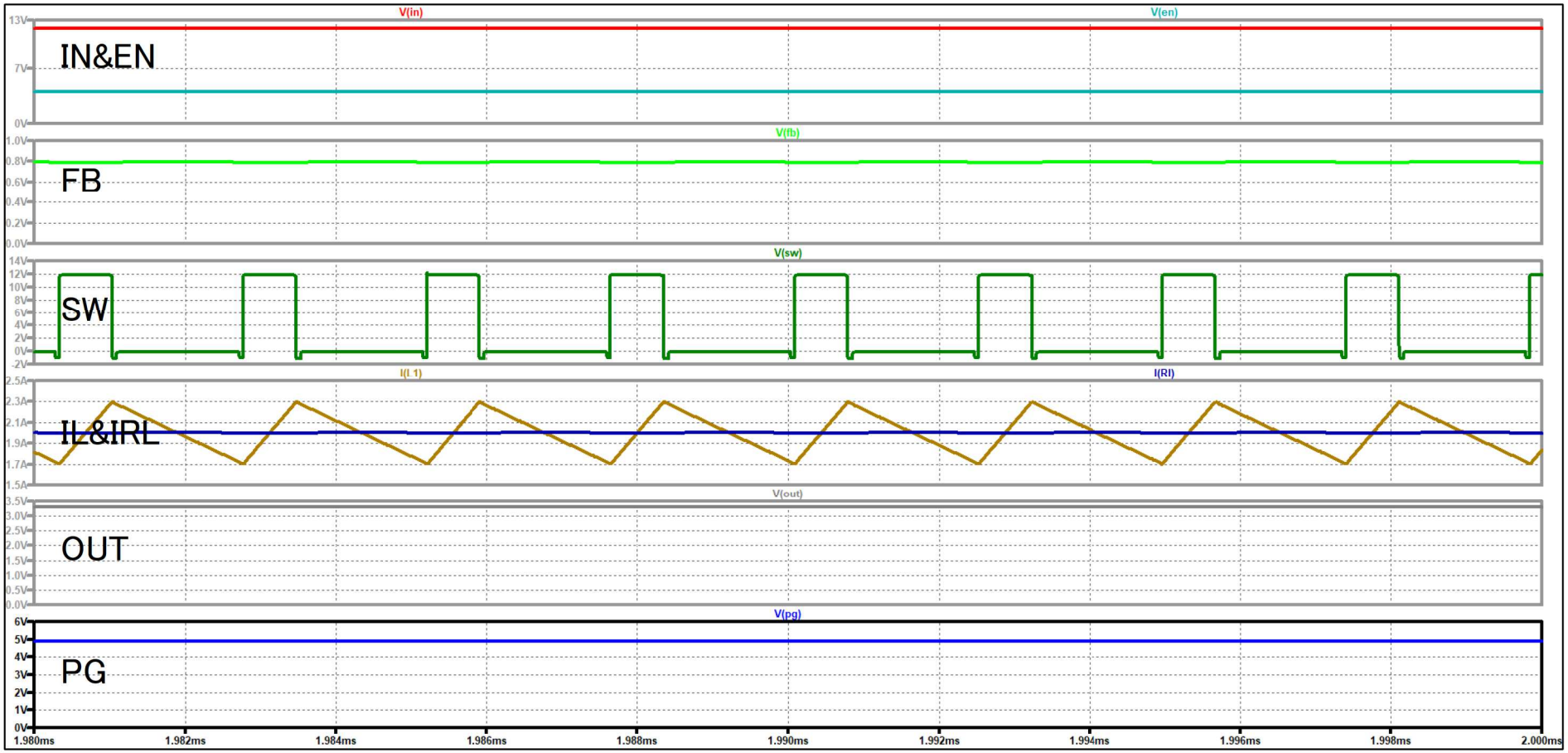
3.1.1 Normal Mode Operation



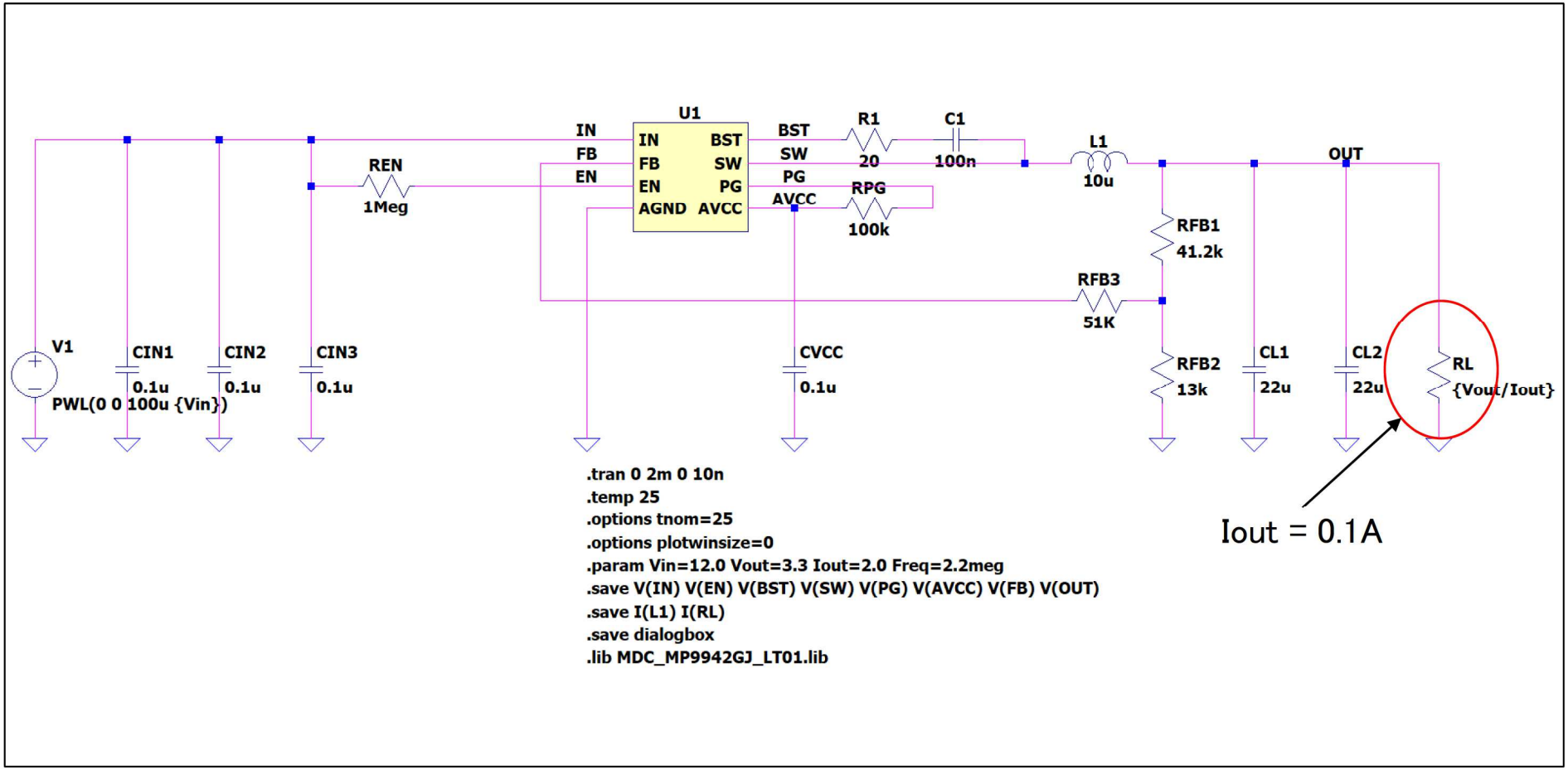
3.1.2 Normal Mode Operation (Startup)



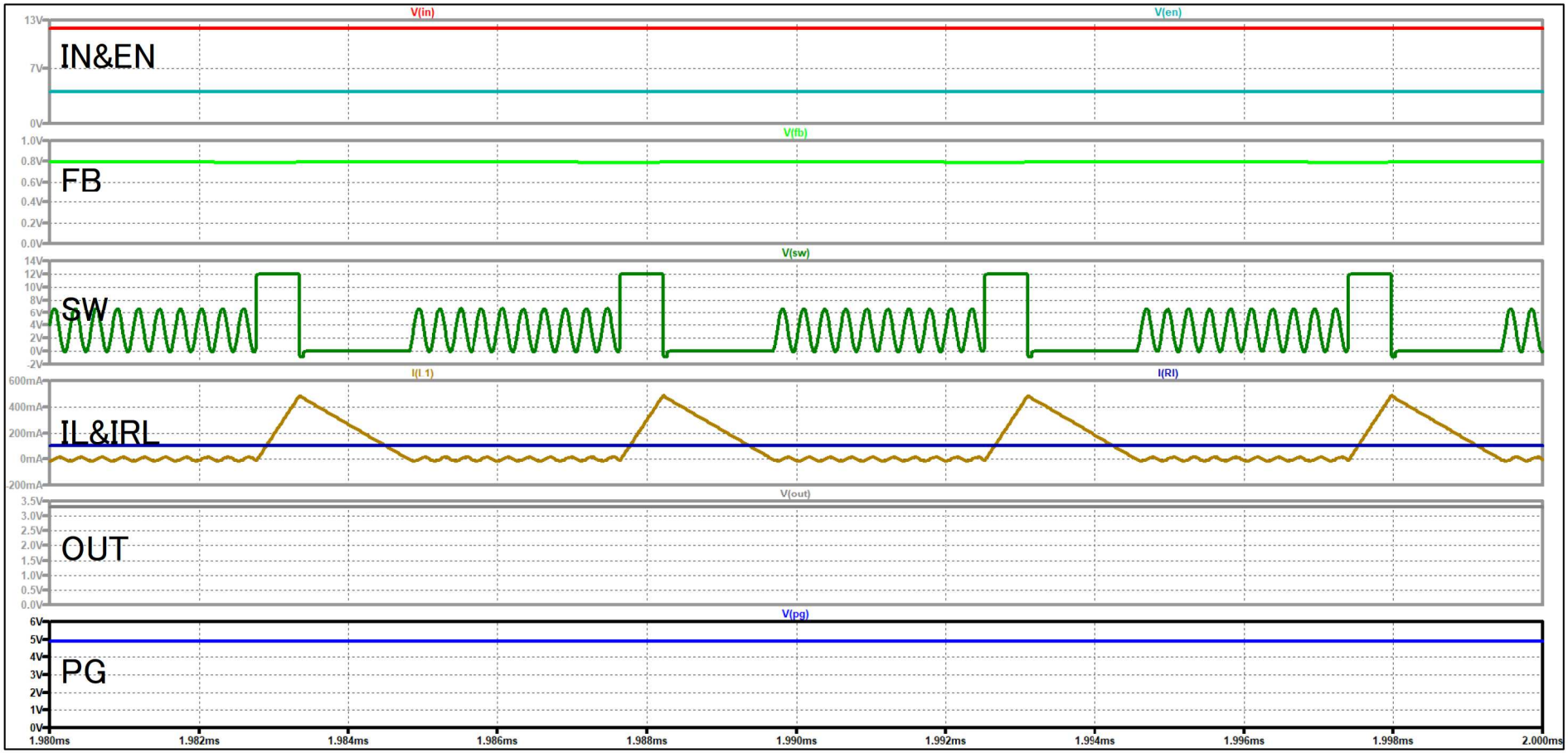
3.1.3 Normal Mode Operation (Steady State)



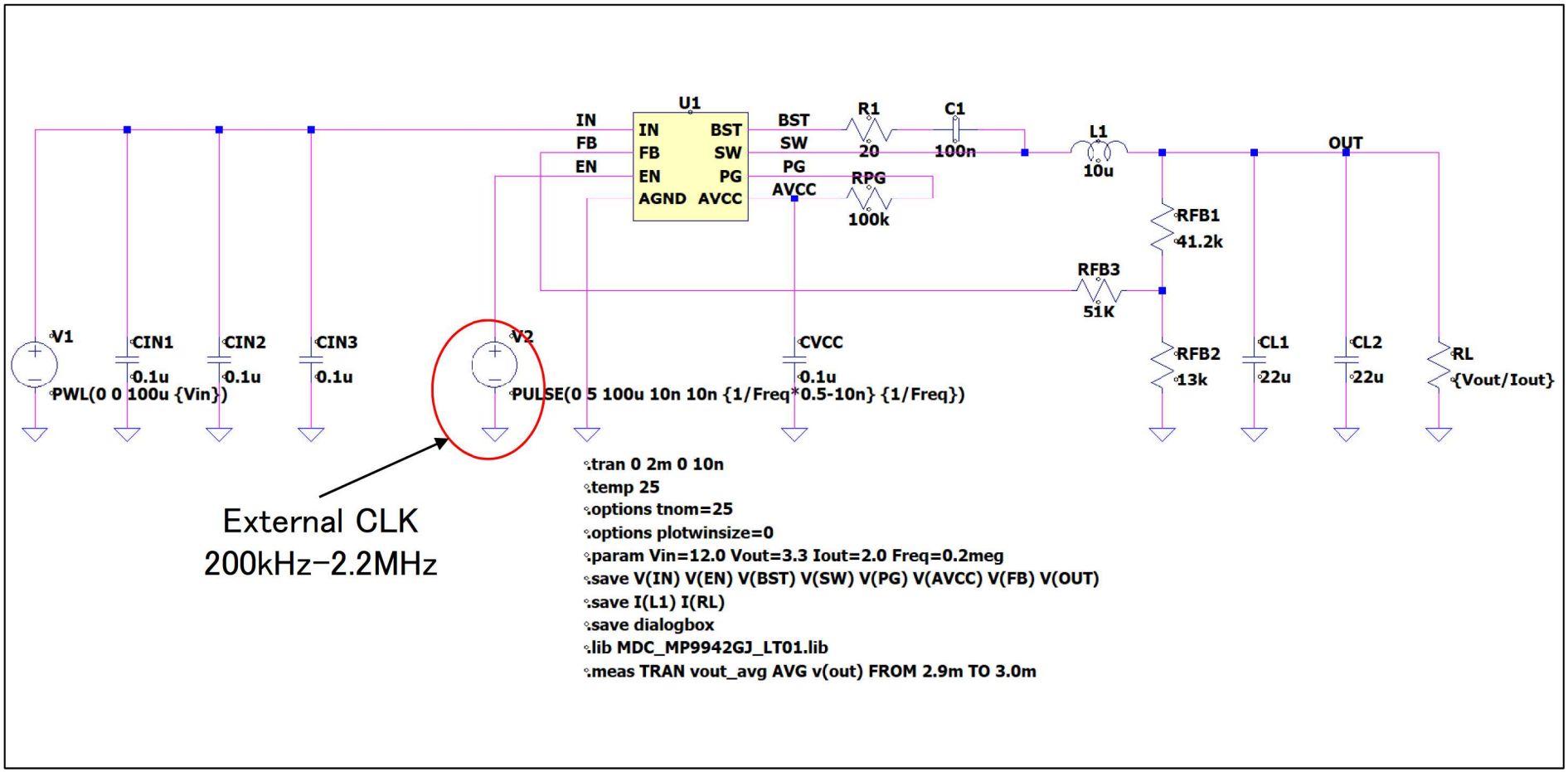
3.2.1 Internal Power-Save Mode



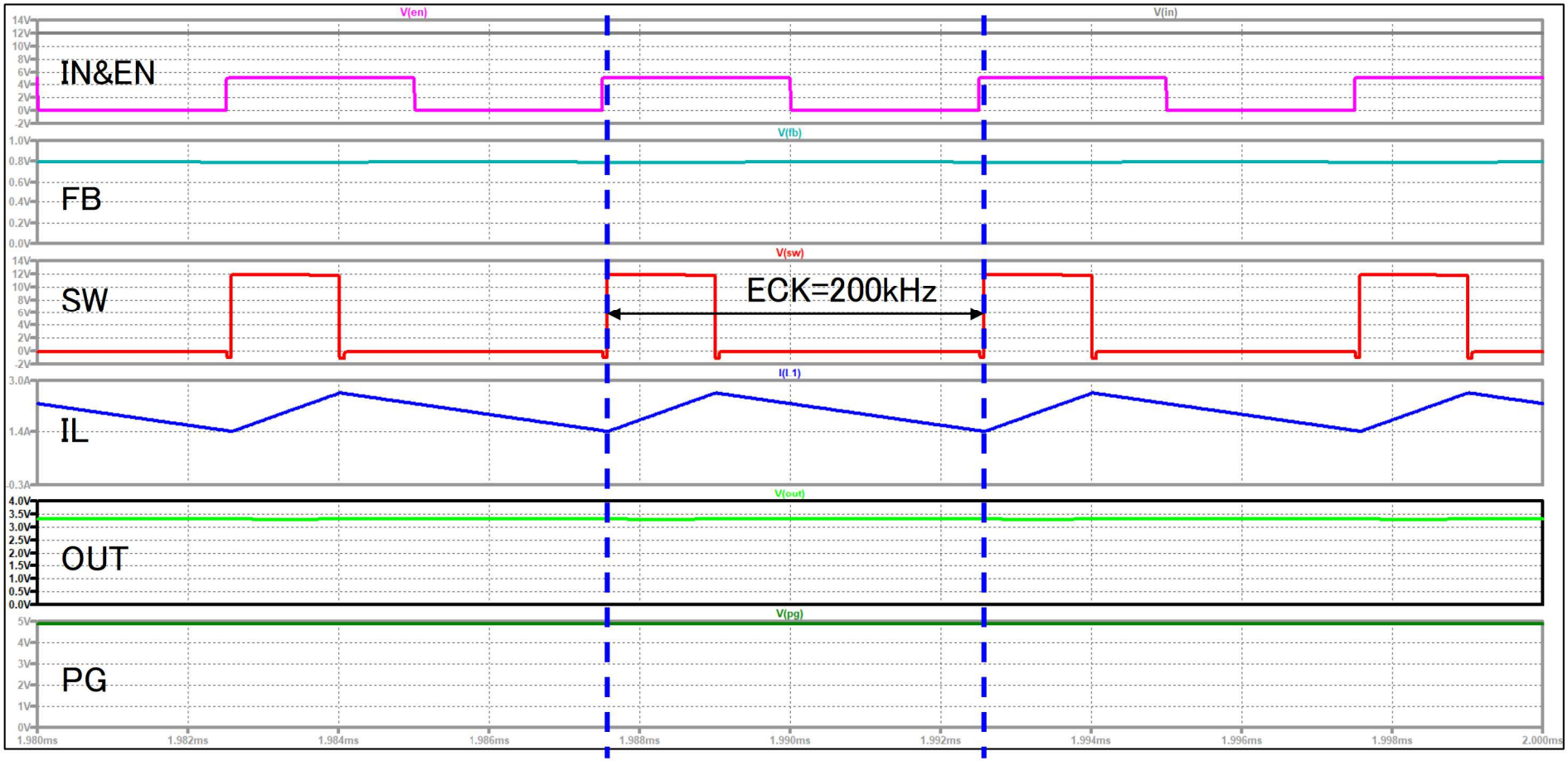
3.2.2 Internal Power-Save Mode



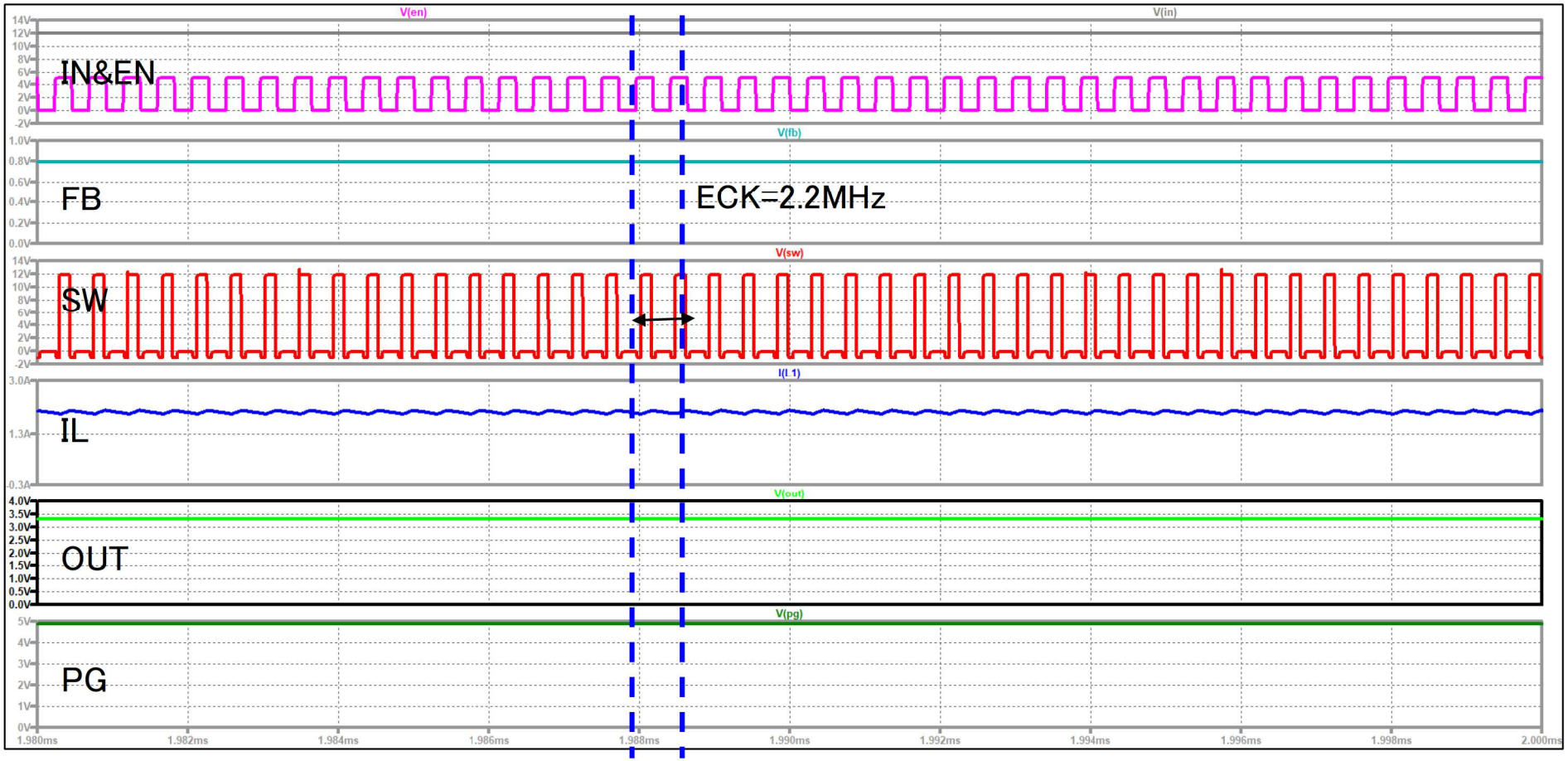
3.3.1 Synchronizes External Clock



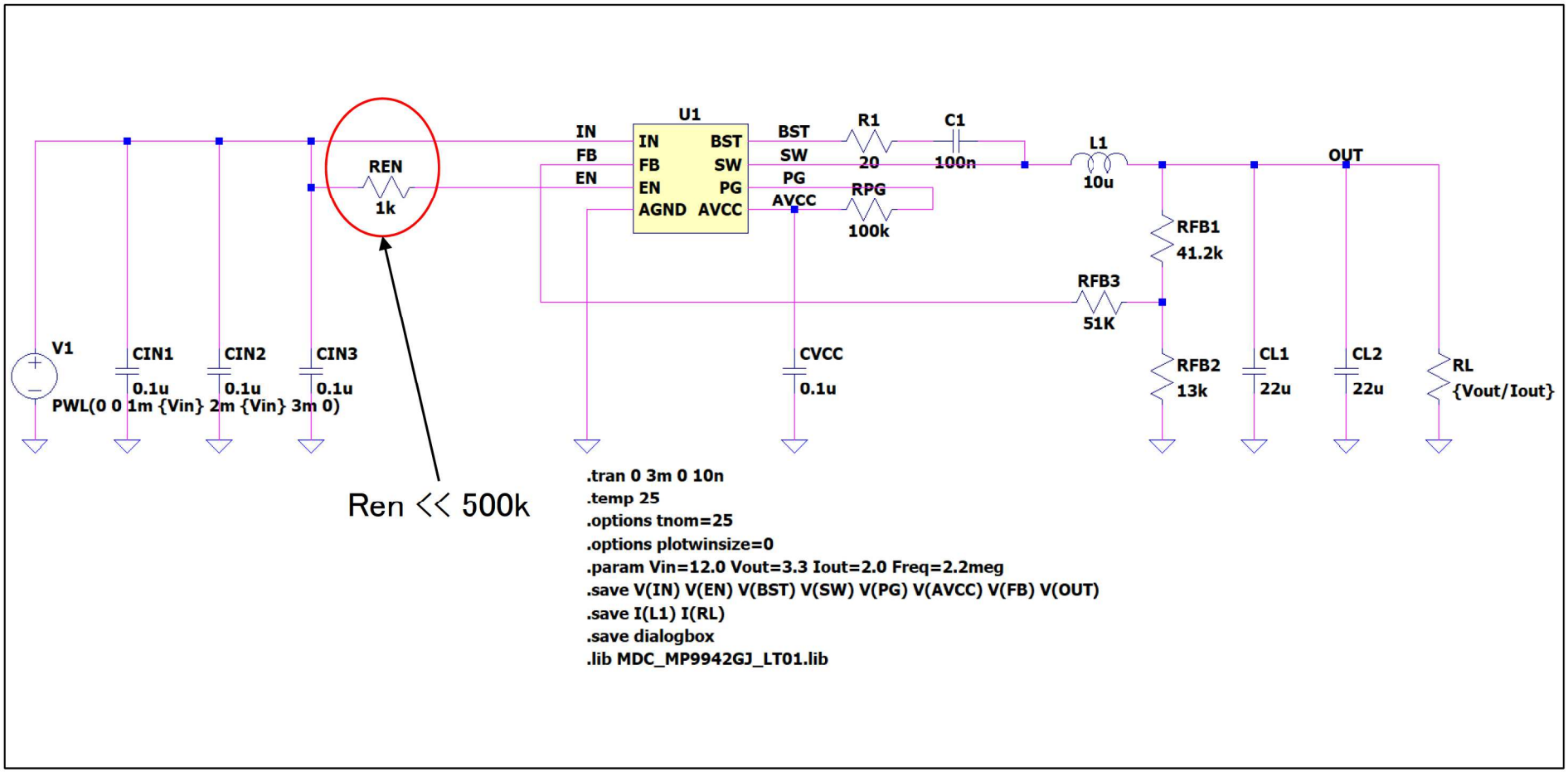
3.3.2 Synchronizes External Clock (ECK=200kHz)



3.3.3 Synchronizes External Clock (ECK=2.2MHz)

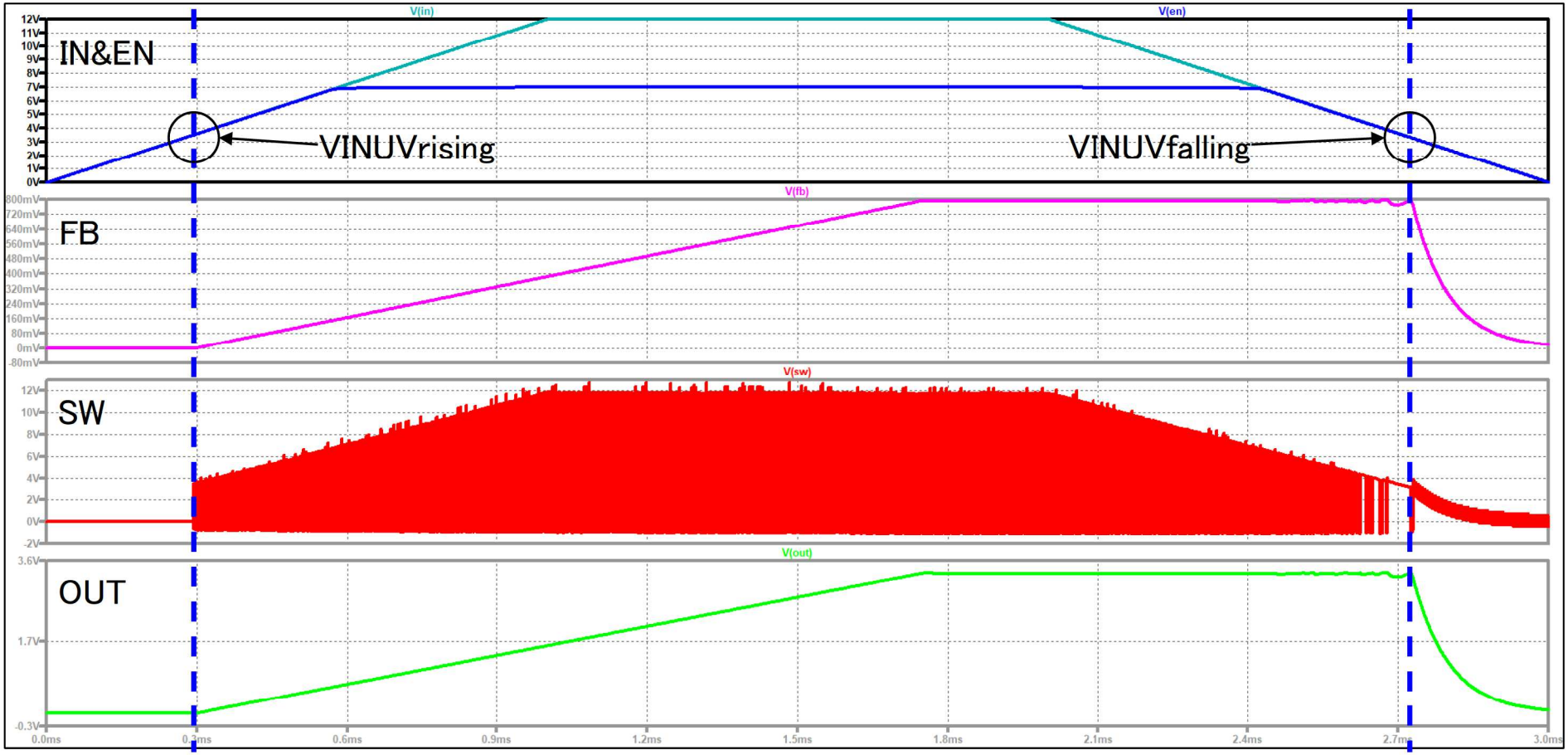


3.4.1 UVLO

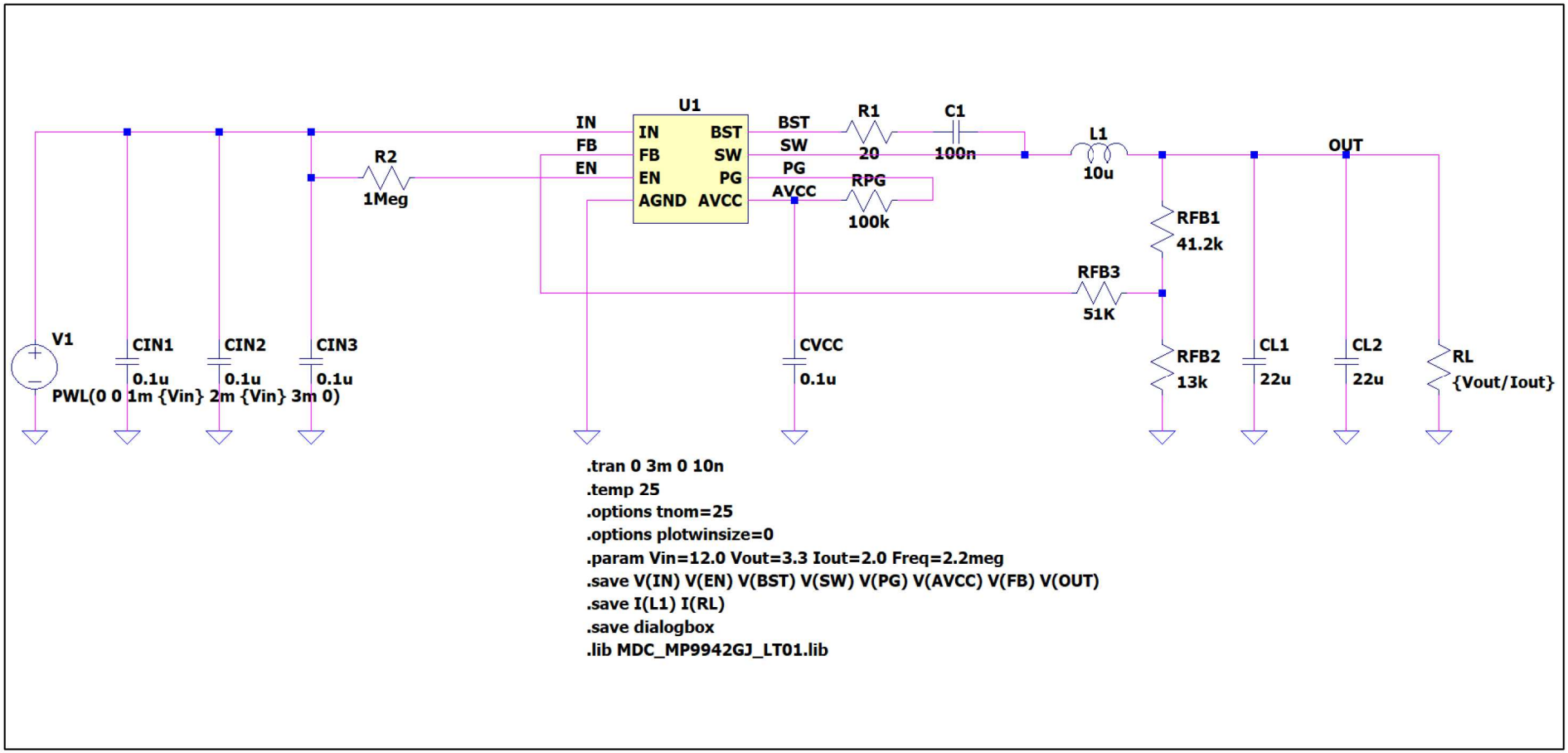


3.4.2 UVLO

Item	Datasheet	Model
INUVrising	3.5	3.5
INUVfalling	3.3	3.3

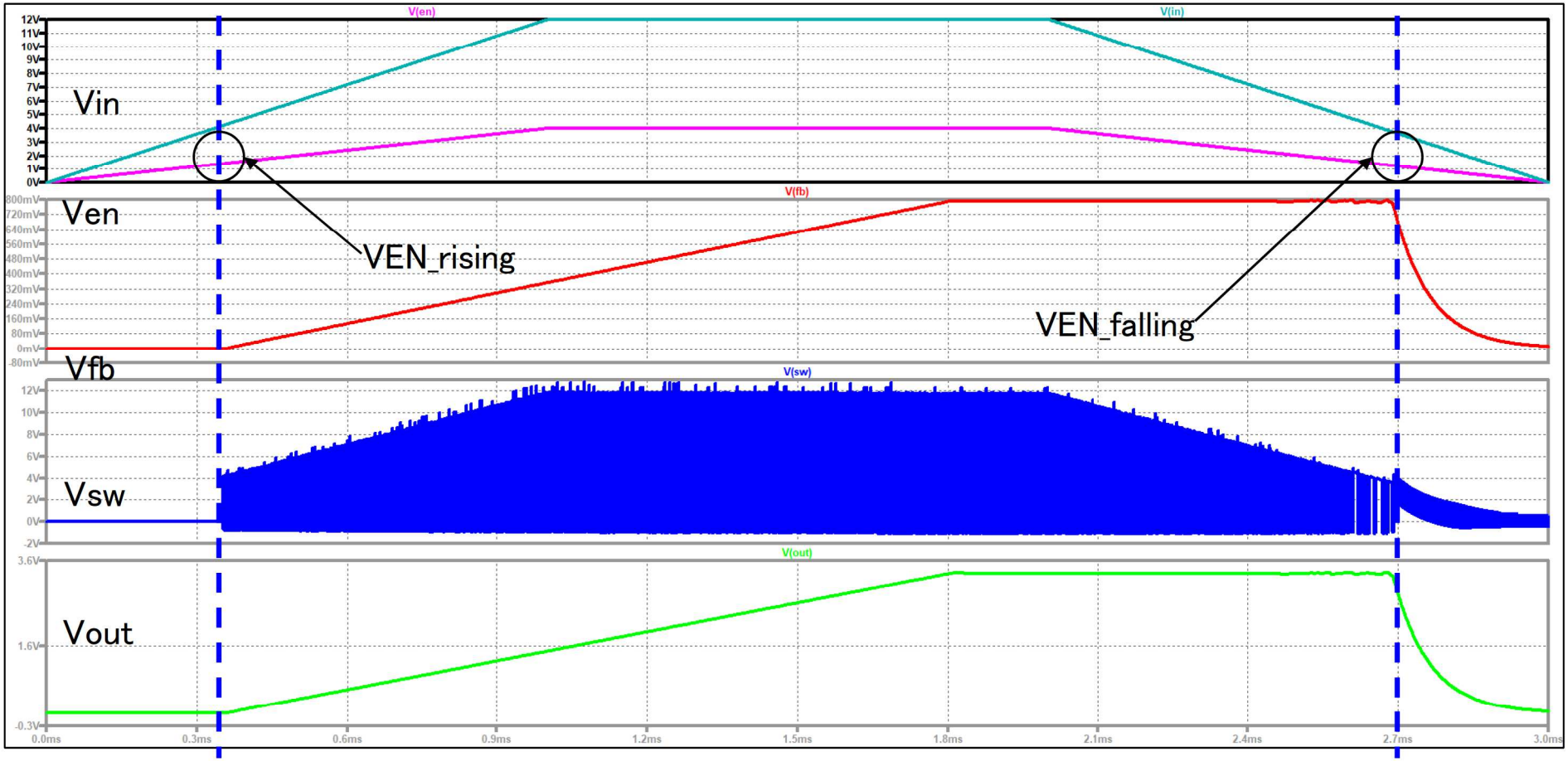


3.5.1 EN

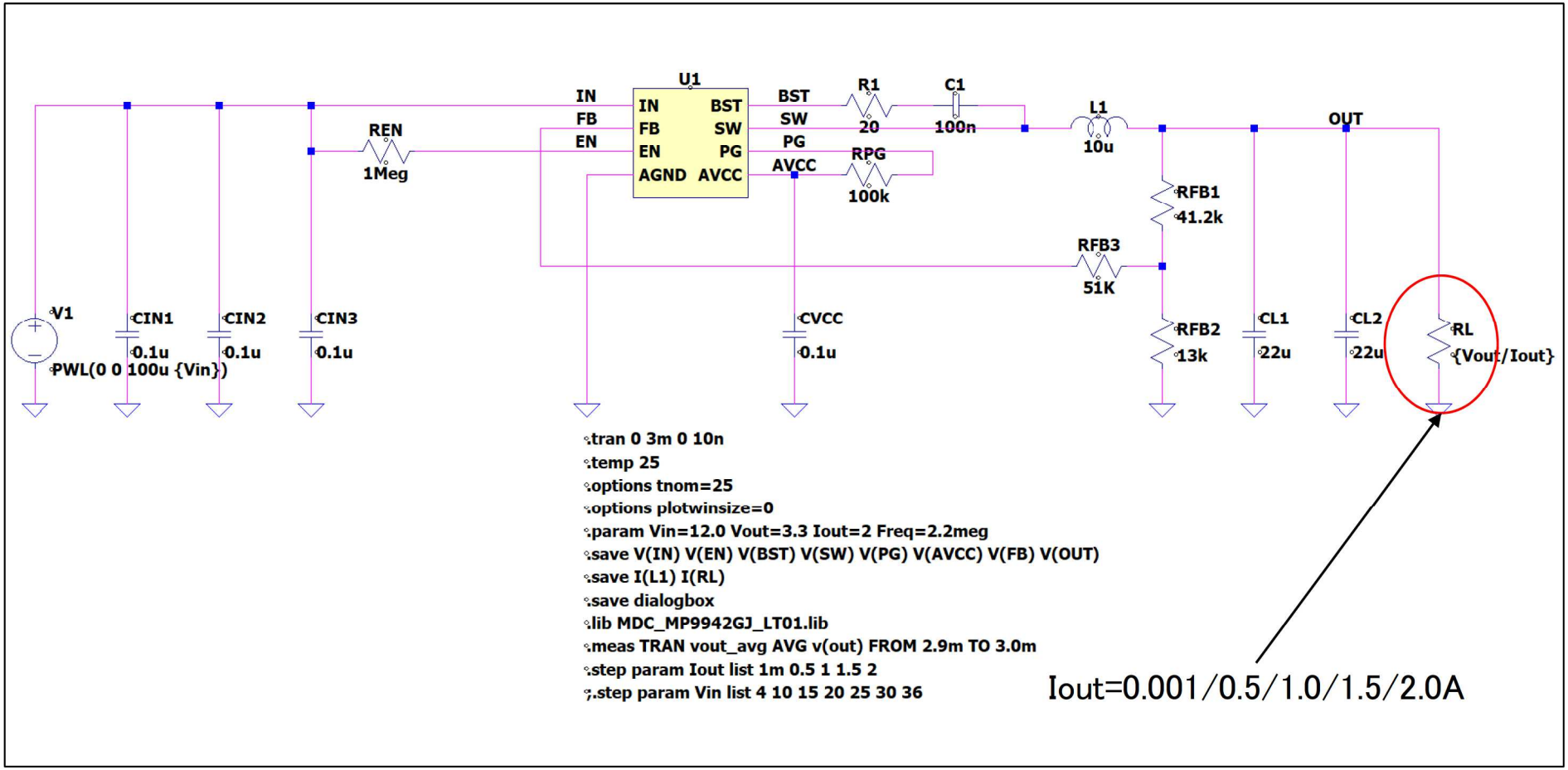


3.5.2 EN

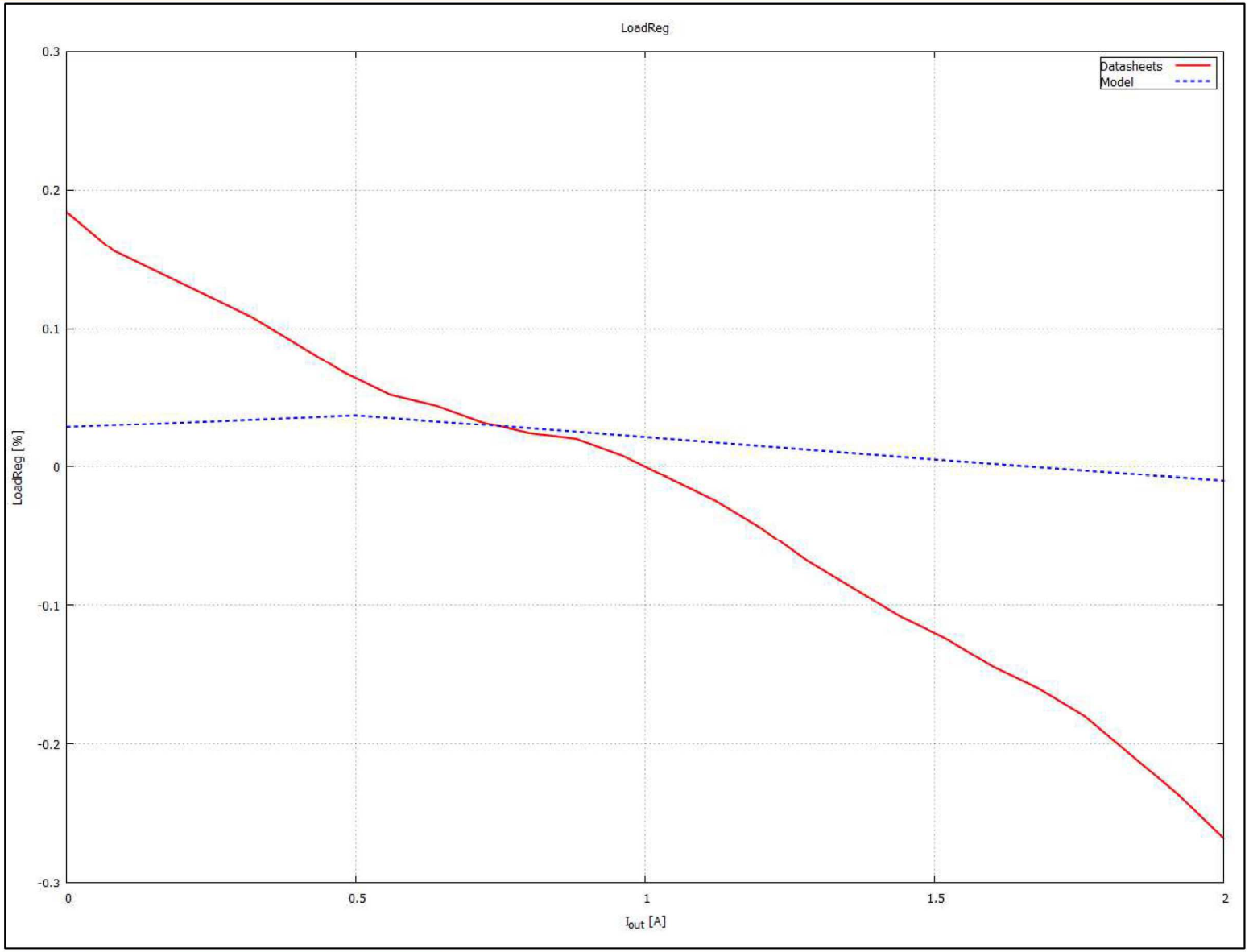
Item	Datasheet	Model
VEN_rising	1.40	1.40
VEN_falling	1.25	1.25



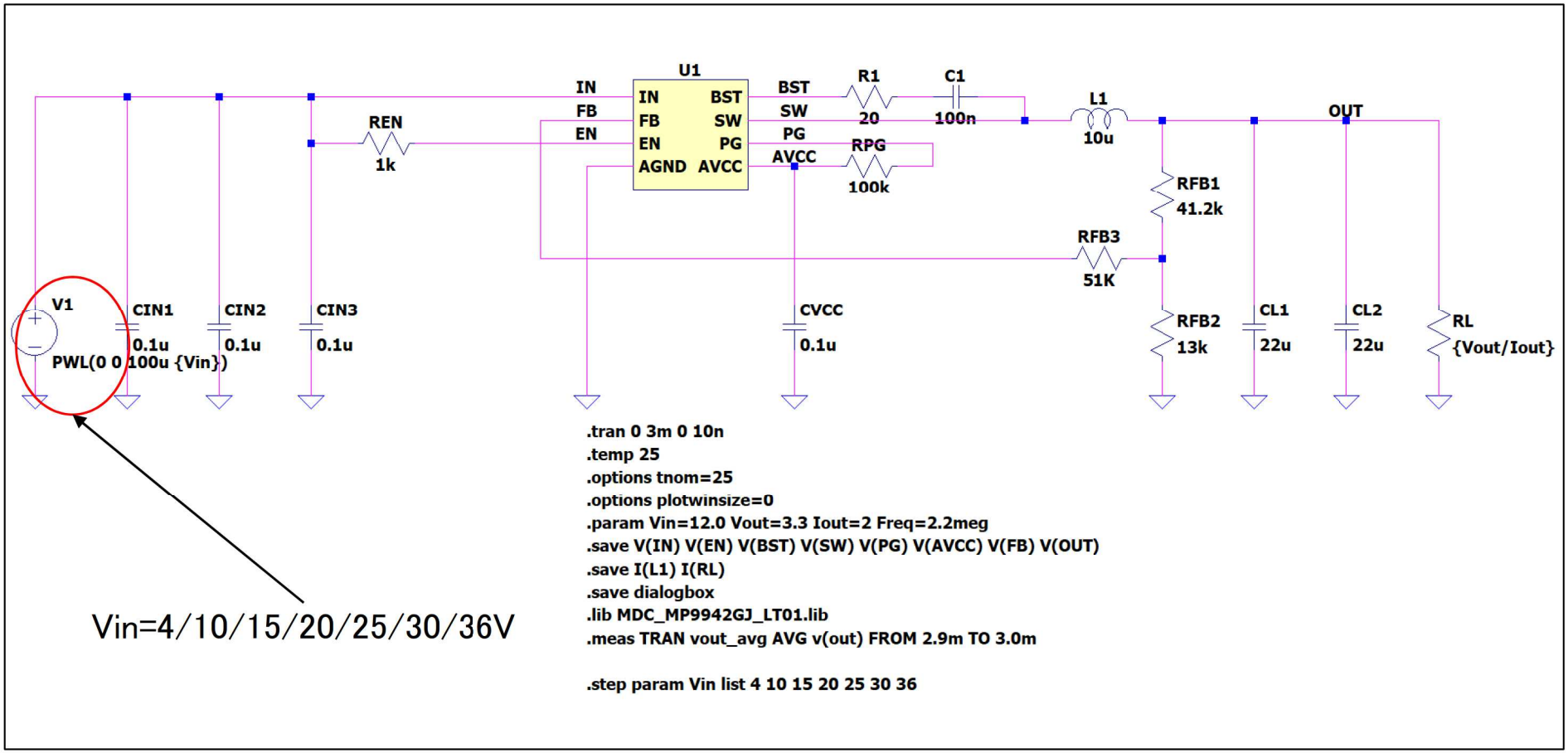
3.6.1 Load Regulation



3.6.2 Load Regulation



3.7.1 Line Regulation



3.7.2 Line Regulation