MoDeCH

Global Design Infrastructure Innovation

Gate Driver IC Model Report

Product Type : 2EDL05I06PJ

2019.11.30-J
2020.10.02-E

http://www.modech.com/

1. Model Feature and Characteristics

- 1.1 Supported Model Features
- 1.2 Target Fitting Characteristics
- 1.3 Others

1.1 Supported Model Features

Functions	Device	Model
Gate Driver function	○	○
Undervoltage Lockout（UVLO）	○	○
Deadtime and Interlock Function	○	○
Bootstrap diode	○	○
Tolerant to negative transient voltage	○	—

1.2.1 Target Fitting Characteristics

Red rectangle shows target modeling characteristics

Table 5 Static parameters

Parameter		Symbol	Values			Unit	Test condition
			Min	Typ	Max		
High level input voltage		V_{IH}	1.7	2.1	2.4	V	
Low level input voltage		V_{IL}	0.7	0.9	1.1		
High level output voltage	LO	V_{OH}	–	V_{DD} -0.45	V_{DD} -1		I_O = - 20 mA
	HO		–	V_B -0.45	V_B -1		
Low level output voltage	LO	V_{OL}	–	V_{GND}+0.13	V_{GND}+0.3		I_O = 20 mA
	HO		–	V_S+0.13	V_S +0.3		
V_{DD} supply undervoltage positive going threshold	IGBT-types	V_{DDUV+}	11.8	12.5	13.2		
	MOSFET types		8.3	9.1	9.9		
V_{BS} supply undervoltage positive going threshold	IGBT-types	V_{BSUV+}	10.9	11.6	12.4		
	MOSFET types		8.3	9.1	9.9		
V_{DD} supply undervoltage negative going threshold	IGBT-types	V_{DDUV-}	10.9	11.6	12.4		
	MOSFET types		7.5	8.3	9		
V_{BS} supply undervoltage negative going threshold	IGBT-types	V_{BSUV-}	10	10.7	11.7		
	MOSFET types		7.5	8.3	9		
V_{DD} and V_{BS} supply UVLO hysteresis	IGBT-types	V_{DDUVH}	0.5	0.9	–		
	MOSFET types	V_{BSUVH}	0.5	0.9	–		
High side leakage current betw. VS and GND		I_{LVS+}	–	1	12.5	µA	V_S = 600V
High side leakage current betw. VS and GND		I_{LVS+}[1]	–	10	–		T_J = 125 °C, V_S = 600 V
Quiescent current V_{BS} supply (VB only)		I_{QBS1}	–	170	300		HO = low depending on current types
Quiescent current V_{BS} supply (VB only)		I_{QBS2}	–	170	300		HO = high depending on current types
Quiescent current VDD supply (VDD only)		I_{QDD1}	–	0.3	0.6	mA	V_{LIN} = float.

All fitting is done for typical and Ta=25°C

1.2.2 Target Fitting Characteristics

Red rectangle shows target modeling characteristics

Table 5 Static parameters

Parameter	Symbol	Values			Unit	Test condition
		Min.	Typ.	Max.		
Quiescent current VDD supply (VDD only)	I_{QDD2}	–	0.28	0.6		V_{LIN} = 3.3 V, V_{HIN}=0
Quiescent current VDD supply (VDD only)	I_{QDD3}	–	0.28	0.6		V_{LIN}=0 , V_{HIN}=3.3 V
Input bias current	I_{LIN+}	15	35	60	µA	V_{LIN} = 3.3 V
Input bias current	I_{LIN-}	–	0	–		V_{LIN} = 0
Input bias current	I_{HIN+}	15	35	60		V_{HIN} = 3.3 V
Input bias current	I_{HIN-}	–	0	–		V_{HIN} = 0
Mean output current for load capacity charging in range from 3 V (20%) to 6 V (40%)	I_{O+}	0.18	0.23	–	A	C_L = 22 nF
Peak output current turn on (single pulse)	I_{Opk+}[1]	–	0.36	–		R_L = 0 Ω, t_p <10 µs
Mean output current for load capacity discharging in range from 12 V (80%) to 9 V (60%)	I_{O-}	0.39	0.48	–		C_L = 22 nF
Peak output current turn off (single pulse)	I_{Opk-}[1]	–	0.70	–		R_L = 0 Ω, t_p <10 µs
Bootstrap diode forward voltage between VDD and VB	$V_{F,BSD}$	–	1.0	1.2	V	I_F = 0.3 mA
Bootstrap diode forward current between VDD and VB	$I_{F,BSD}$	30	55	80	mA	$V_{DD} - V_B$ = 4 V
Bootstrap diode resistance	R_{BSD}	20	36	54	Ω	V_{f1} = 4 V, V_{f2} = 5 V

All fitting is done for typical and Ta=25°C

1.2.3 Target Fitting Characteristics

Red rectangle shows target modeling characteristics

Table 6 Dynamic parameters

Parameter		Symbol	Values			Unit	Test condition
			Min.	Typ.	Max.		
Turn-on propagation delay	IGBT types	t_{on}	280	420	610	ns	$V_{LIN\&HIN}$ = 0 or 3.3 V
	MOSFET types		210	310	460		
Turn-off propagation delay	IGBT types	t_{off}	260	400	590		
	MOSFET types		200	300	440		
Turn-on rise time		t_r	–	48	80		$V_{LIN\&HIN}$ = 0 or 3.3 V C_L = 1 nF
Turn-off fall time		t_f	–	24	40		
Input filter time at LIN/HIN for turn on and off	IGBT types	t_{FILIN}	120	192	–		$V_{LIN\&HIN}$ = 0 & 3.3 V
	MOSFET types HIN LIN		 50 100	 100 150	 170 250		
Dead time (not for 2EDL05I06BF)	IGBT types	DT	260	380	540	ns	$V_{LIN\&HIN}$ = 0 & 3.3 V
	MOSFET types		30	75	140		
Dead time matching abs(DT_LH – DT_HL) for single IC (not for 2EDL05I06BF)	IGBT types	MDT	–	10	80		ext. dead time 0ns
	MOSFET types			10	50		
Matching delay ON, abs(ton_HS - ton_LS)		MT_{ON}	–	10	60		external dead time > 500 ns
Matching delay OFF, abs(toff_HS-toff_LS)		MT_{OFF}	–	10	60		external dead time >500 ns
Output pulse width matching. PW_{in}-PW_{out}	IGBT types	PM	–	20	80		PW_{in} > 1 µs
	MOSFET types		–	20	70		

All fitting is done for typical and Ta=25°C

1.3 Others

- Supported Simulator
  - LTspiceXVII

- Ta=25℃、TNOM=25℃

2. Terminal Information

Table 1 2EDL05 family lead definitions

Pin no.	Name	Function
1	VDD	Low-side and logic supply voltage
2	HIN	Logic input for high-side gate driver output (HO), in phase. Schmitt trigger inputs with hysteresis and pull down
3	LIN	Logic input for low-side gate driver output (LO), in phase. Schmitt trigger inputs with hysteresis and pull down
4	GND	Low-side gate drive return
5	LO	Low-side driver output
6	VS	High voltage floating supply return
7	HO	High-side driver output
8	VB	High-side gate drive floating supply

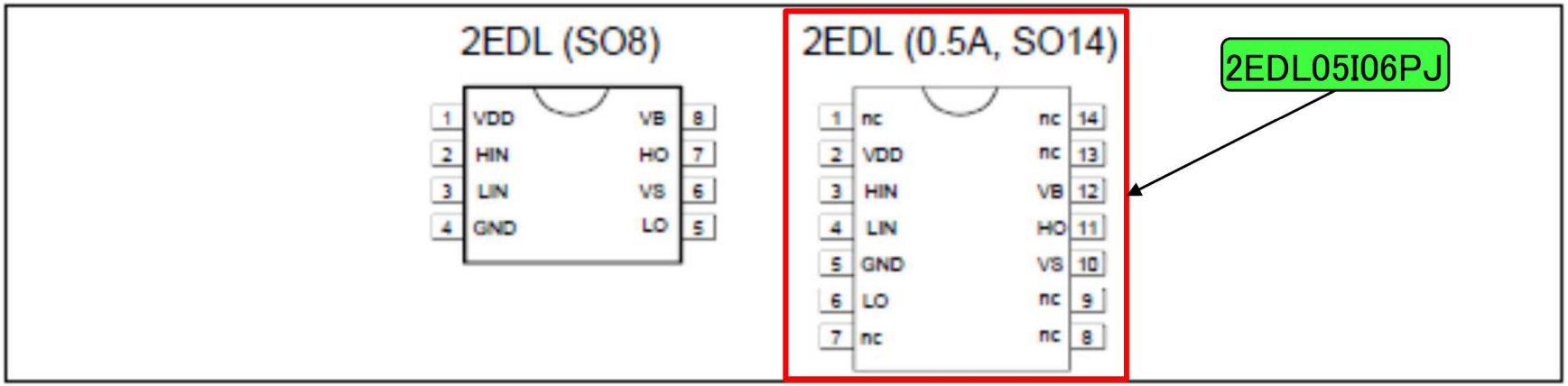


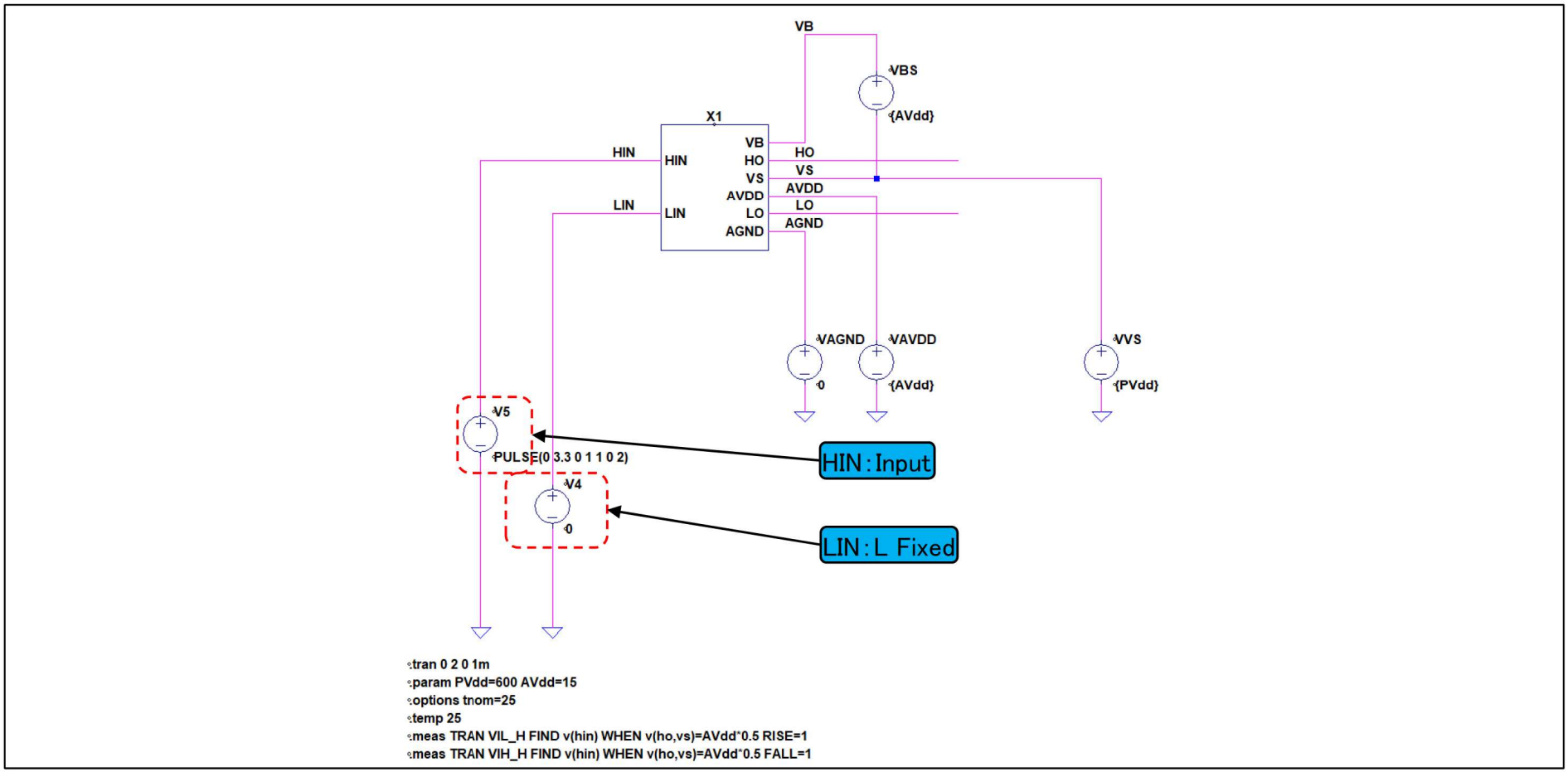
Figure 3 2EDL05 family lead assignments (top view)

3. Verification Results

- 3.1 HIN threshold
- 3.2 LIN threshold
- 3.3 HO VOLH
- 3.4 LO VOLH
- 3.5 VBS UVLO
- 3.6 VDD UVLO
- 3.7 Input bias current
- 3.8 Bootstrap diode VF
- 3.9 Bootstrap diode IF
- 3.10 Turn-on/off propagation delay
- 3.11 Turn-on rise time & Turn-off fall time
- 3.12 Input filter time at LIN/HIN for turn on and off
- 3.13 Dead time
- 3.14 Function (Normal operation)

3.1.1 HIN threshold

Test Bench



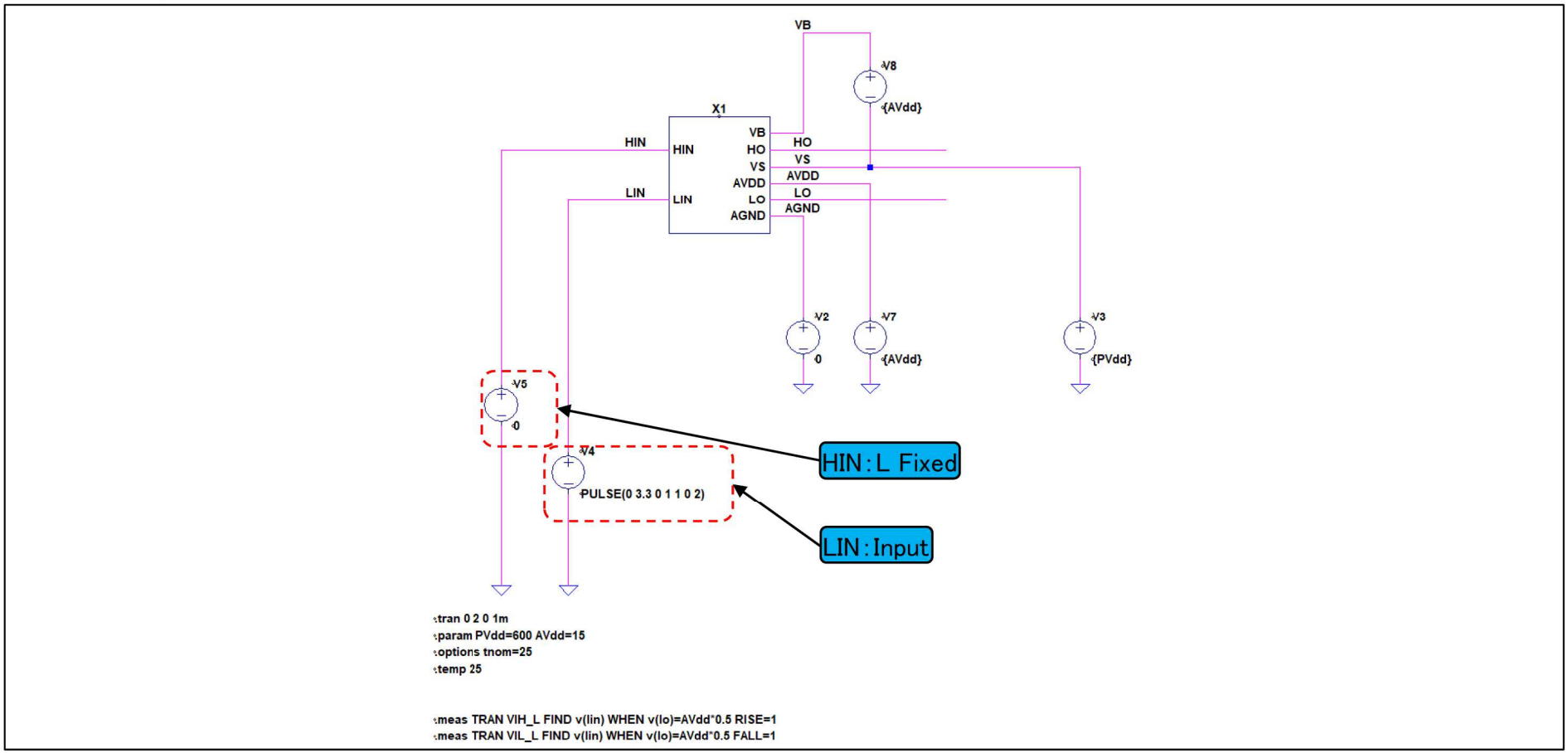
3.1.2 HIN threshold

Simulation Result

symbol	Unit	DS	Sim.
VIH	V	2.1	2.1
VIL	V	0.9	0.9

3.2.1 LIN threshold

Test Bench



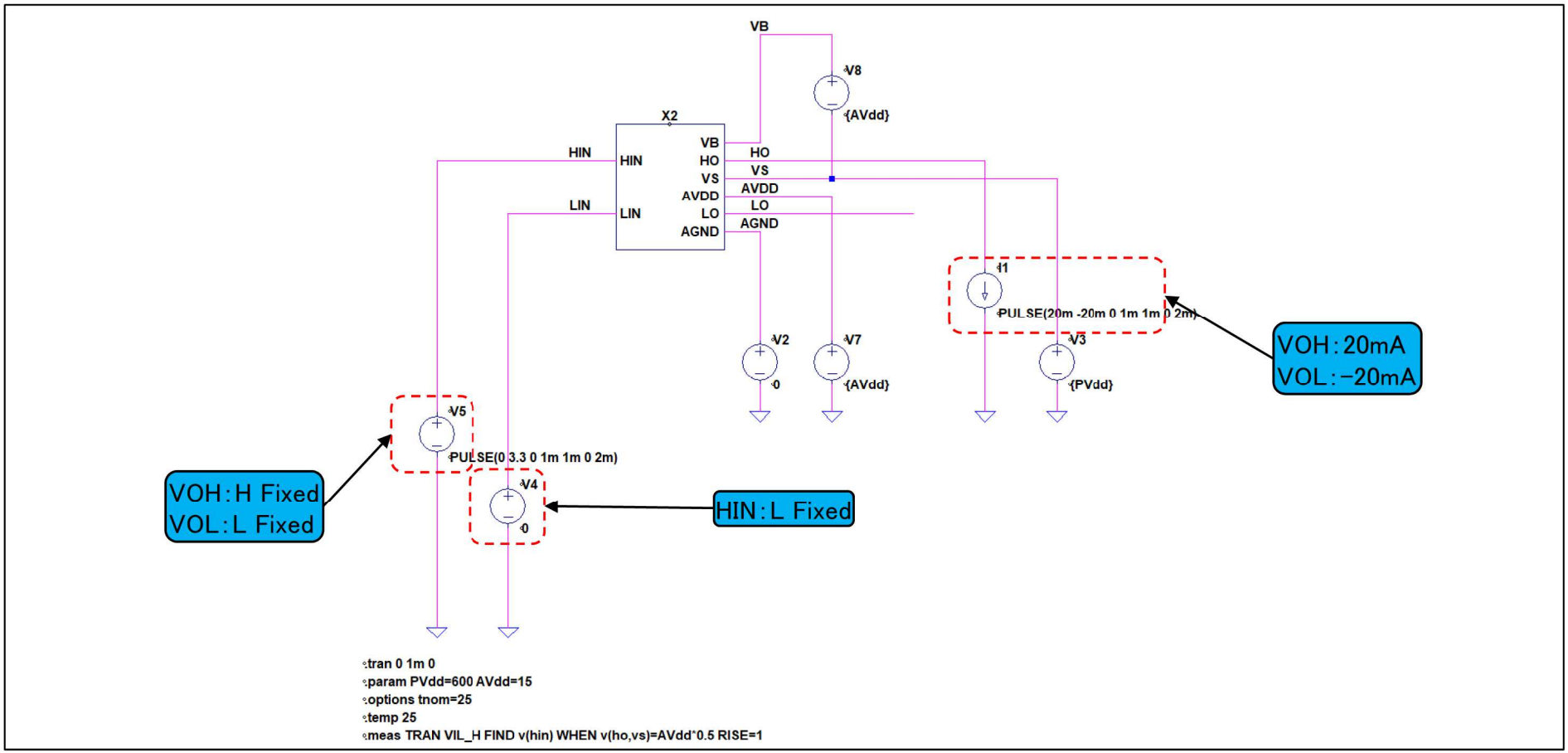
3.2.2 LIN threshold

Simulation Result

symbol	Unit	DS	Sim.
VIH	V	2.1	2.1
VIL	V	0.9	0.9

3.3.1 HO VOLH

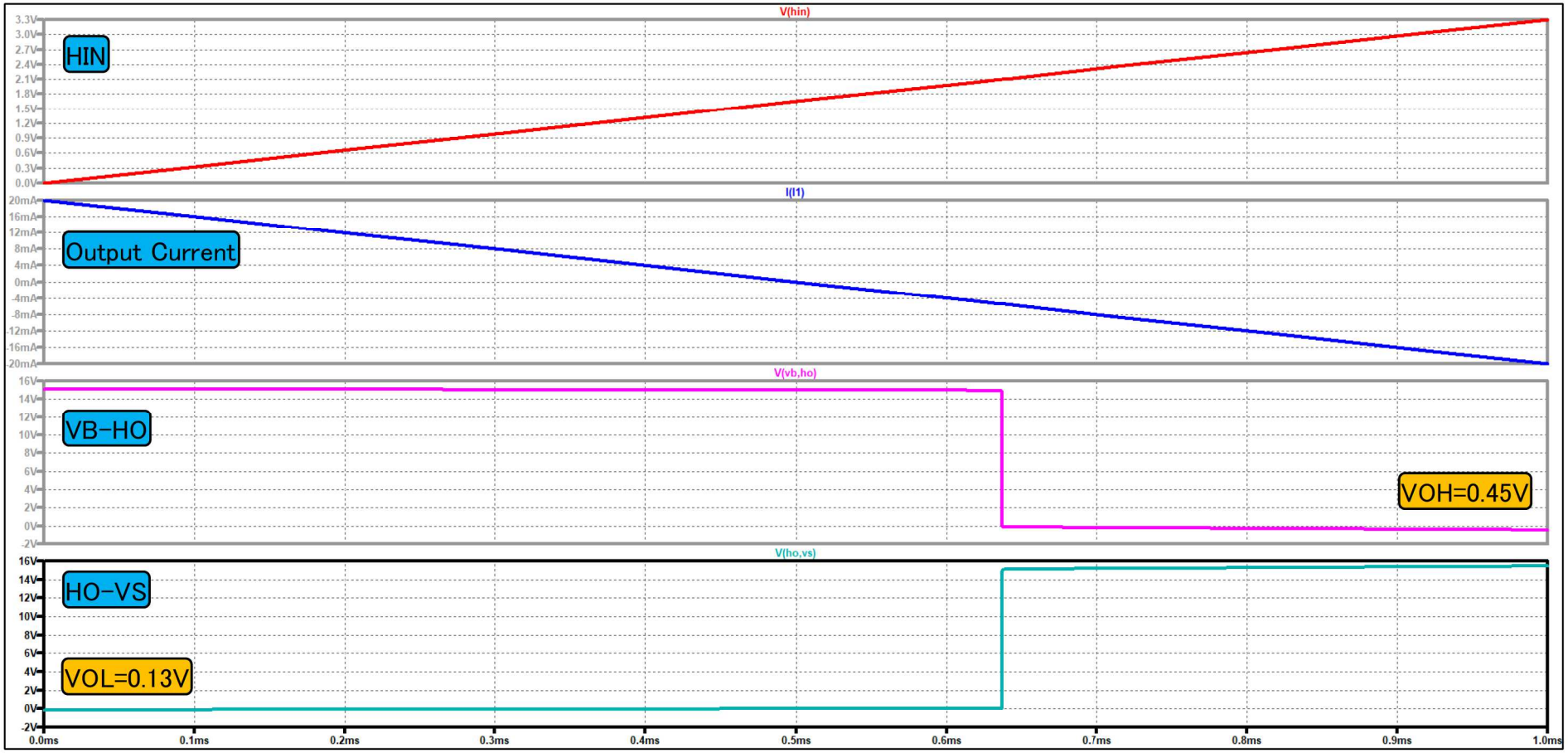
Test Bench



3.3.2 HO VOLH

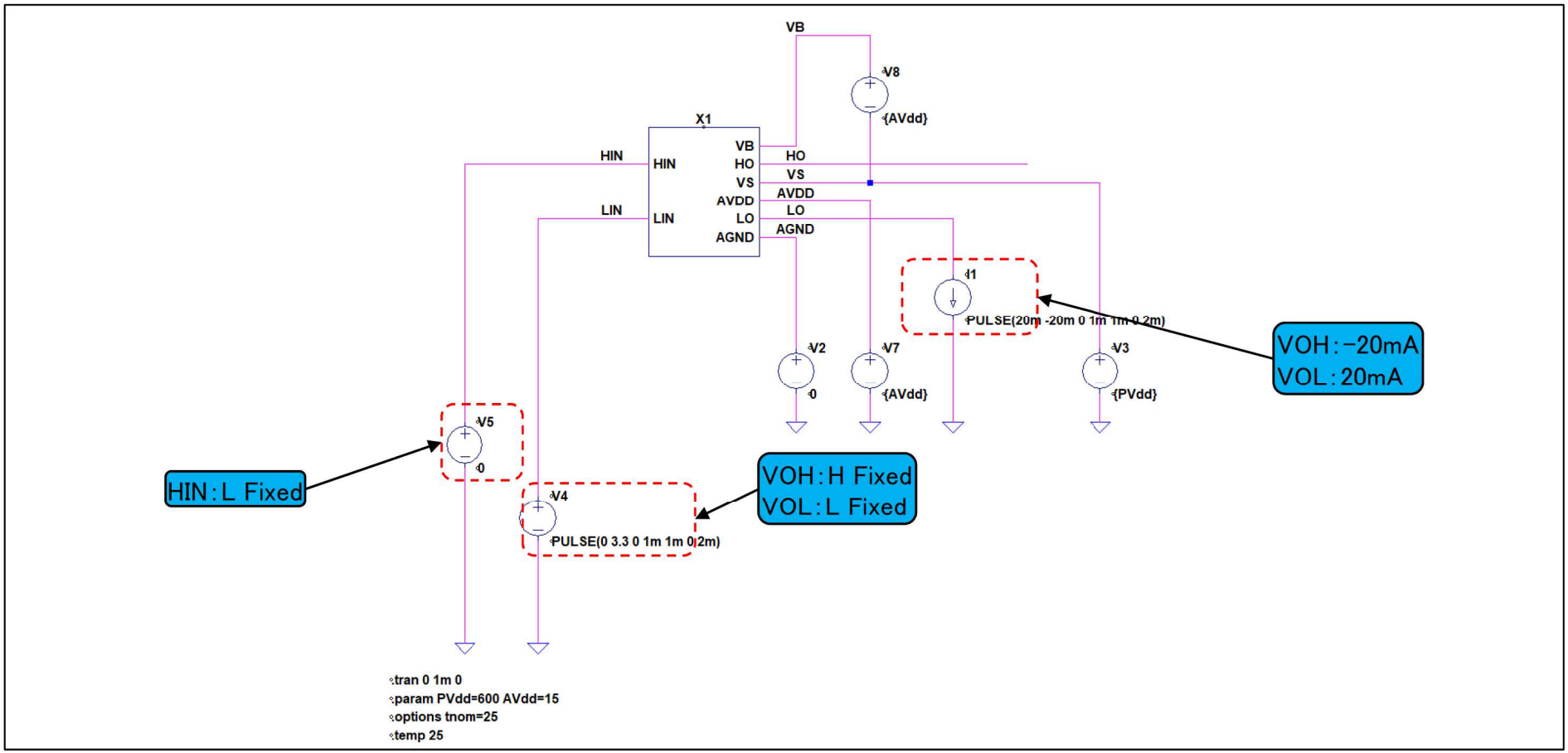
Simulation Result

symbol	Unit	DS	Sim.
VOH	V	0.45	0.45
VOL	V	0.13	0.13



3.4.1 LO VOLH

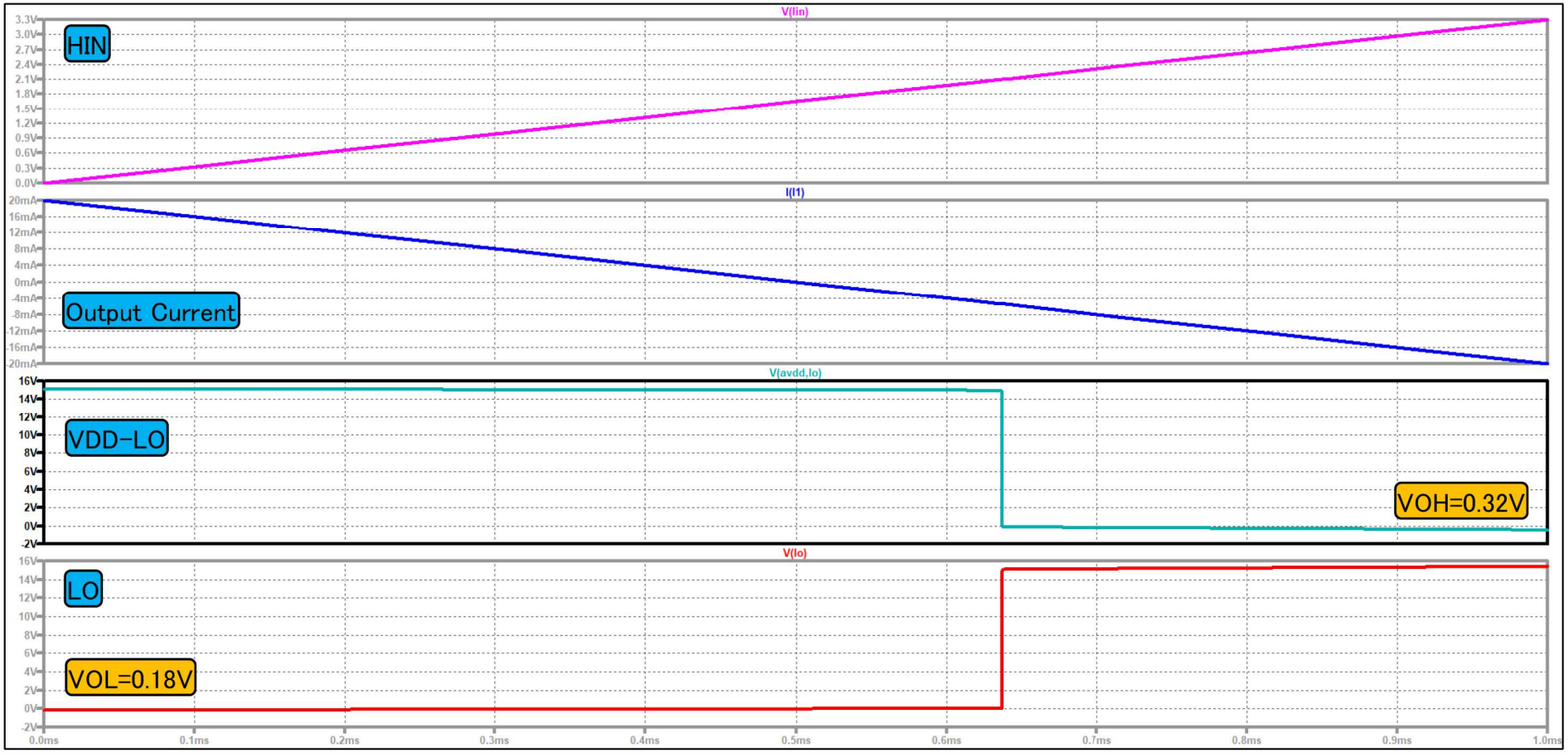
Test Bench



3.4.2 LO VOLH

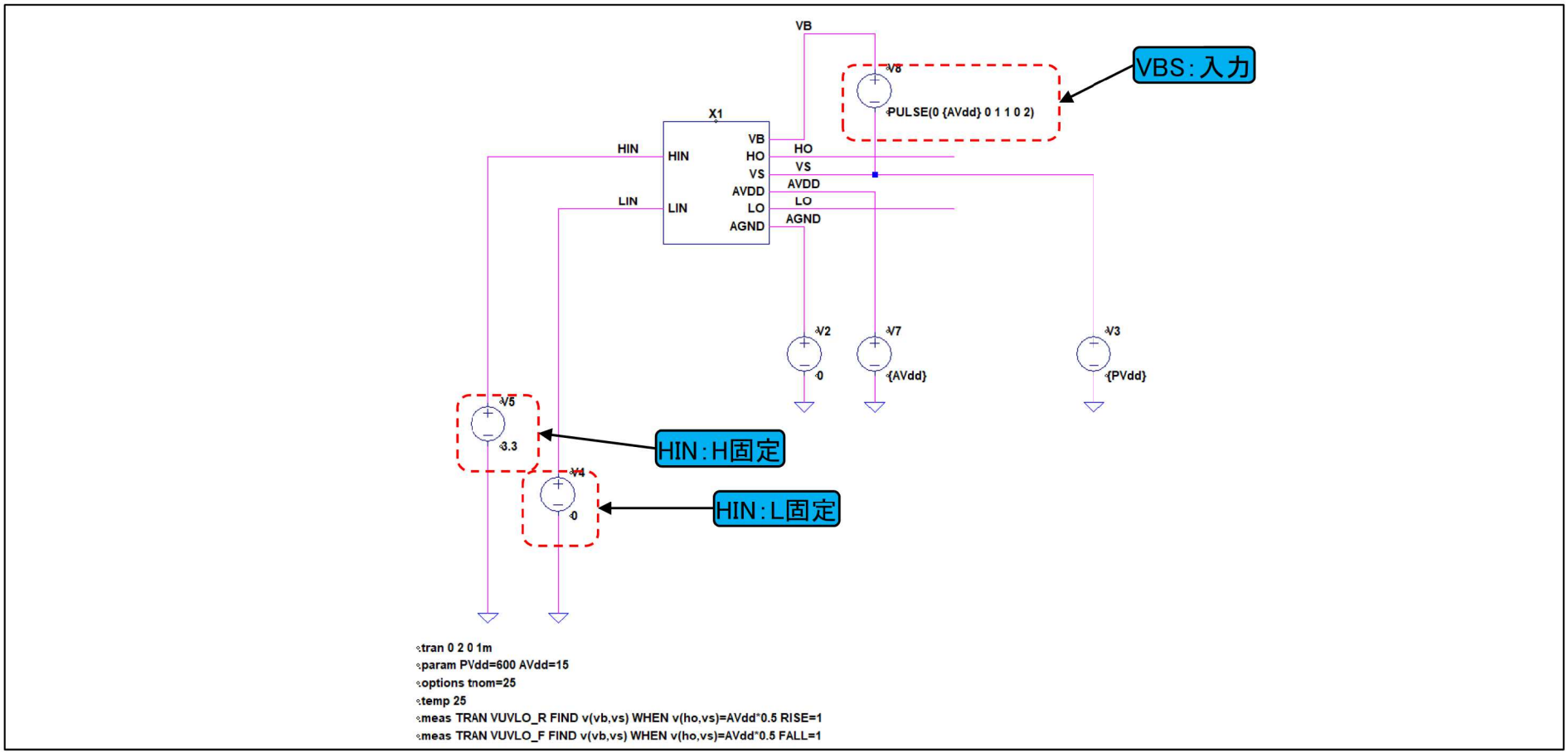
Simulation Result

symbol	Unit	DS	Sim.
VOH	V	0.45	0.45
VOL	V	0.13	0.13



3.5.1 VBS UVLO threshold

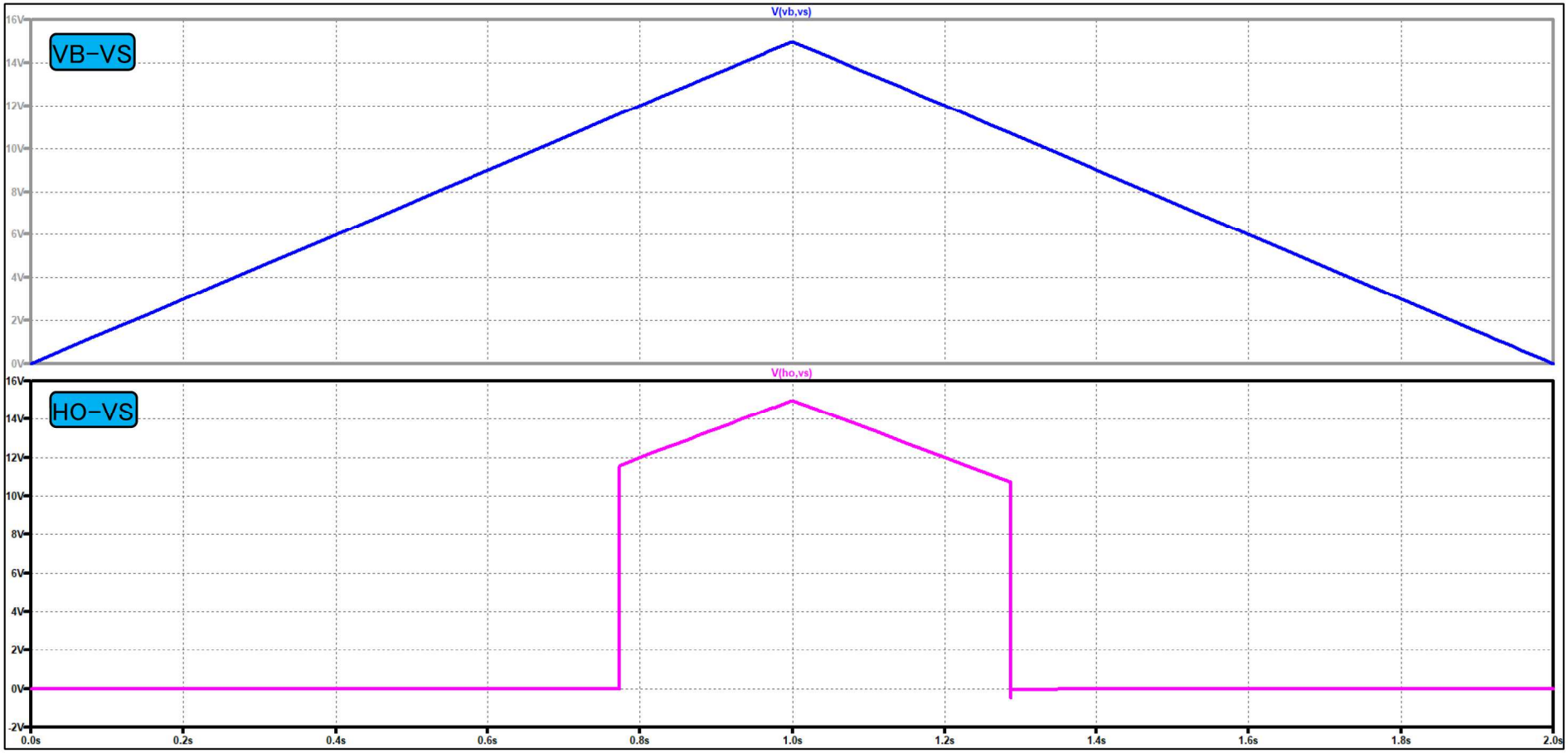
テストベンチ



3.5.2 VBS UVLO threshold

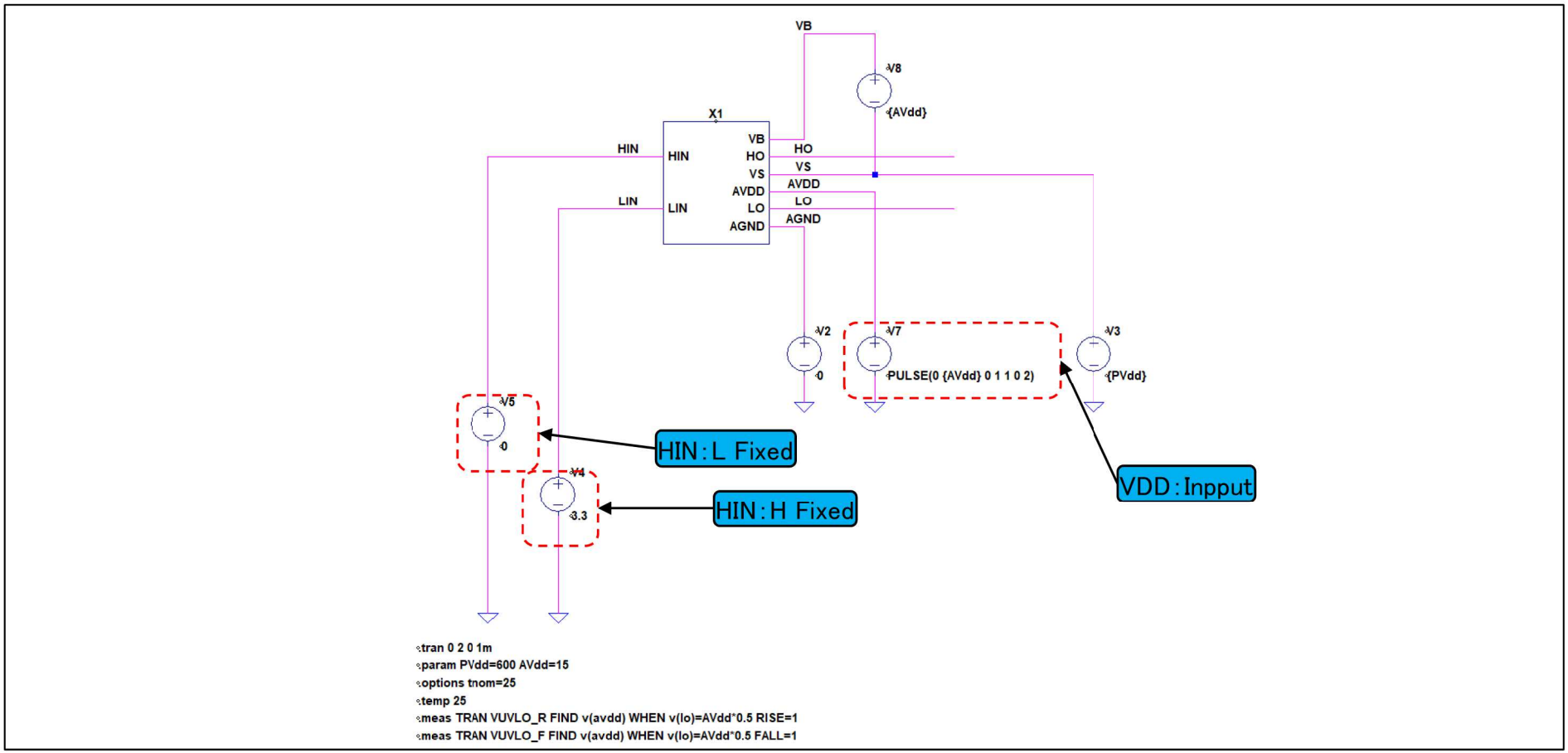
シミュレーション結果

symbol	Unit	DS	Sim.
VBSUV+	V	11.6	11.6
VBSUV-	V	10.7	10.7



3.6.1 VDD UVLO threshold

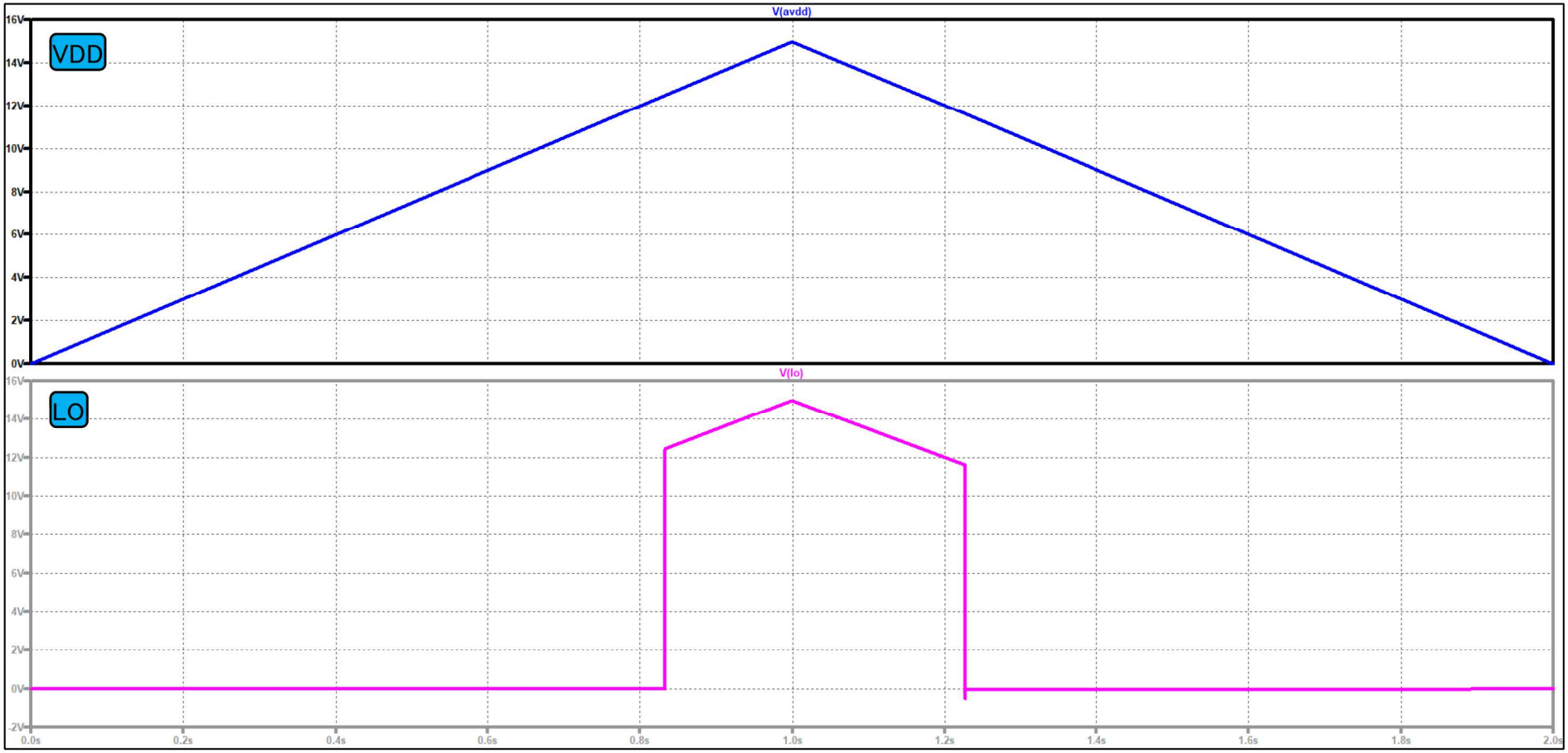
Test Bench



3.6.2 VDD UVLO threshold

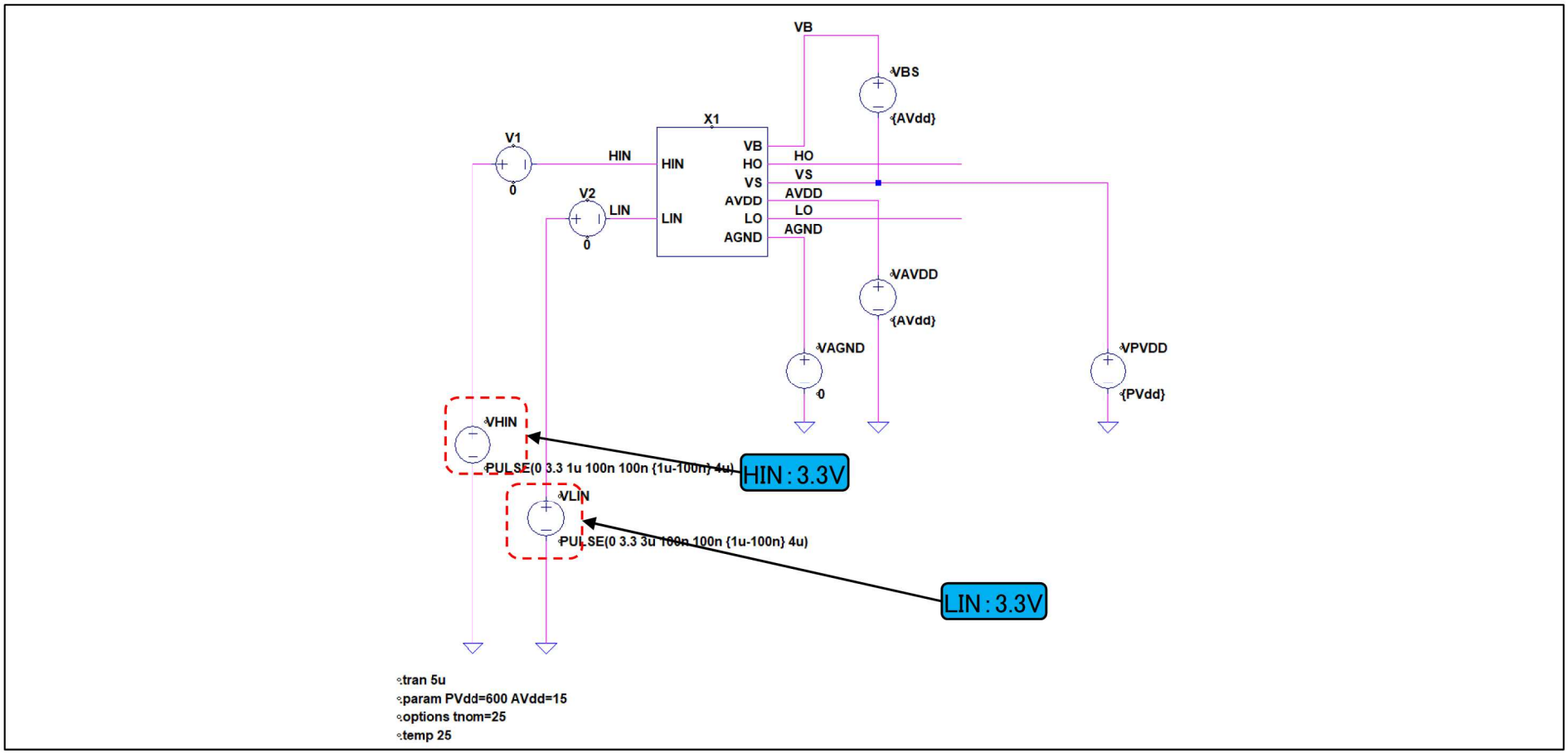
Simulation Result

symbol	Unit	DS	Sim.
VDDUV+	V	12.5	12.5
VDDUV−	V	11.6	11.6



3.7.1 Input bias current

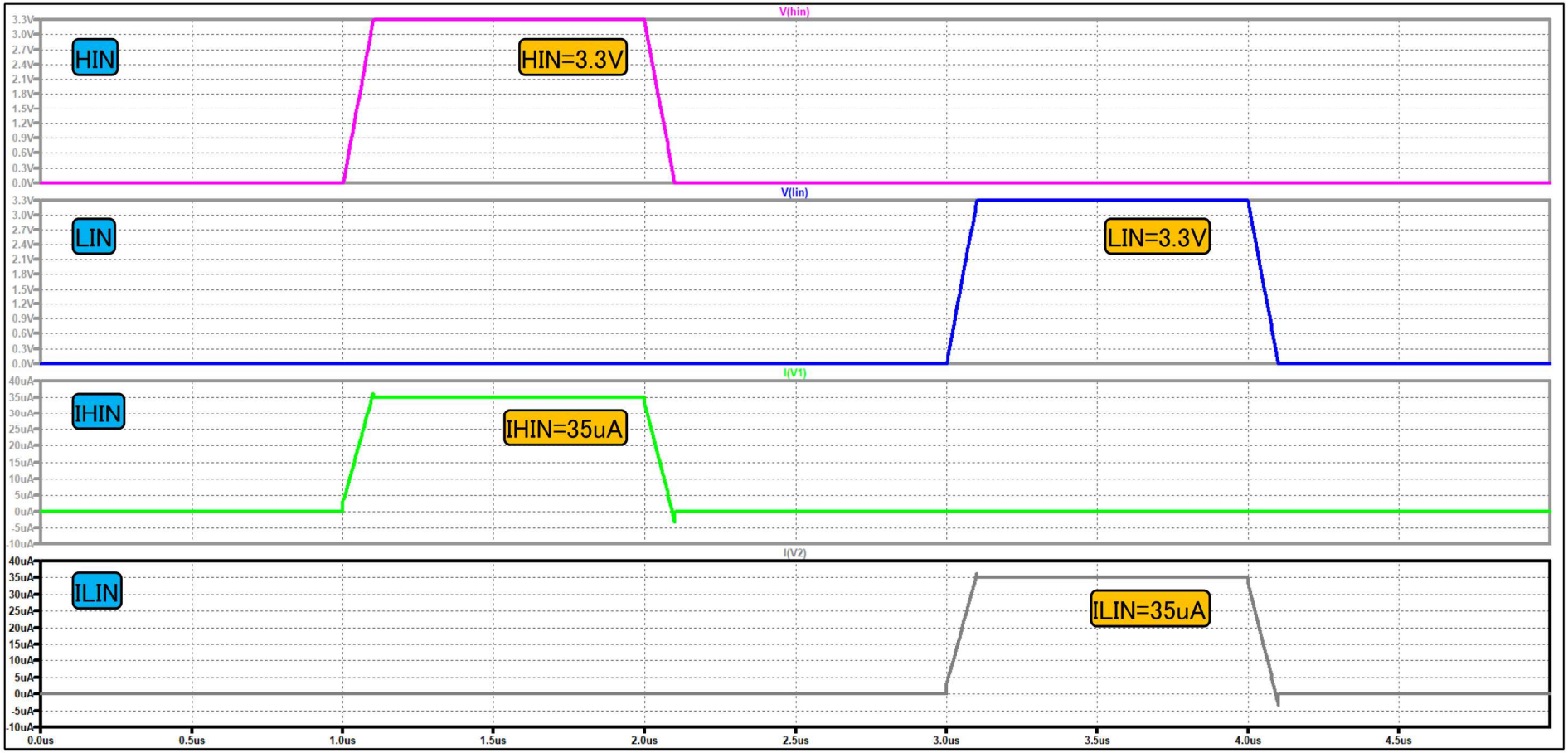
Test Bench



3.7.2 Input bias current

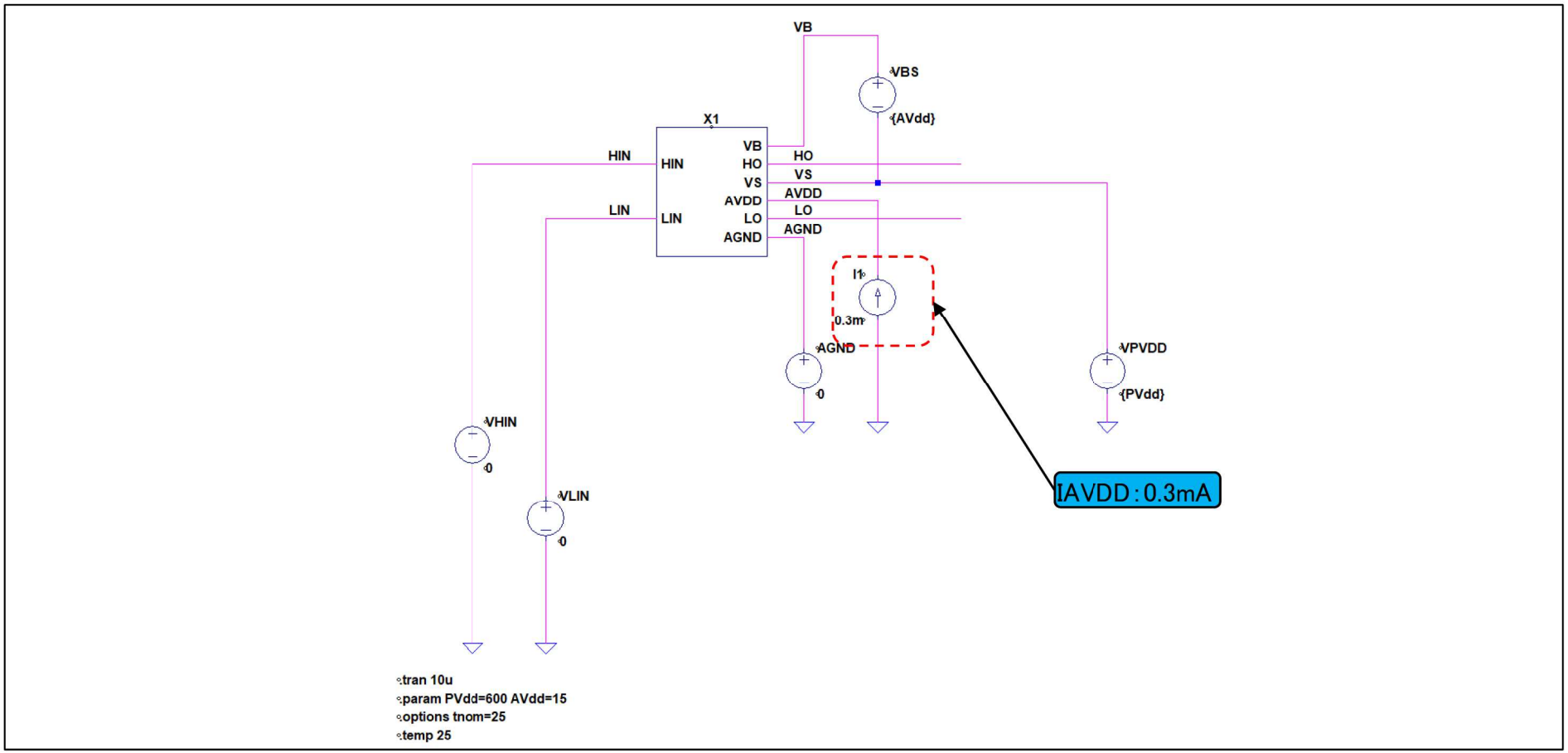
Simulation Result

Symbol	Unit	DS	Sim.
IHIN+	uA	35	35
ILIN+	uA	35	35



3.8.1 Bootstrap diode VF

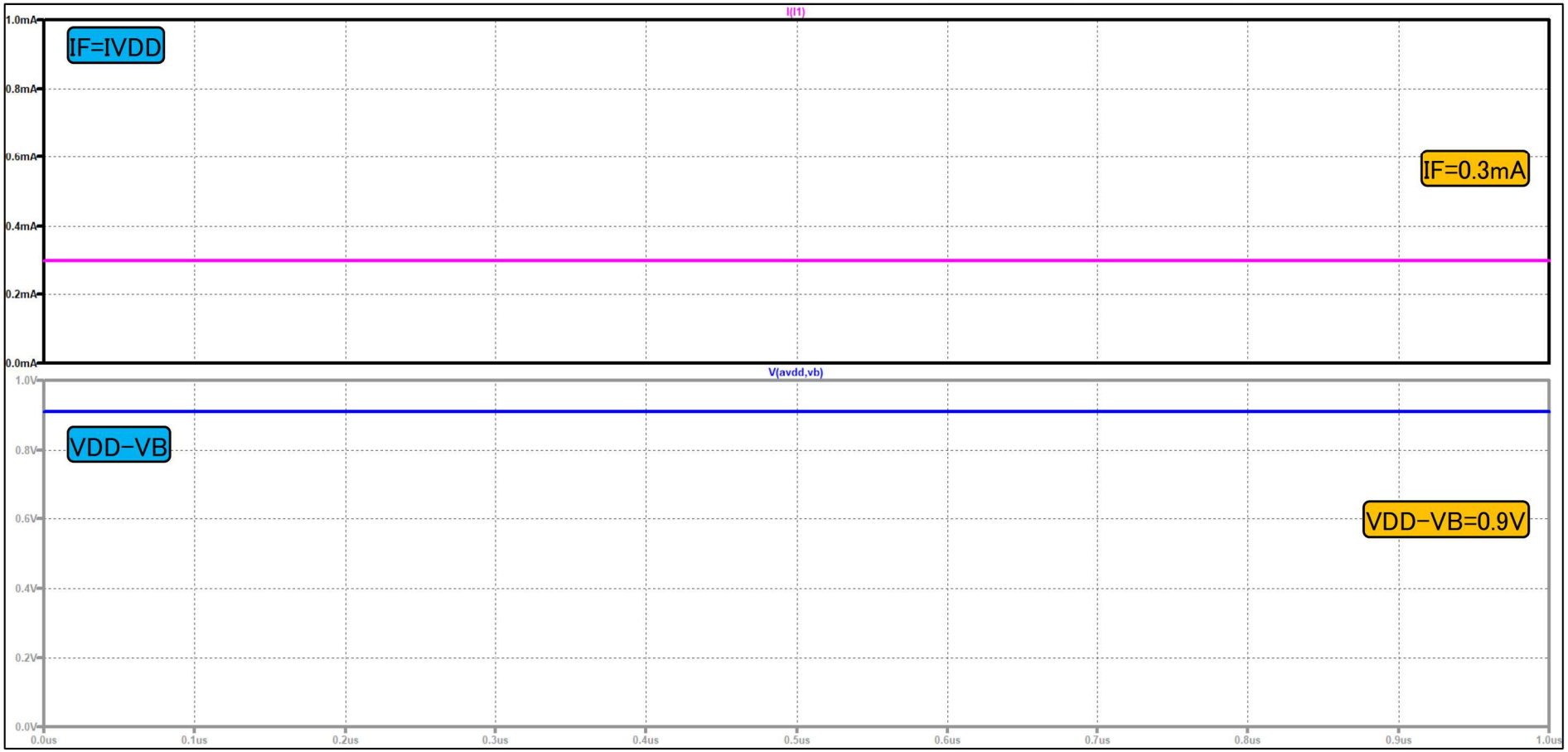
Test Bench



3.8.2 Bootstrap diode VF

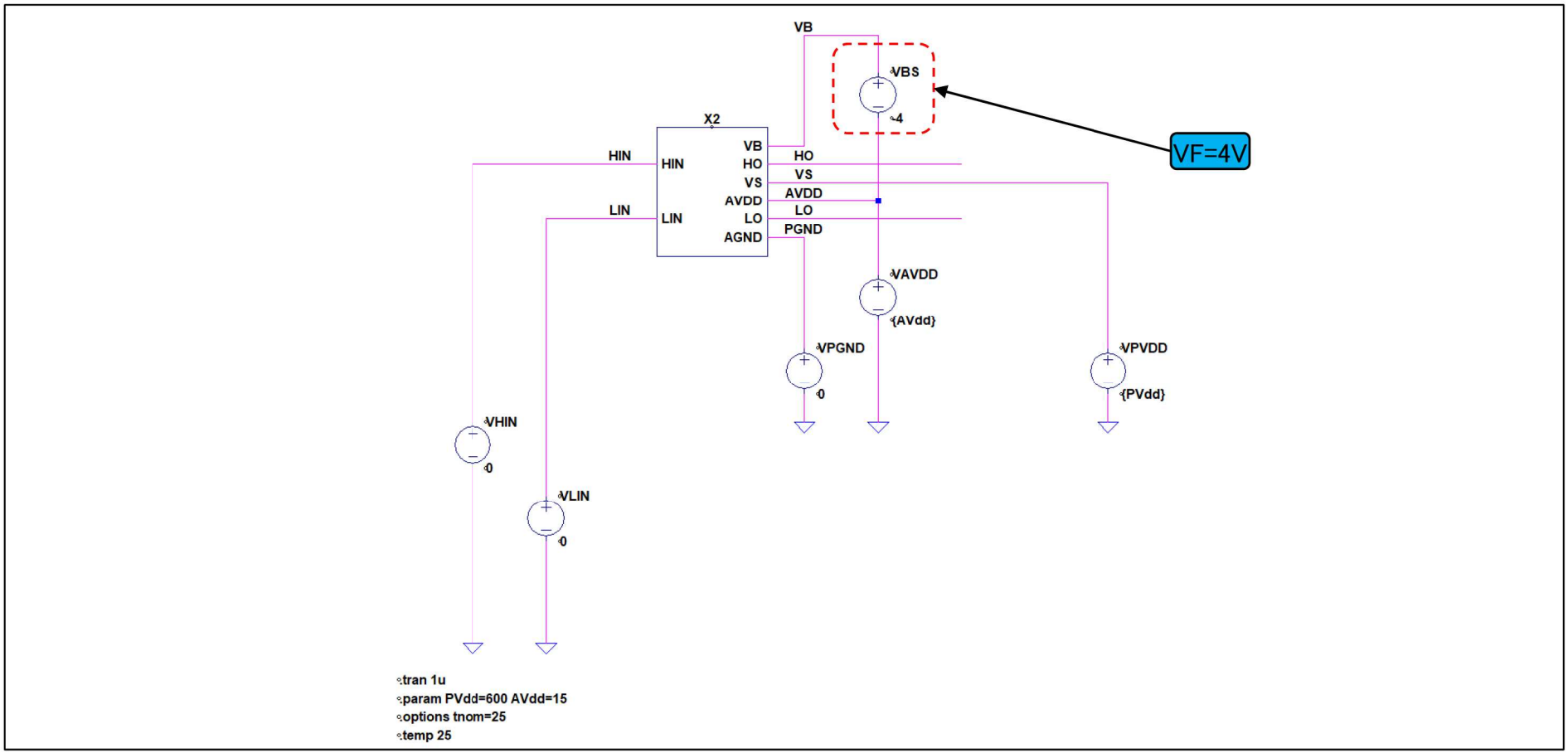
Simulation Result

Symbol	Unit	DS	Sim.
VF,BSD	V	0.9	0.9



3.9.1 Bootstrap diode IF

Test Bench



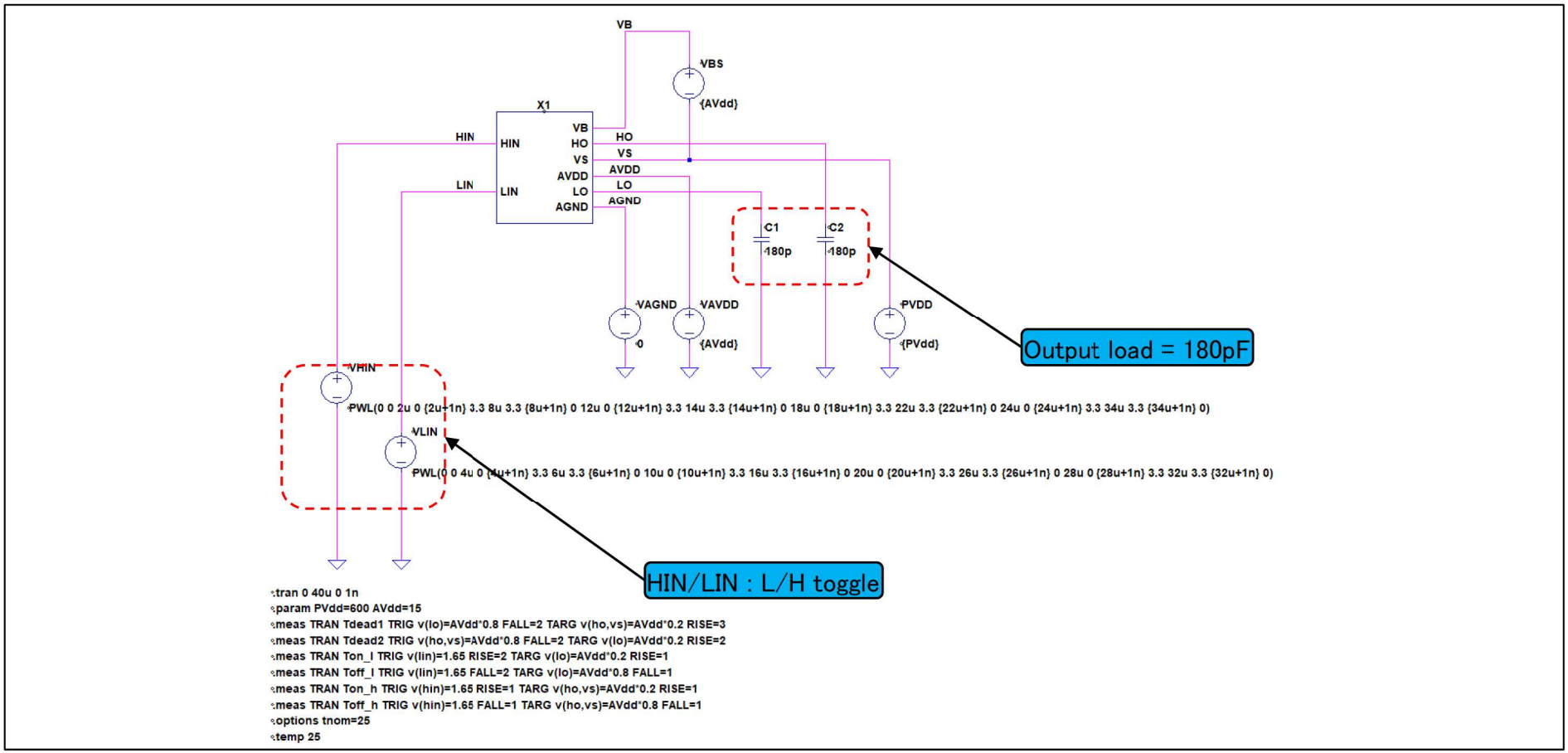
3.9.2 Bootstrap diode IF

Simulation Result

Symbol	Unit	DS	Sim.
IF,BSD	mA	55	55

3.10.1 Turn-on/off propagation delay

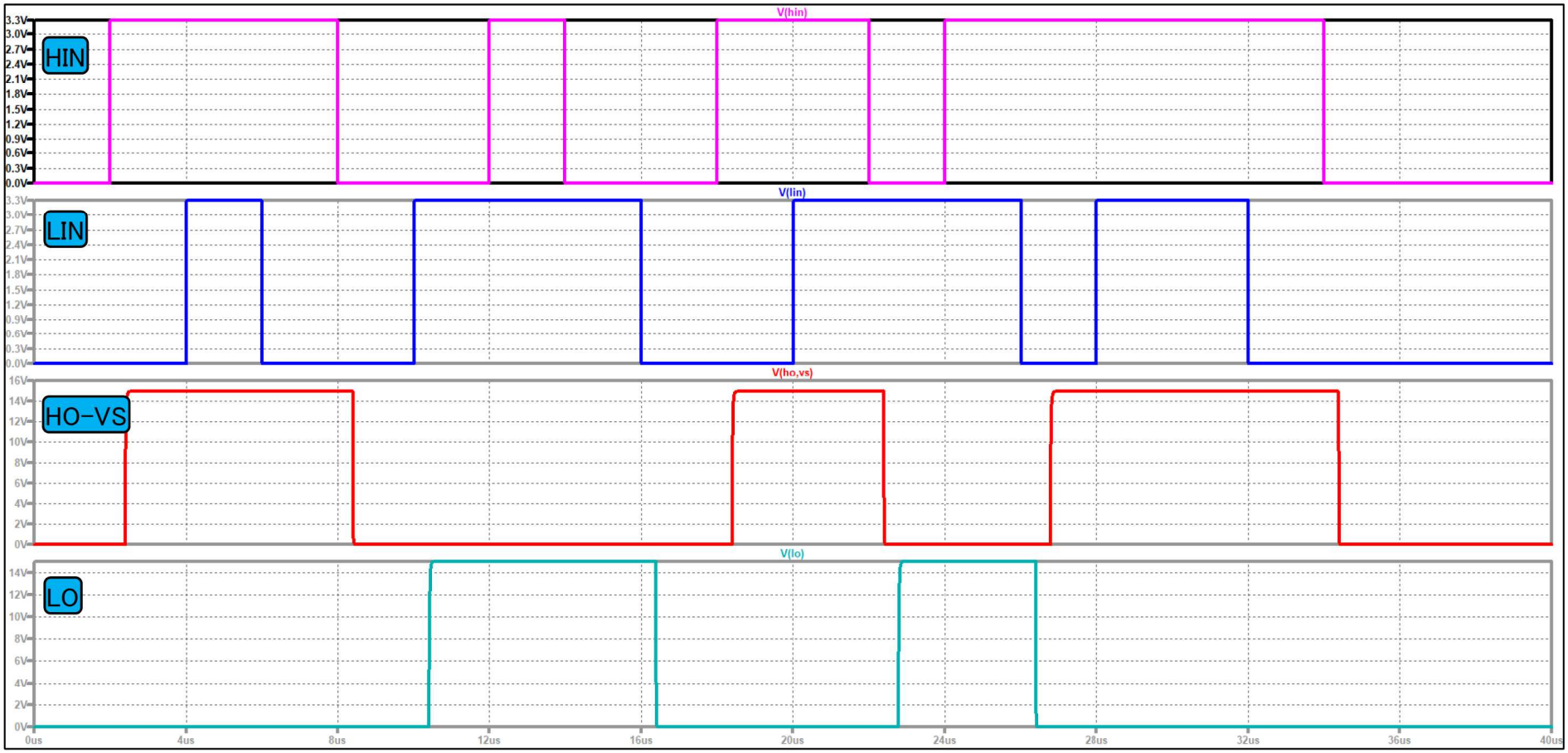
Test Bench



3.10.2 Turn-on/off propagation delay

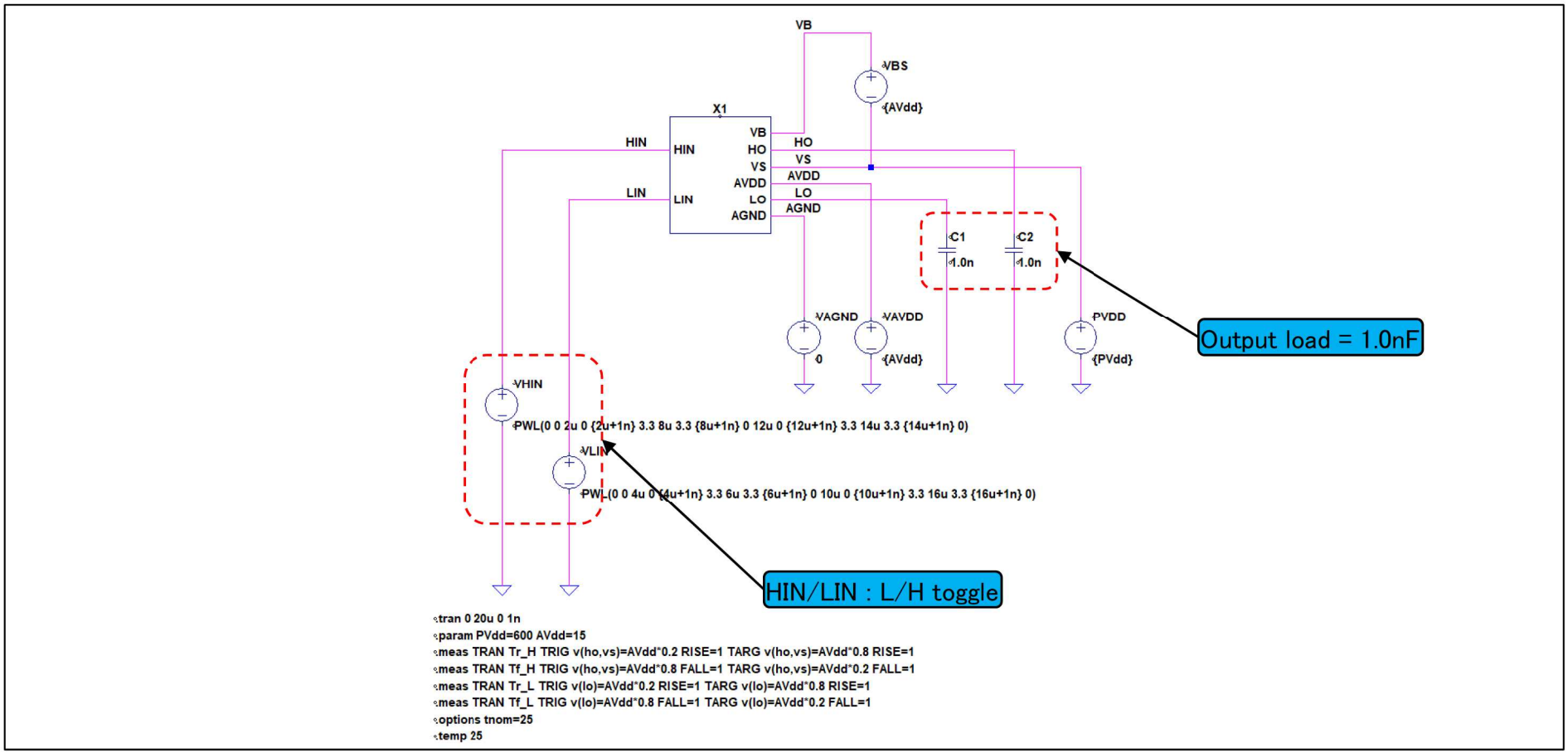
Simulation Result

Signal	Symbol	Unit	DS	Sim.
HO	tON	ns	420	398
	tOFF	ns	400	396
LO	tON	ns	420	398
	tOFF	ns	400	396



3.11.1 Turn-on rise time & Turn-off fall time

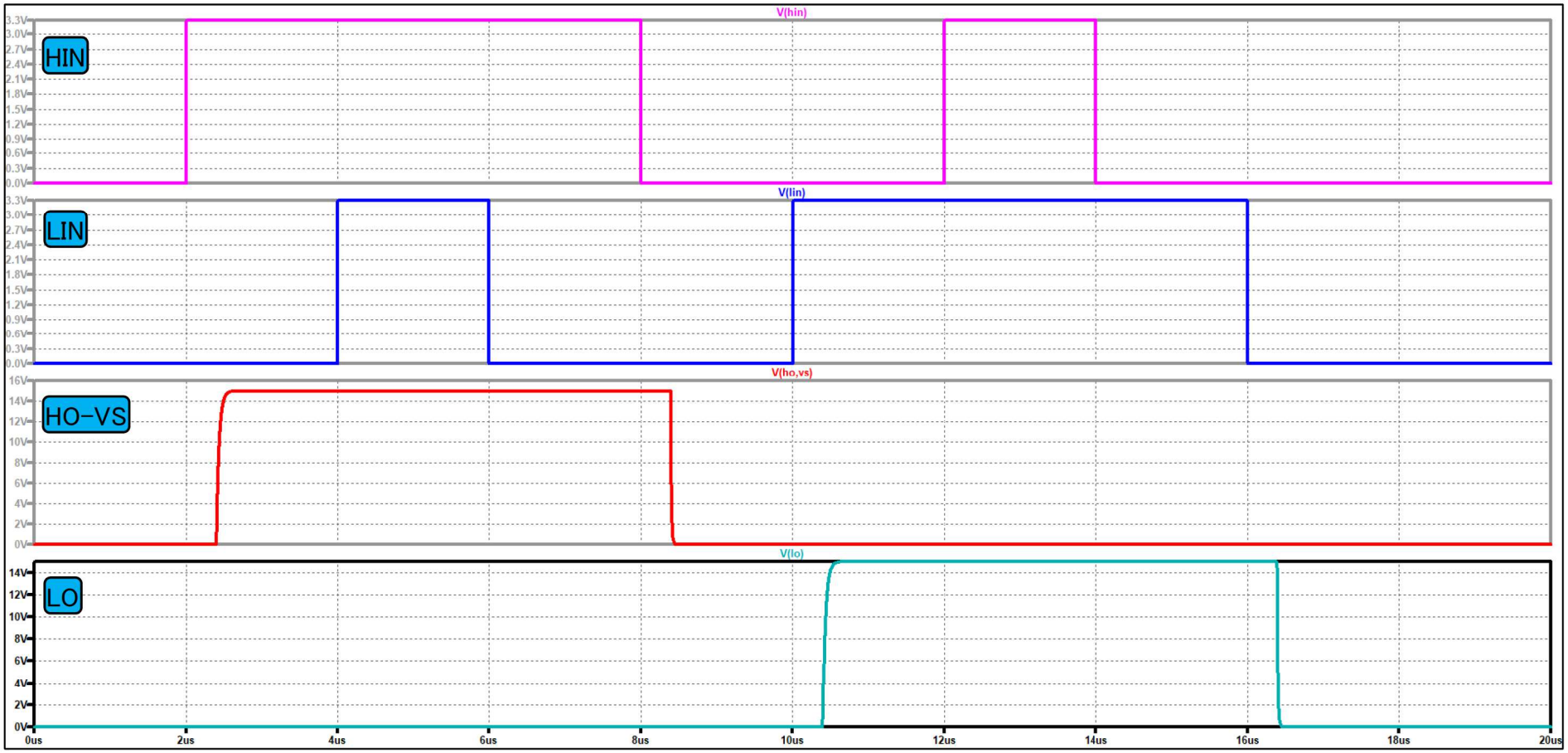
Test Bench



3.11.2 Turn-on rise time & Turn-off fall time

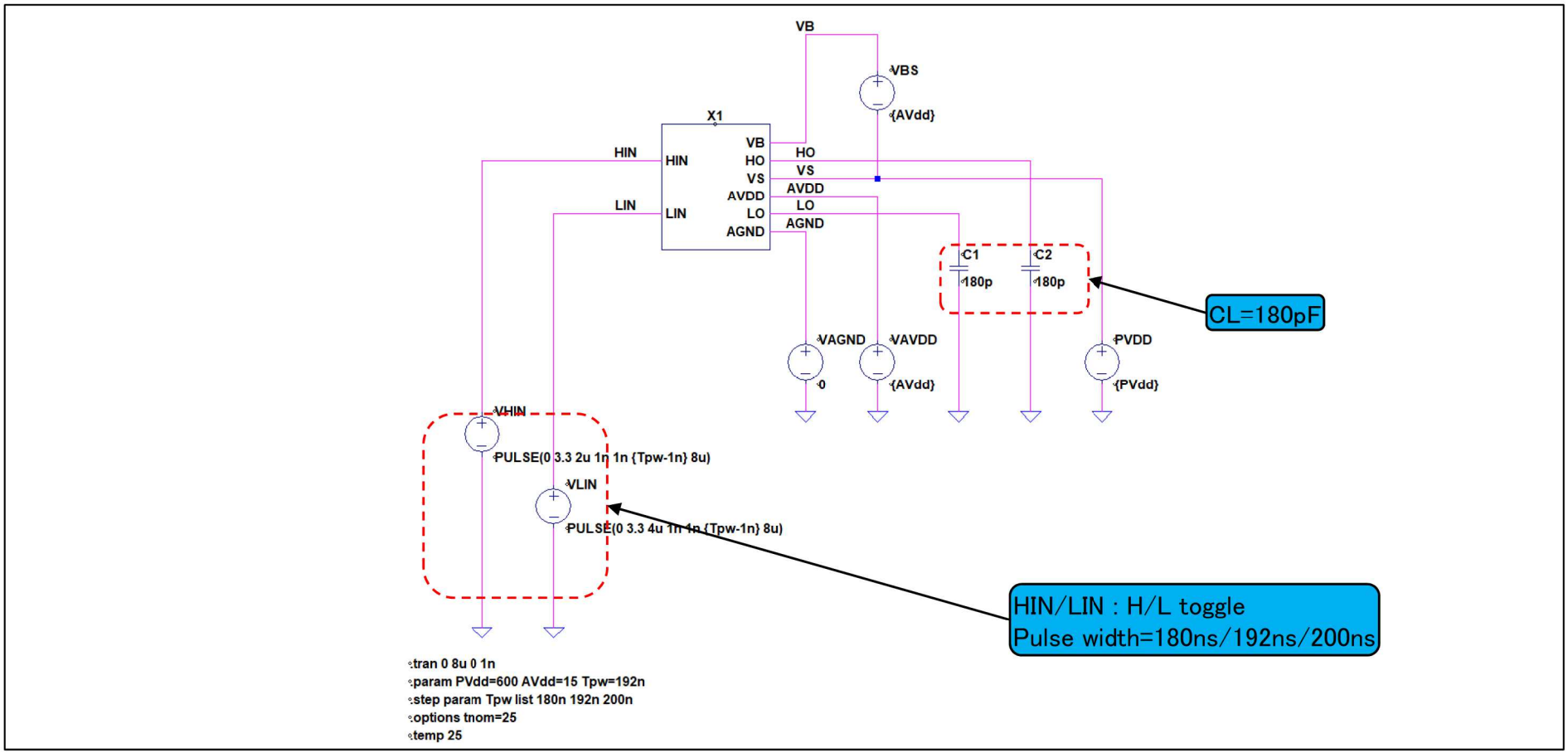
Simulation Result

Signal	Symbol	Unit	DS	Sim.
HO	Tr	ns	48.0	46.7
	Tf	ns	24.0	13.5
LO	Tr	ns	48.0	46.7
	Tf	ns	24.0	13.5



3.12.1 Input filter time at LIN/HIN for turn on and off

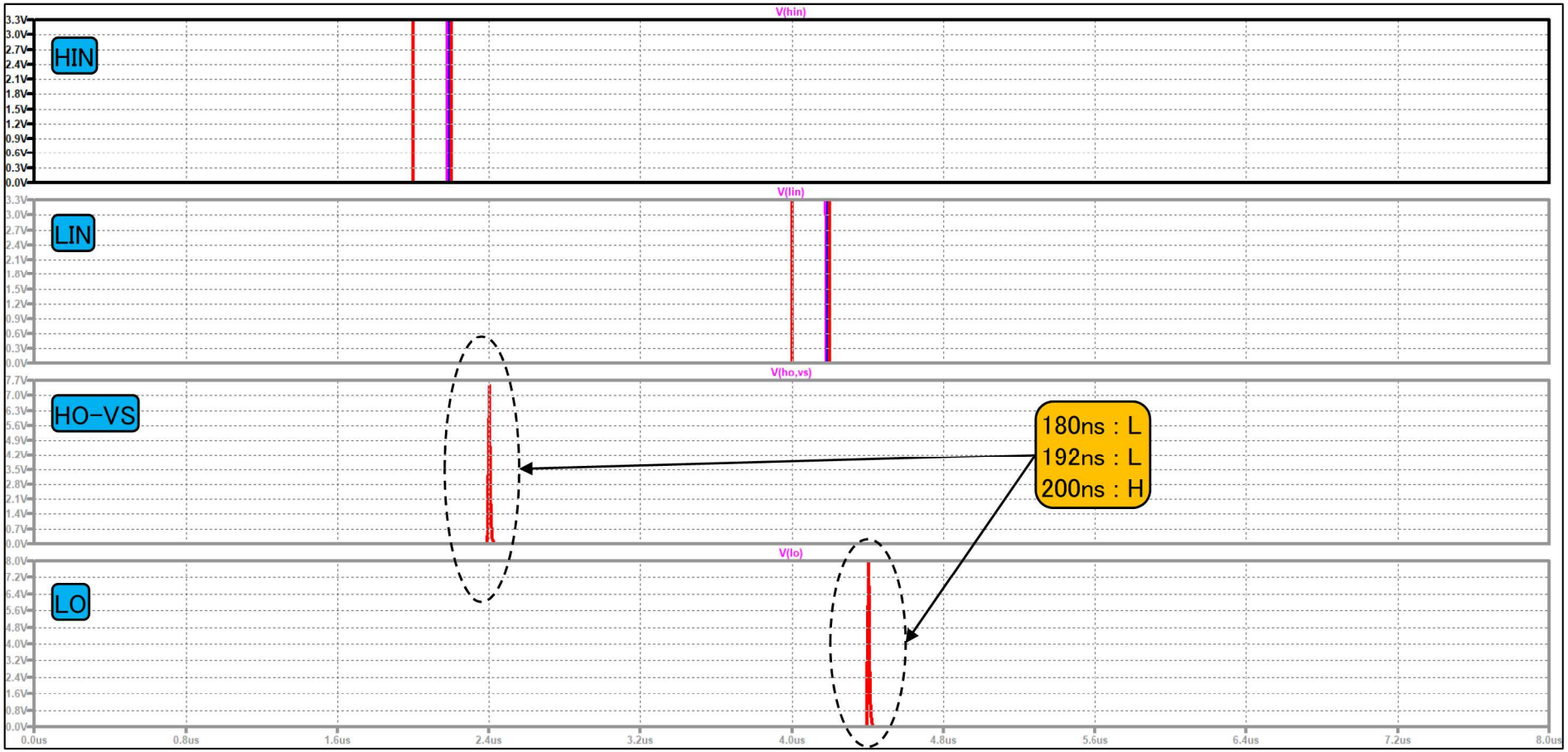
Test Bench



3.12.2 Input filter time at LIN/HIN for turn on and off

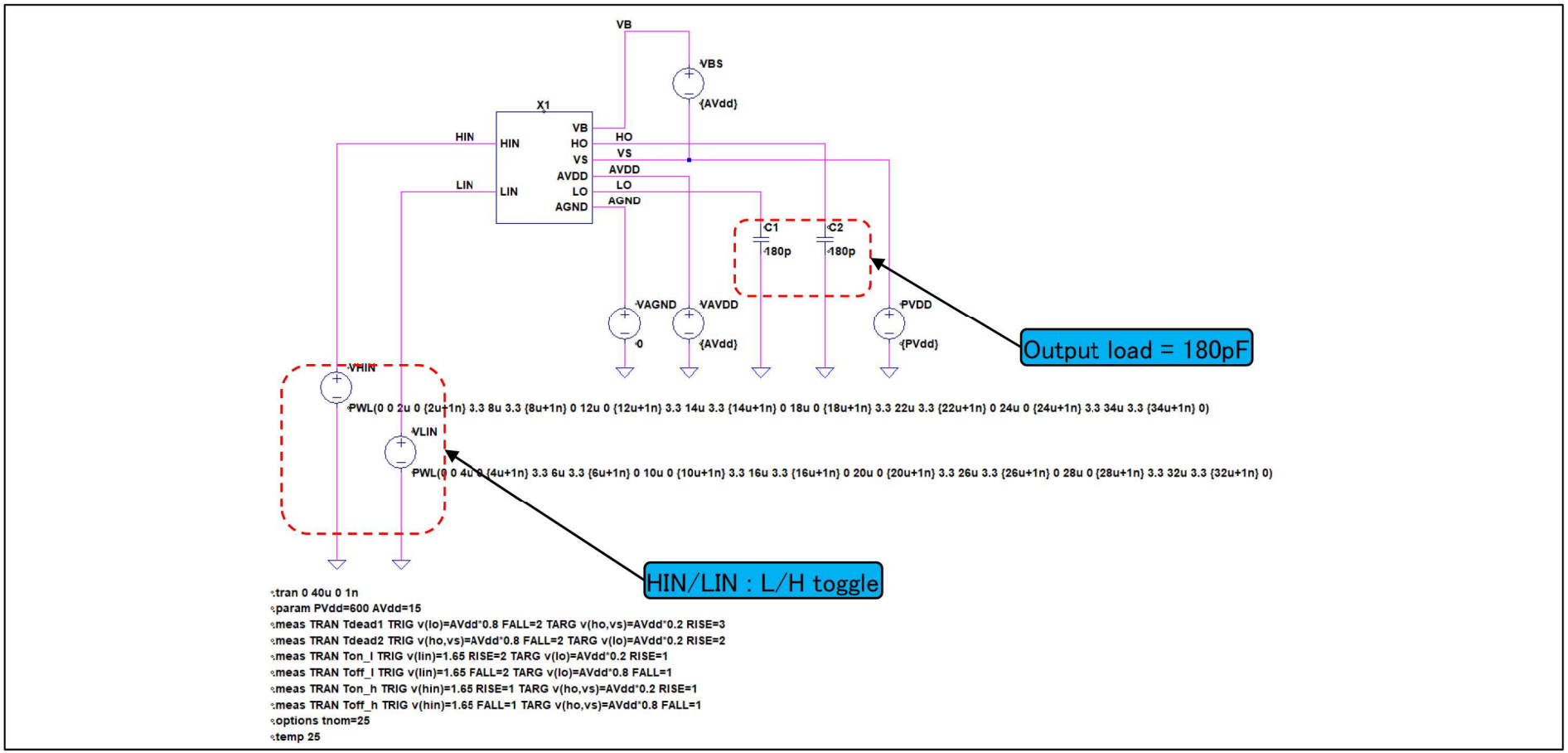
Simulation Result

Symbol	Unit	DS	Sim.
tFILIN	ns	192	192



3.13.1 Dead time

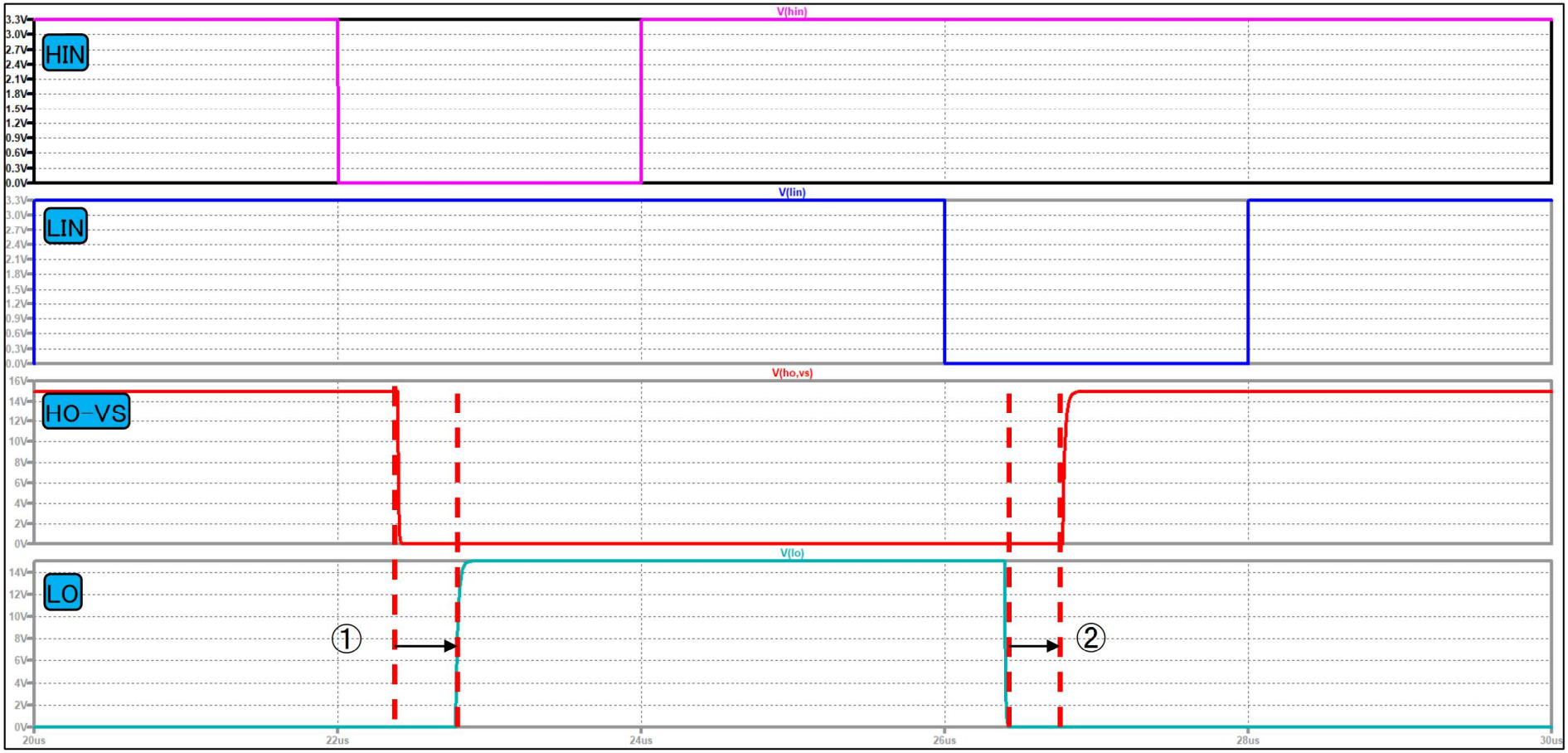
Test Bench



3.13.2 Dead time

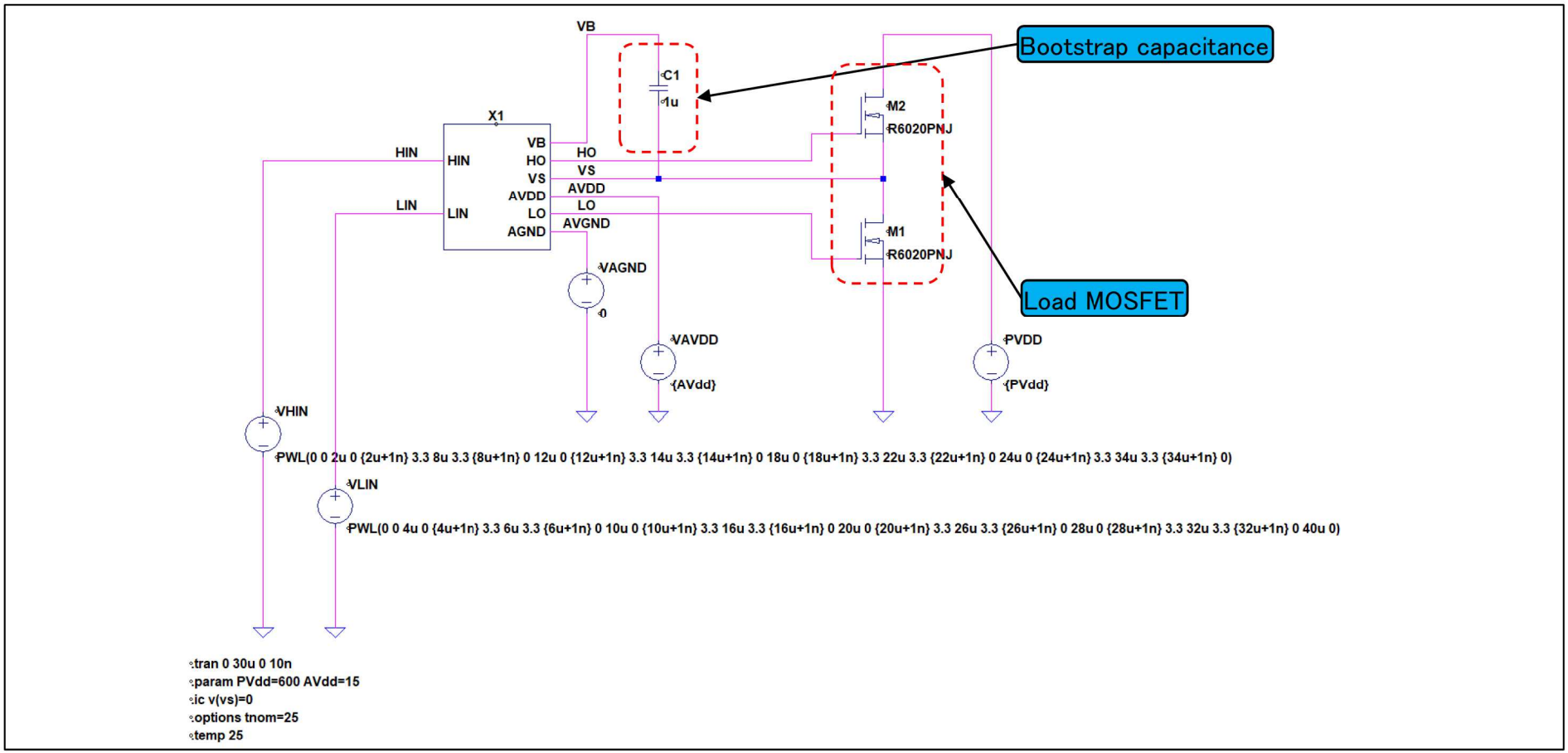
Simulation Result

Signal	Symbol	Unit	DS	Sim.
①	DT	ns	380	382
②		ns	380	382



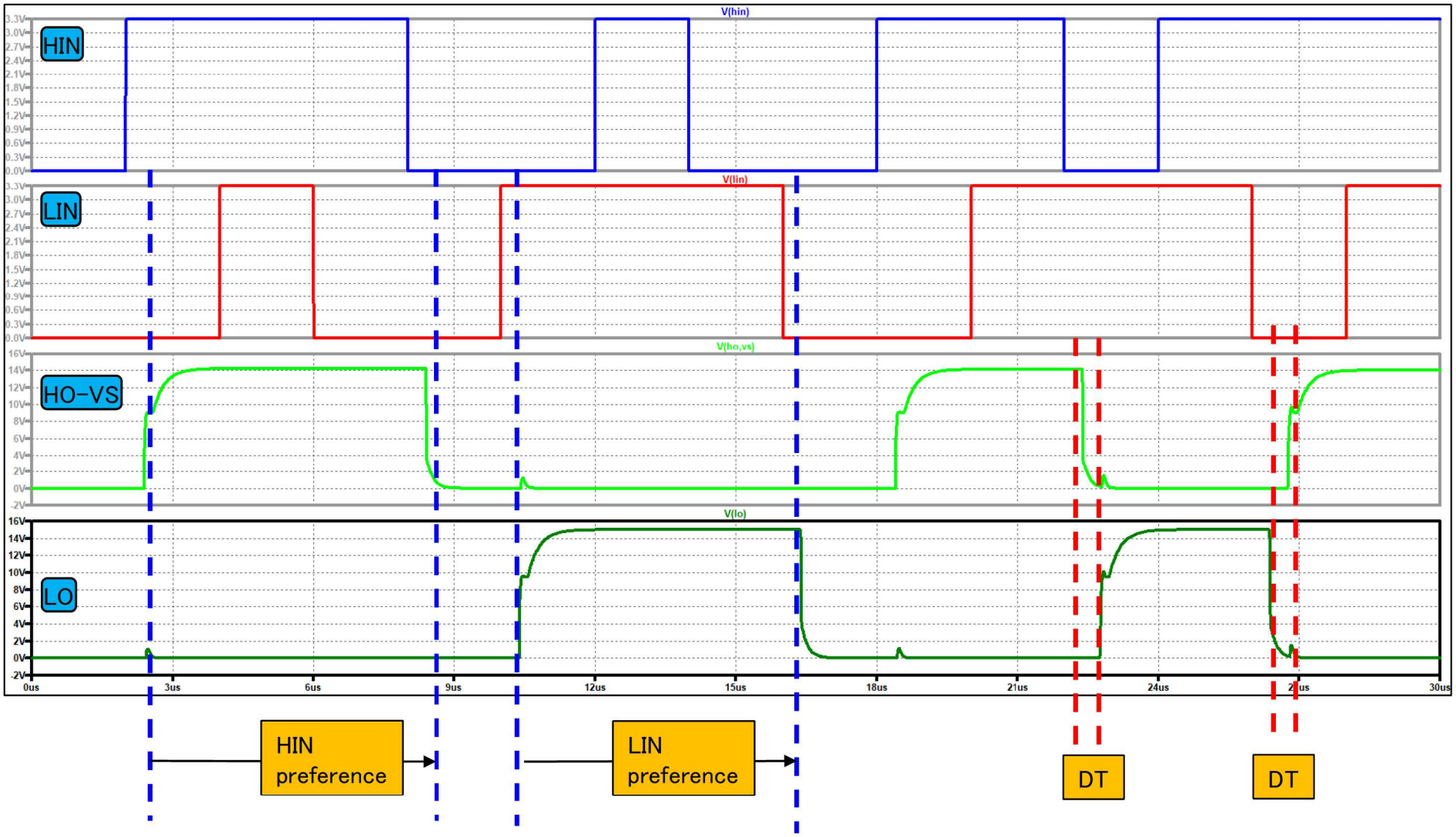
3.14.1 Function (Normal operation)

Test Bench



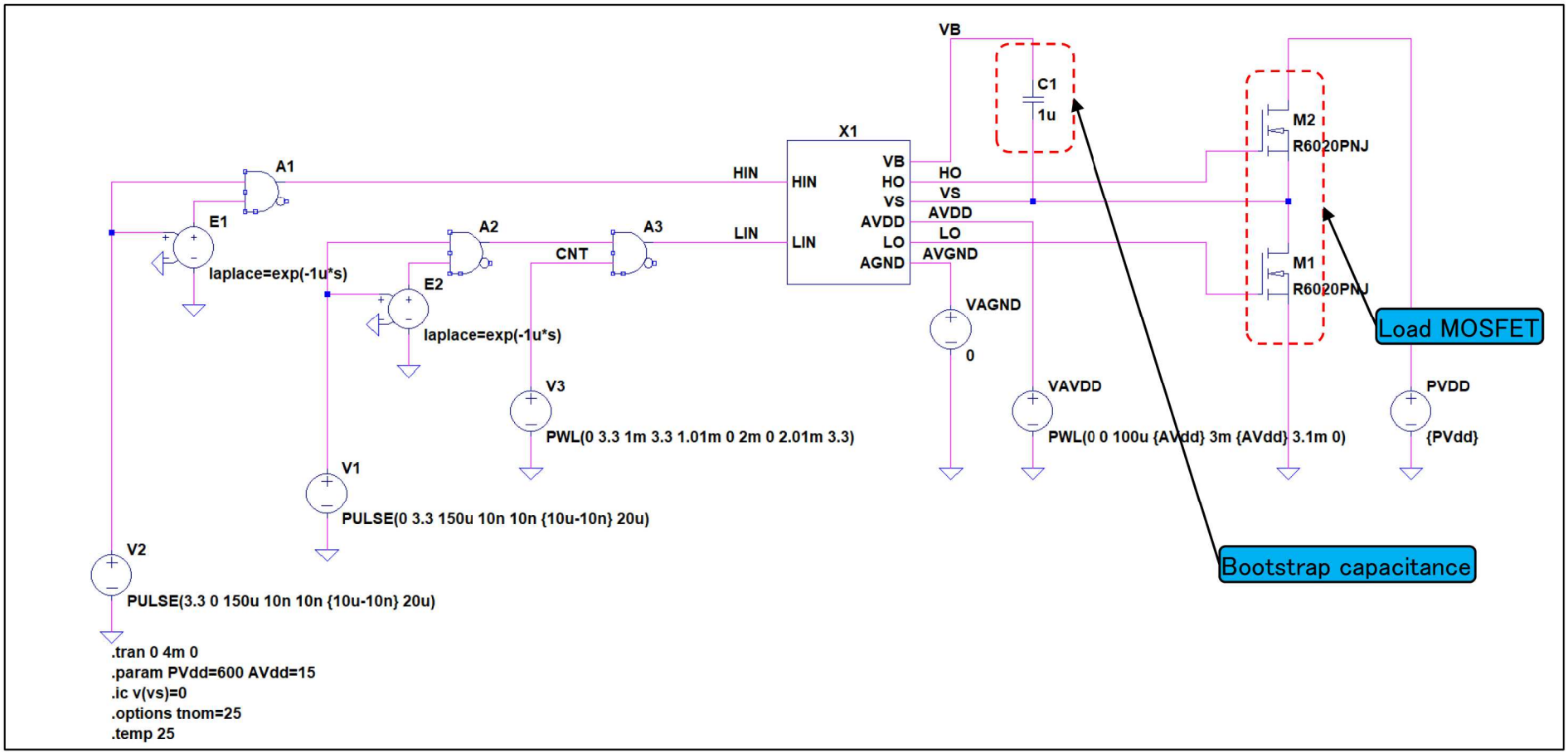
3.14.2 Function (Normal operation)

Simulation Result



3.15.1 Function（VDD/VBS UVLO operation）

Test Bench



3.15.2 Function (VDD/VBS UVLO operation)

Simulation Result