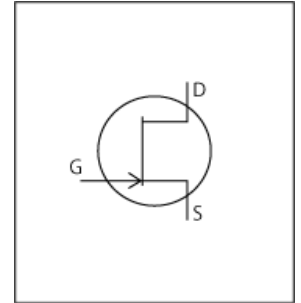
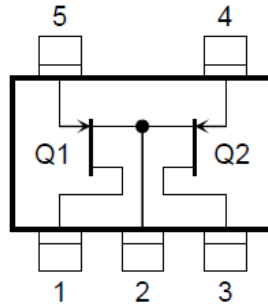


LTspice Model

N-Channel JFET

TOSHIBA

2SK2145



Model Information

Model A macro model based on general SPICE jfet model
Call Name MDC_2SK2145_LT
Pin Assign 1:D1 2:S1/S2 3:D2 4:G2 5:G1
File List Model Library MDC_2SK2145_LT01.lib
 Model Report MDC_2SK2145_LT.pdf (this file)

Verified Simulator Version LTspice version XVII
Note

References

The information which was used for modeling is as follow:

[Data Sheet]

- Date/Version 2014-03-01
- Product name 2SK2145
- Company name Toshiba Corporation
- Characteristics IdVds[Vgs], IdVgs[Temp], YfsId[Temp], CissVds[Vgs], CrssVgs[Vds]

Simulation Range

This table shows the range of evaluated simulation range that was not occurs any convergence problems in this area.

Item	Range			Unit
	Min.		Max.	
Gate-drain voltage (DC)	-50	to	0	V
Gate-source voltage (DC)	-50	to	0	V
Temperature	-55	to	125	deg C

JFET

○ : Implemented
 × : Not Implemented
 — : Not applicable

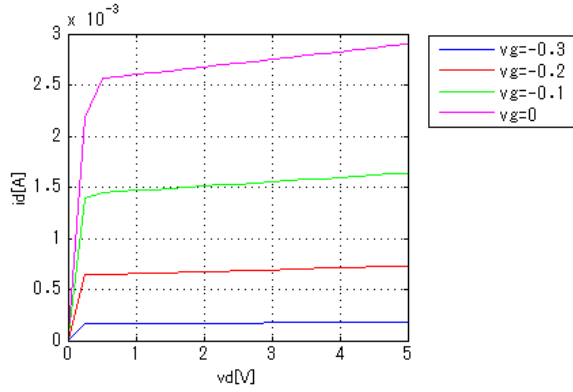
Model Functions Table
RANK=1

Functions	RANK	Implemented
ID-VDS-VGS	1	○
ID-VGS-TEMP	1	○
yfs-ID	1	○
Yos-ID	1	—
RDS(on)-ID	1	—
Capacitance	1	○
IG-VDG	1	—

Simulation results are following.
 Explanatory notes — : simulated

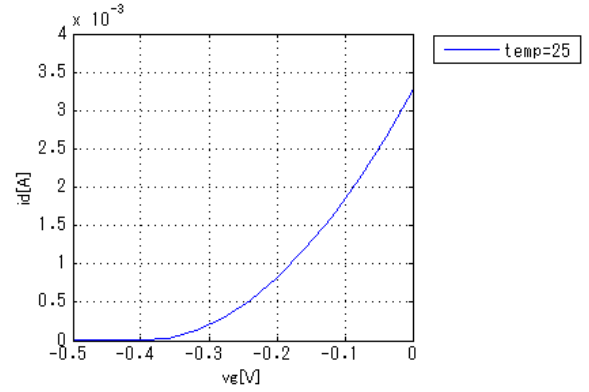
IdVds[Vgs]

Temp. = 25deg C



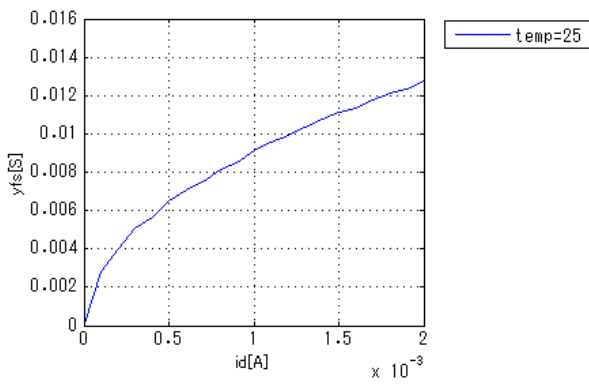
IdVgs[Temp]

$V_d = 10V$



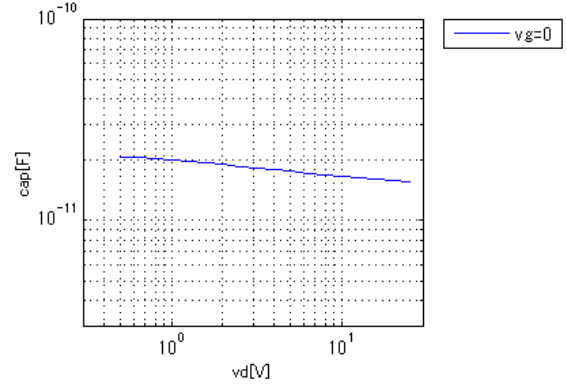
YfsId[Temp]

$v_d = 10V$



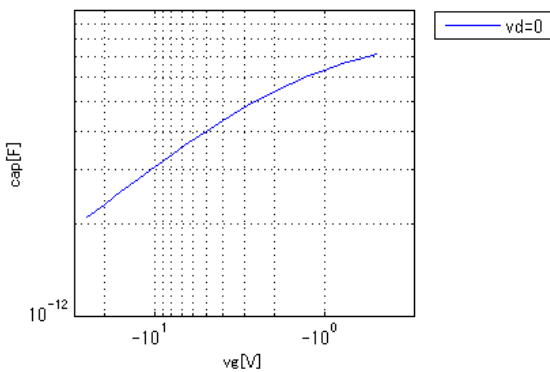
CissVds[Vgs]

freq = 1000000Hz



CrssVgs[Vds]

freq = 1000000Hz



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