

PSpice Model

Power Factor Correction Controller

On Semiconductor

NCP1654BD65R2G

Model Information

Model A macro model
Call Name MDC_NCP1654BD65R2G_PS
Pin Assign 1:GND 2:VM 3:CS 4:BO 5:VCNT 6:FB 7:VCC 8:DRV
File List Model Library MDC_NCP1654BD65R2G_PS.lib
 Model Report MDC_NCP1654BD65R2G_PS.pdf(this file)
Verified Simulator Version PSpice 17.2
Note

References

The information which was used for modeling is as follow:

[Data Sheet]

- Date/Version March 2021 Rev. 6
- Product name NCP1654BD65R2G
- Company name ON Semiconductor

[Characteristics listed]

- Characteristics Roh, Rol, Tr, Tf, Vref
Is(ocp), Ics(opl1), Ics(opl2)
Dcycle, Fsw, Vboh, Vbol, Vcc(on), Vcc(off)

Simulation Condition

This table shows the range of evaluated simulation range that was not occurs any convergence problems in this area.

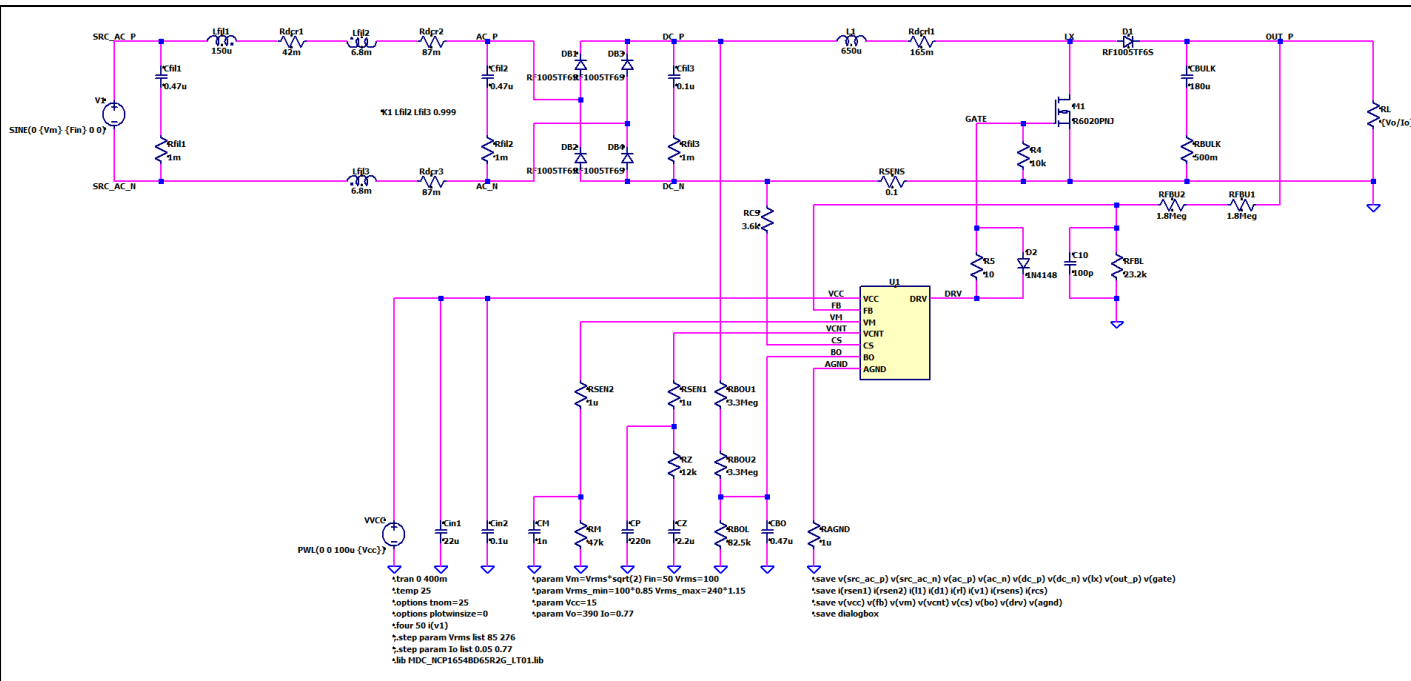
Item	Condition	Unit
Temperature	25	deg C

Model Functions Table

Functions	Implemented
Programmable Overcurrent Protection	○
Brown-Out Detection	○
Overvoltage Protection	○
Soft Start	○
Continuous Conduction Mode	○
Average Current-Mode or Peak Current-Mode Operation	○
Programmable Overpower Limitation	○
Undervoltage Detection for Open Loop Detection (shutdown)	○
Inrush Currents Detection	○

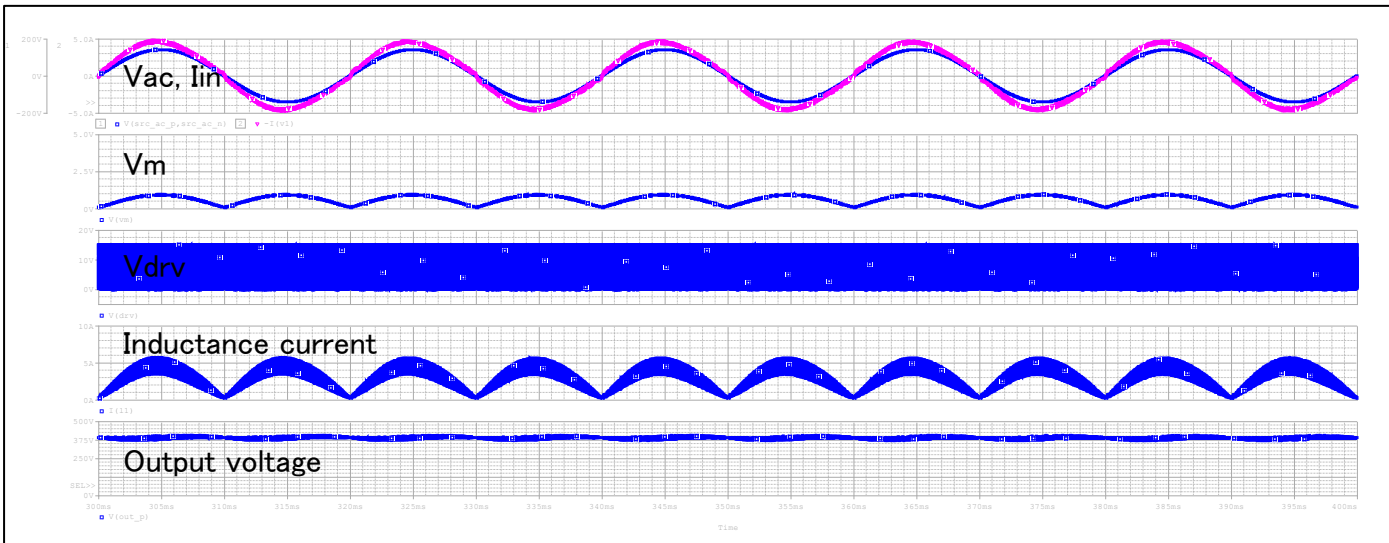
Power Factor Correction (CCM) Testbench (Vrms=100[V] Vout=390[V] Iout=0.77[A])

Referred to Data Sheet



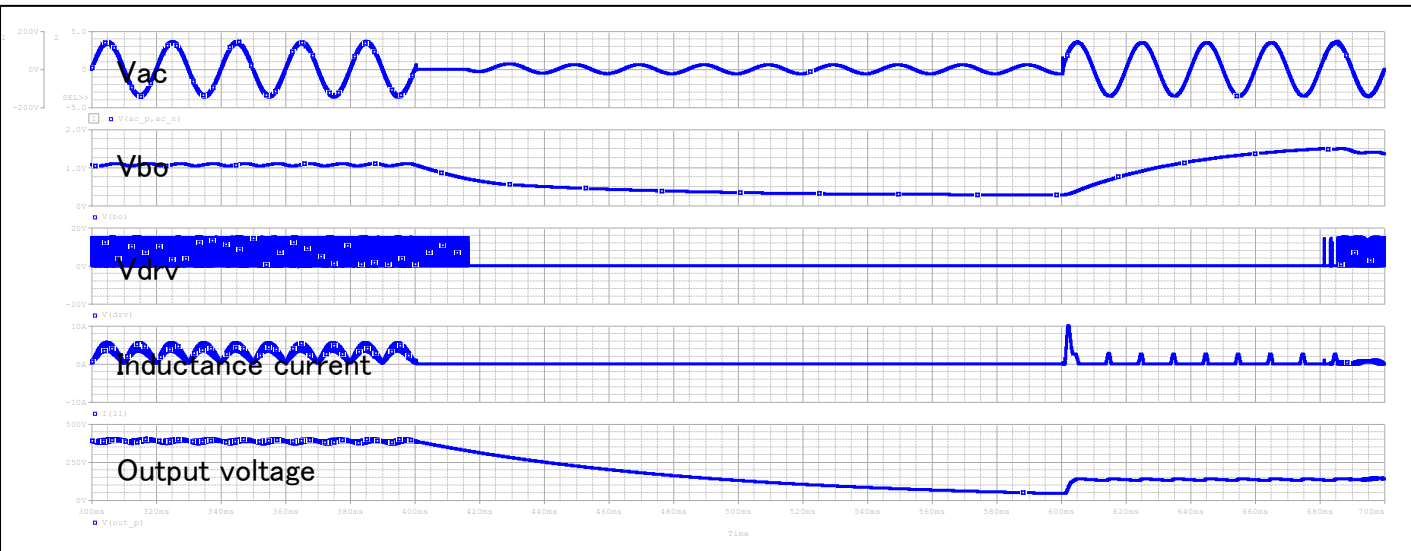
Simulation results are following.
Explanatory notes — : simulated

Power Factor Correction (CCM) Testbench (Vrms=100[V] Vout=390[V] Iout=0.77[A])



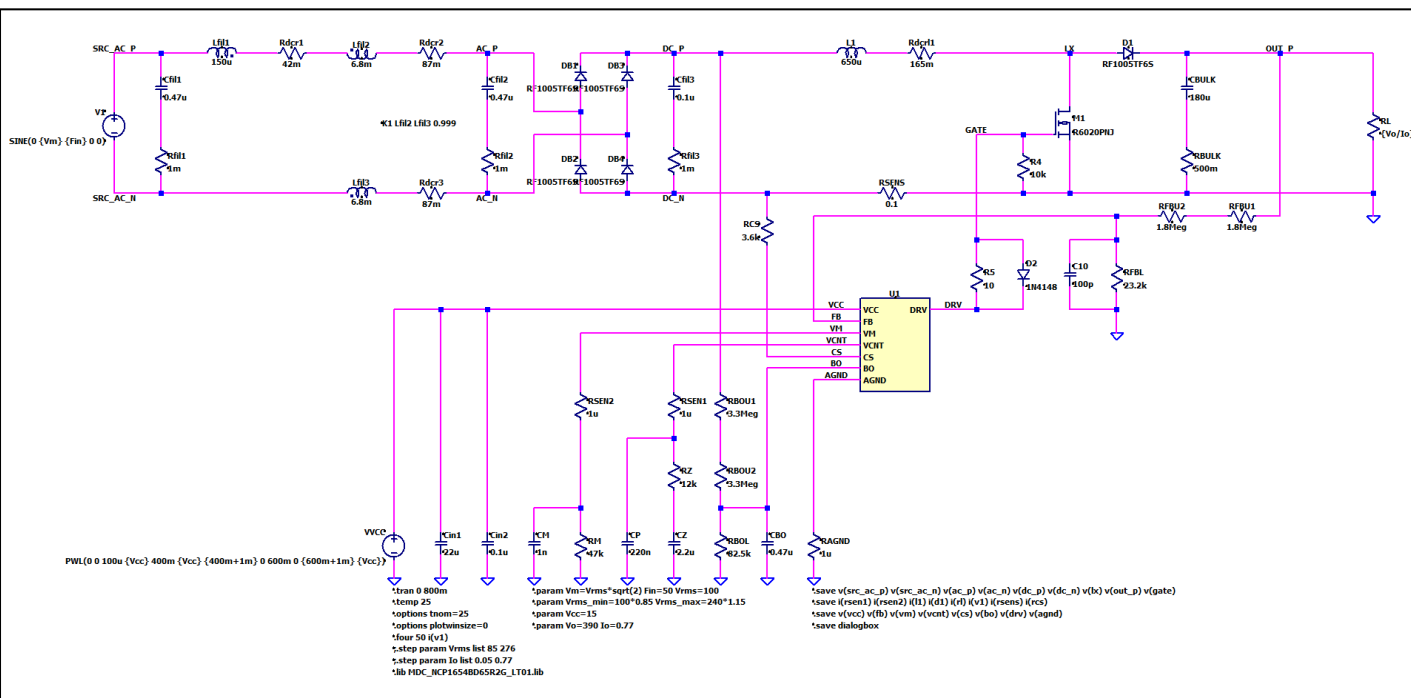
Simulation results are following.
Explanatory notes — : simulated

Brown-out Testbench (Vrms=100[V] Vout=390[V] Iout=0.77[A])



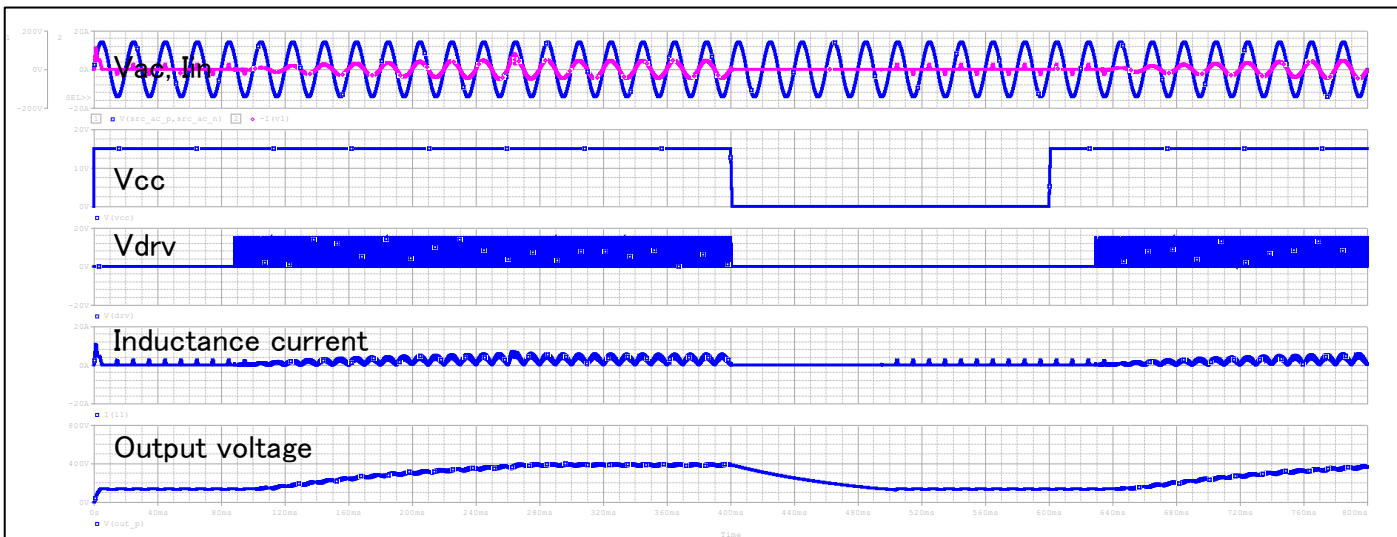
Vcc UVLO Testbench (Vrms=100[V] Vout=390[V] Iout=0.77[A])

Referred to Data Sheet



Simulation results are following.
Explanatory notes — : simulated

Brown-out Testbench (Vrms=100[V] Vout=390[V] Iout=0.77[A])



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