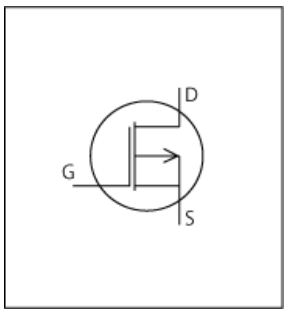
LTspice Model
PMOS
Infineon
IRF4905LPBF



Model Information

Model	A macro model based on BSIM3 model	
Call Name	MDC_IRF4905LPBF_LT	
Pin Assign	1:G 2:D 3:S 4:D	
File List	Model Library	MDC_IRF4905LPBF_LT01.lib
	Model Report	MDC_IRF4905LPBF_LT.pdf (this file)
Verified Simulator Version		LTspice version XVII
Note		

References

The information which was used for modeling is as follow:

[Data Sheet]

- ●Date/Version Unknown
- ●Product name IRF4905LPBF
- ●Company name Infineon Technologies AG
- ●Characteristics IdVgs[Temp],IdVds[Vgs],Crss,Coss,Ciss,VgsQg[Vdd],Rds(on)Temp[Id],VthTemp[Id],IsVsd[Temp],tdon,tdoff,tf,tr

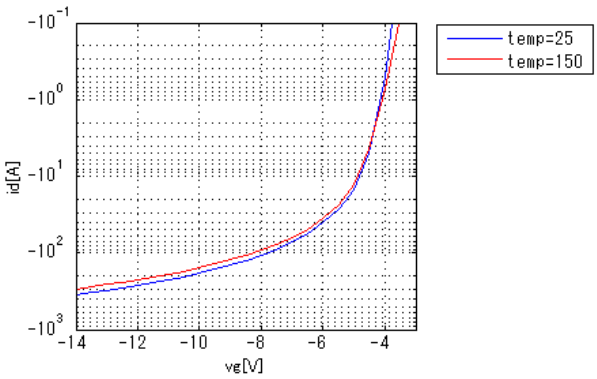
Simulation Range

This table shows the range of evaluated simulation range that was not occurs any convergence problems in this area.

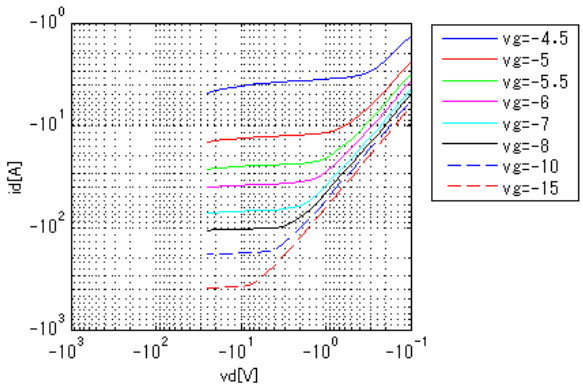
Item	Range			Unit
	Min.		Max.	
Drain-source voltage (DC)	0	to	-55	V
Gate-source voltage (DC)	0	to	-20	V
Temperature	-55	to	150	deg C

Simulation results are following.
Explanatory notes — : simulated

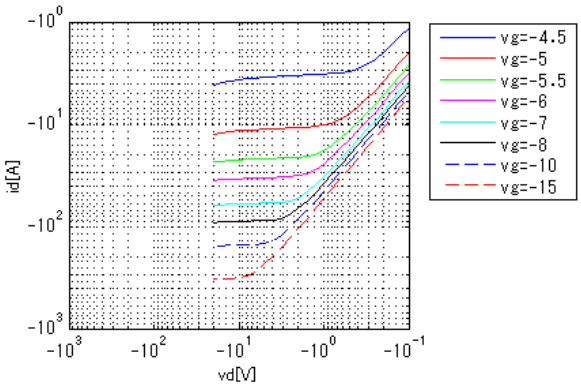
IdVgs[Temp]
Vds = -25V



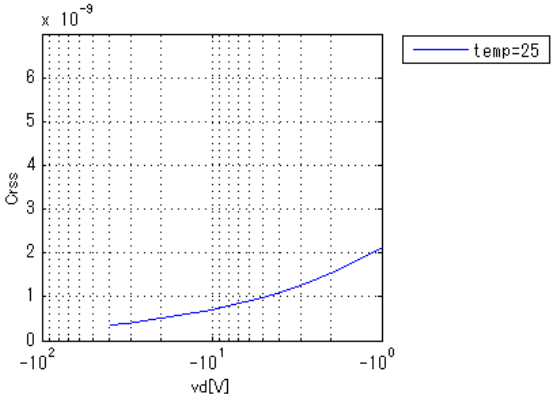
IdVds[Vgs]
Temp. = 25deg C



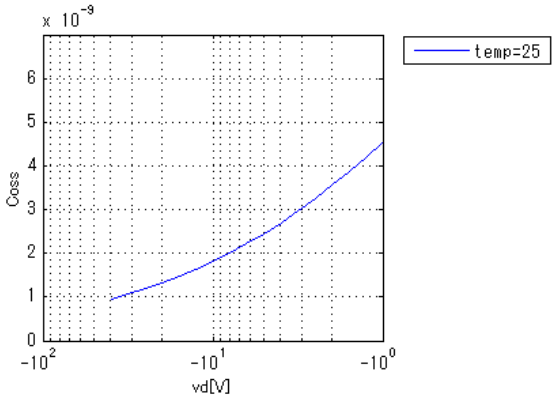
IdVds[Vgs]
Temp. = 150deg C



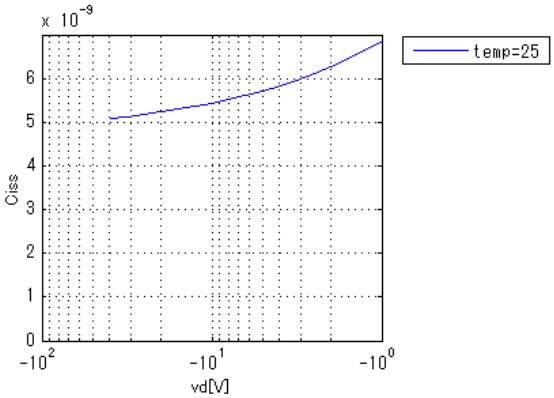
Crss
Freq. = 1MHz



Coss
Freq. = 1MHz

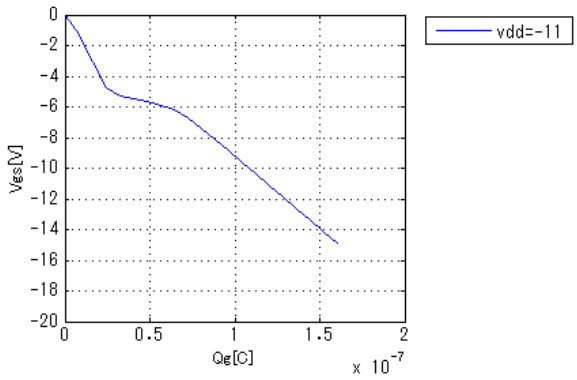


Ciss
Freq. = 1MHz

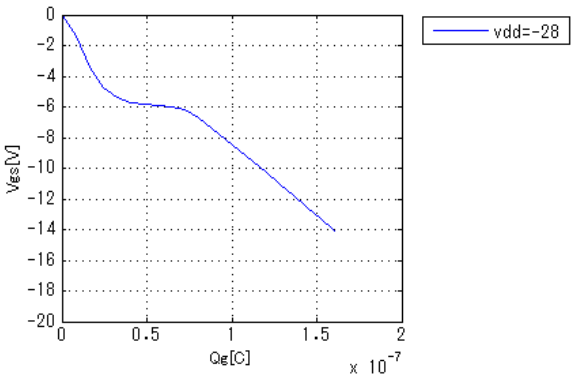


Simulation results are following.
Explanatory notes — : simulated

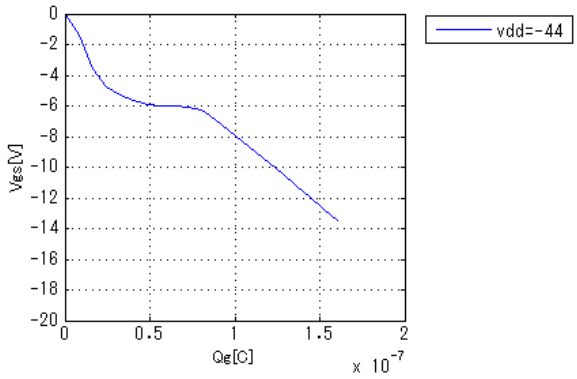
VgsQg[Vdd]
Id = -42A



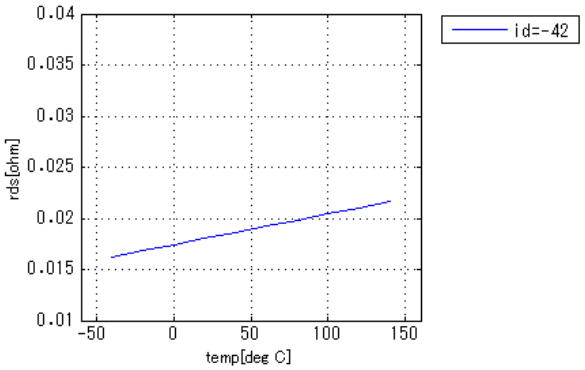
VgsQg[Vdd]
Id = -42A



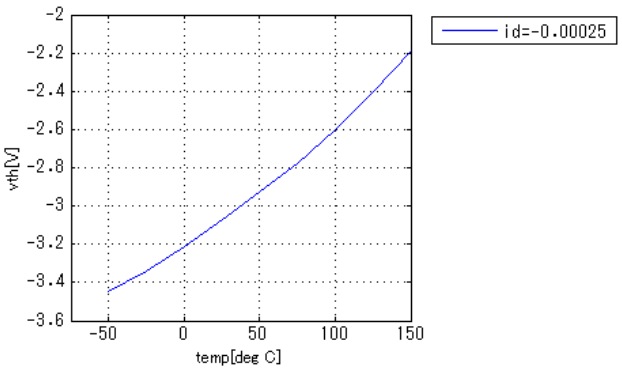
VgsQg[Vdd]
Id = -42A



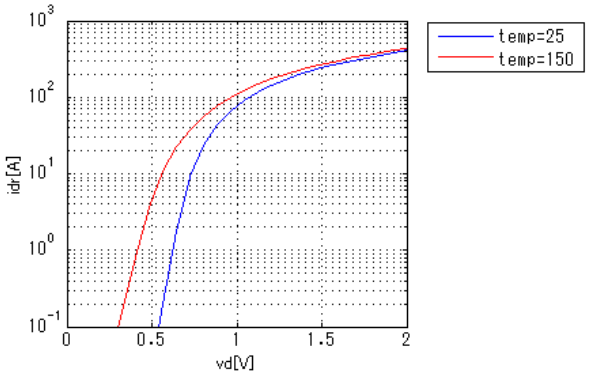
Rds(on)Temp[Id]
Vgs = -10V



VthTemp[Id]
Vd = Vg



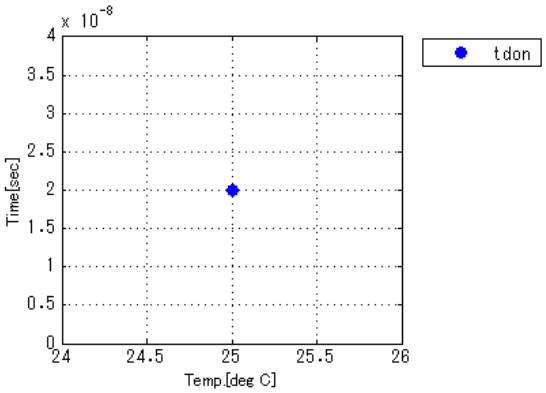
IsVsd[Temp]



Simulation results are following.
Explanatory notes — : simulated

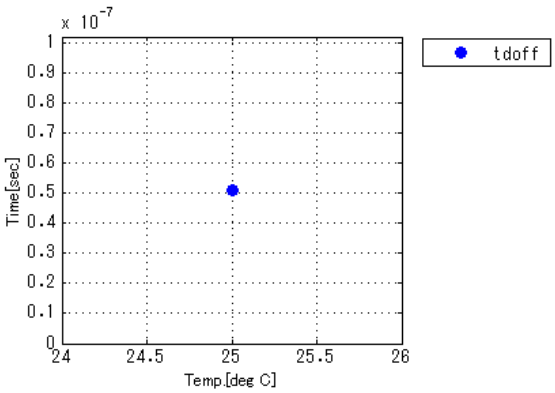
tdon

Vdd = -28V, Id = -42A, +Vg = 0V, -Vg = -10V, Rg = 0.001ohm



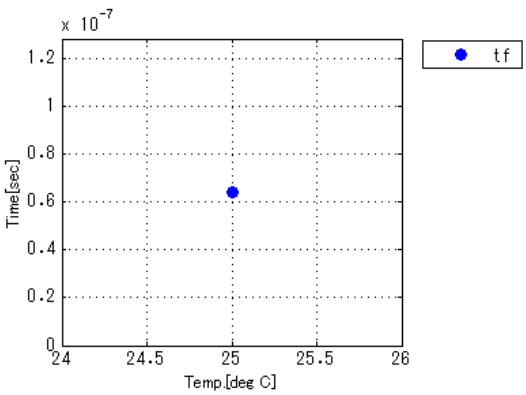
tdoff

Vdd = -28V, Id = -42A, +Vg = 0V, -Vg = -10V, Rg = 0.001ohm



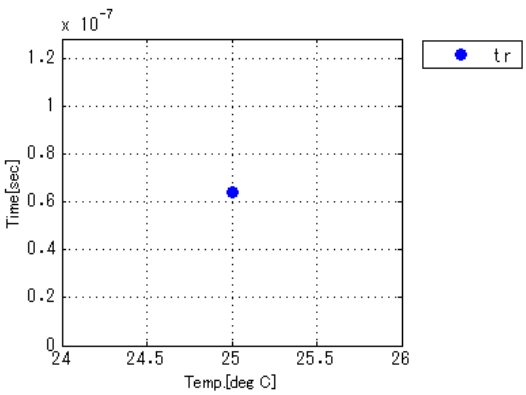
tf

Vdd = -28V, Id = -42A, +Vg = 0V, -Vg = -10V, Rg = 0.001ohm



tr

Vdd = -28V, Id = -42A, +Vg = 0V, -Vg = -10V, Rg = 0.001ohm



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