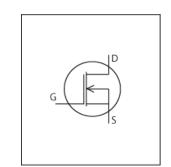


LTspice Model NMOS Infineon IPW65R080CFDA



Model Information

Model A macro model based on BSIM3 model

Call Name MDC IPW65R080CFDA LT

Pin Assign 1:G 2:D 3:S

File List Model Library MDC_IPW65R080CFDA_LT01.lib

Model Report MDC_IPW65R080CFDA_LT.pdf (this file)

Verified Simulator Version

Note

LTspice version XVII

References

The information which was used for modeling is as follow:

[Data Sheet]

Date/Version Rev. 2.1

● Product name IPW65R080CFDA

■Company name Infineon Technologies AG

● Characteristics IdVds[Vgs],Rds(on)Id[Vgs],Rds(on)Temp[Id],IdVgs[Temp],Vg

sQg[Vdd],IsVsd[Temp],Ciss,Coss,Crss,tdon,tdoff,tf,tr

Simulation Range

This table shows the range of evaluated simulation range that was not occurs any convergence problems in this area.

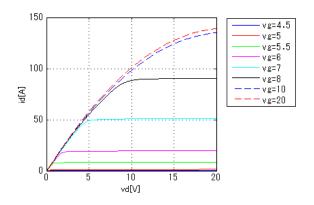
| Item | Range | | | Unit |
|---------------------------|-------|----|------|-------|
| | Min. | | Max. | |
| Drain-source voltage (DC) | 0 | to | 650 | V |
| Gate-source voltage (DC) | 0 | to | 20 | V |
| Temperature | -40 | to | 150 | deg C |



Simulation results are following. Explanatory notes — : simulated

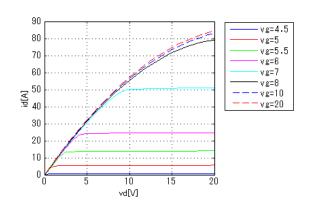
IdVds[Vgs]

Temp. = 25deg C

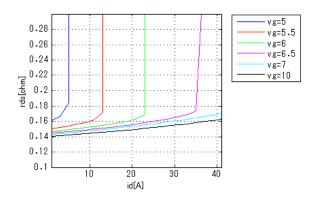


IdVds[Vgs]

Temp. = 125deg C

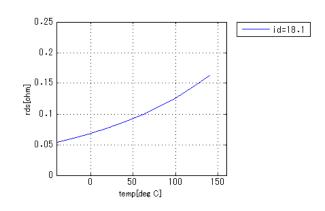


Rds(on)Id[Vgs]



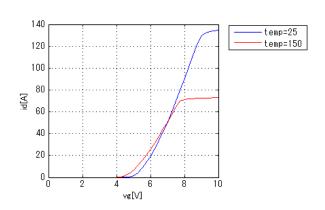
Rds(on)Temp[Id]

Vgs = 10V



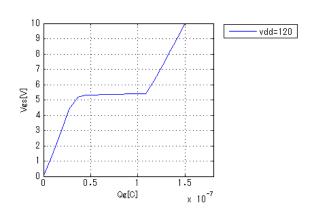
IdVgs[Temp]

Vds = 20V



VgsQg[Vdd]

Id = 6.5A

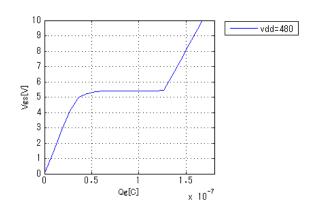




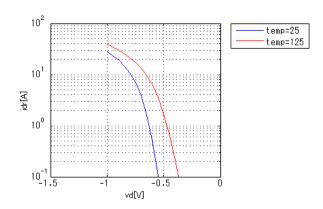
Simulation results are following. Explanatory notes — : simulated

VgsQg[Vdd]

Id = 6.5A

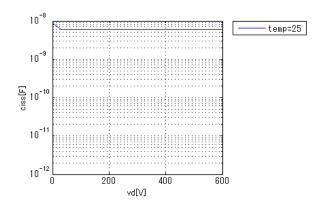


IsVsd[Temp]



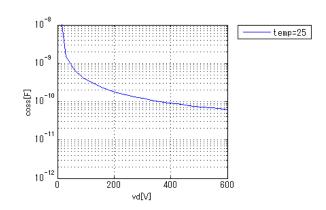
Ciss

Freq. = 1MHz



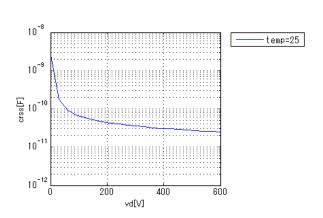
Coss

Freq. = 1MHz



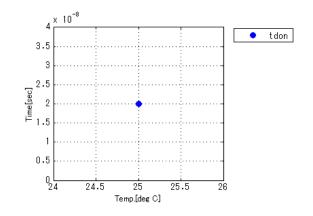
Crss

Freq. = 1MHz



tdon

Vdd = 400V, Id = 26.3A, +Vg = 13V, -Vg = 0V, Rg = 1.8ohm

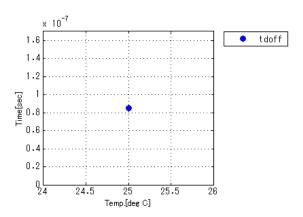




Simulation results are following. Explanatory notes — : simulated

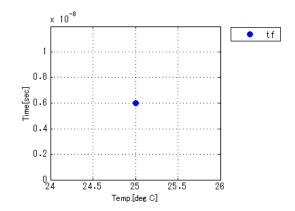
tdoff

Vdd = 400V, Id = 26.3A, +Vg = 13V, -Vg = 0V, Rg = 1.8ohm



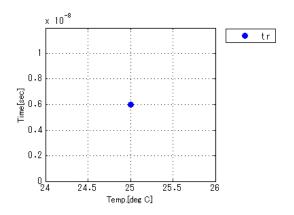
tf

Vdd = 400V, Id = 26.3A, +Vg = 13V, -Vg = 0V, Rg = 1.80hm



tr

Vdd = 400V, Id = 26.3A, +Vg = 13V, -Vg = 0V, Rg = 1.8ohm





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MoDeCH Inc.

Head Office

Location: Mitsuiseimei Hachioji Bldg., 5-15 Yokoyama-cho, Hachioji-Shi, Tokyo 192-0081, Japan

Tel:+81-42-656-3360

E-Mail:model-on-support@modech.co.jp

URL:http://www.modech.com/en/