

LTspice Model

Voltage Detector

ABLIC Inc.

S-80929CNMC-G8ZT2G

Model Information

Model	A macro model
Call Name	MDC_S-80929CNMC-G8ZT2G_LT
Pin Assign	1:OUT 2:VDD 3:VSS 4:NC 5:CD
File List	Model Library MDC_S-80929CNMC-G8ZT2G_LT01.lib Model Report MDC_S-80929CNMC-G8ZT2G_LT.pdf(this file)

Verified Simulator Version LTspice version XVII
Note

References

The information which was used for modeling is as follow:

[Data Sheet]	
●Date/Version	Unknown
●Product name	S-80929CNMC-G8ZT2G
●Company name	ABLIC

[Characteristics listed]	
●Characteristics	VDET, VHYS, ISS, IOUT, ILEAK, tD

Simulation Condition

This table shows the range of evaluated simulation range that was not occurs any convergence problems in this area.

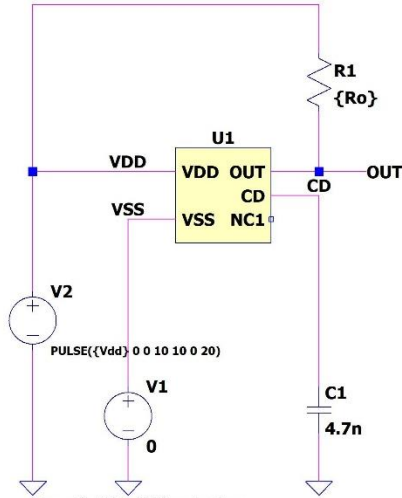
Item	Condition			Unit
	Min	Typ	Max	
Supply Voltage	0.7		10.0	V
Temperature		25		deg C

Model Functions Table

Functions	Implemented
Voltage detection with delay circuit	○
Nch open-drain output	○

Voltage detect function (Vdd = 10.0[V], Rout=100[kohm], Cd=4.7[nF]) Testbench

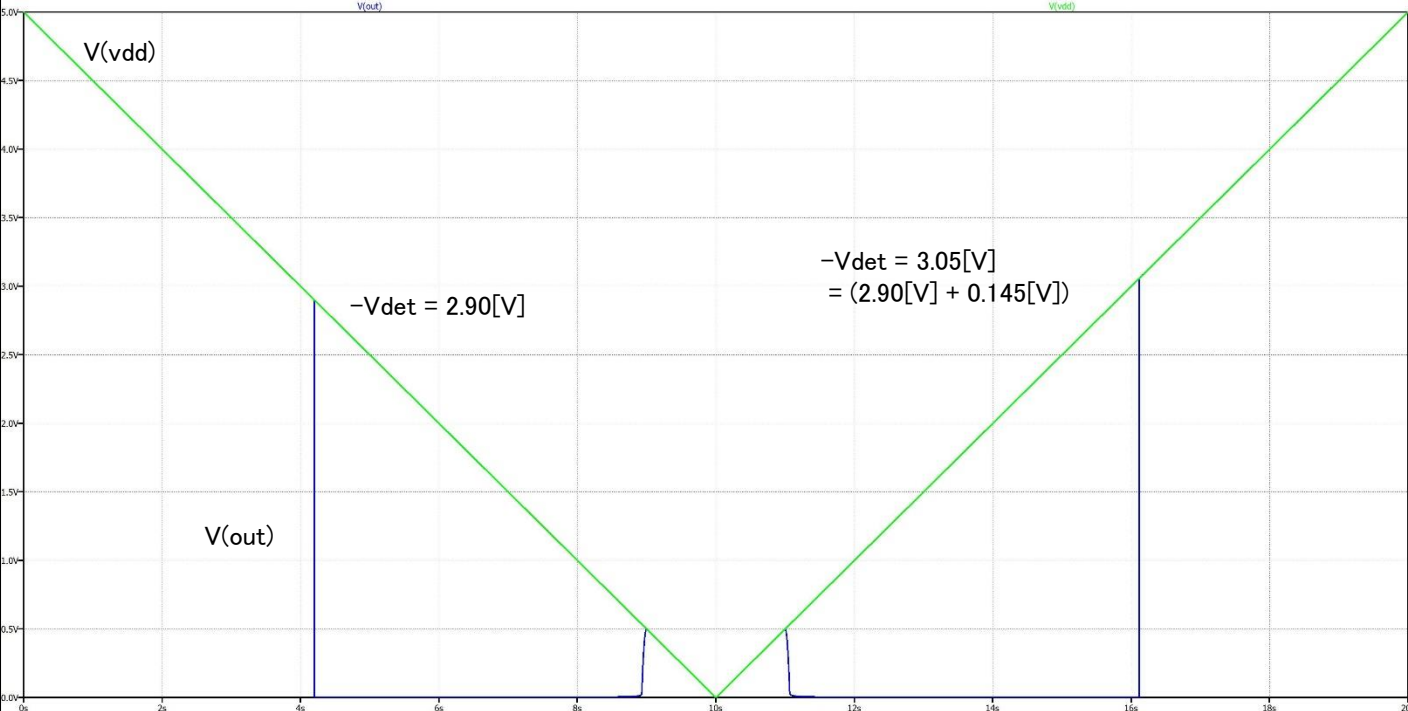
Referred to Data Sheet



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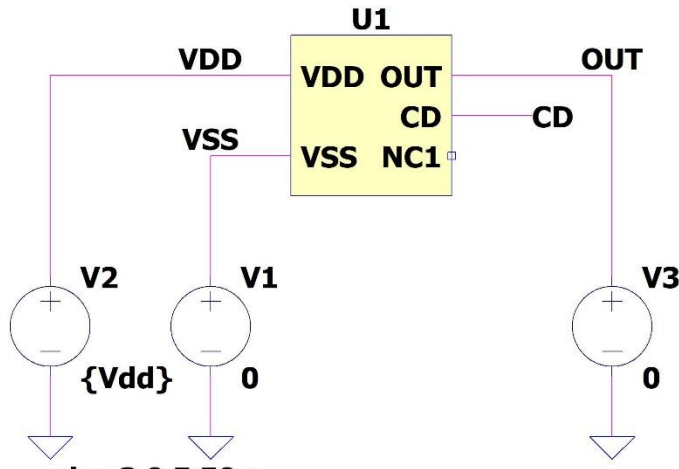
.tran 0 20 0 100u startup
.temp 25
.options tnom=25 plotwinsize=0 method=trapezoidal
.param Vdd=5.0 Vdet=2.9 Ro=100k Vhys=0.145
.meas TRAN ViLH FIND v(vdd) WHEN v(out)=Vdet/2 RISE=1
.meas TRAN ViHL FIND v(vdd) WHEN v(out)=Vdet/2 FALL=1
.meas TRAN Vhys PARAM ViLH-ViHL
.meas TRAN TdLH TRIG v(vdd)={Vdet+Vhys} RISE=1 TARG v(out)=Vdet/2 RISE=1
.lib MDC_S-80929CNMC-G8ZT2G_LT01.lib

```



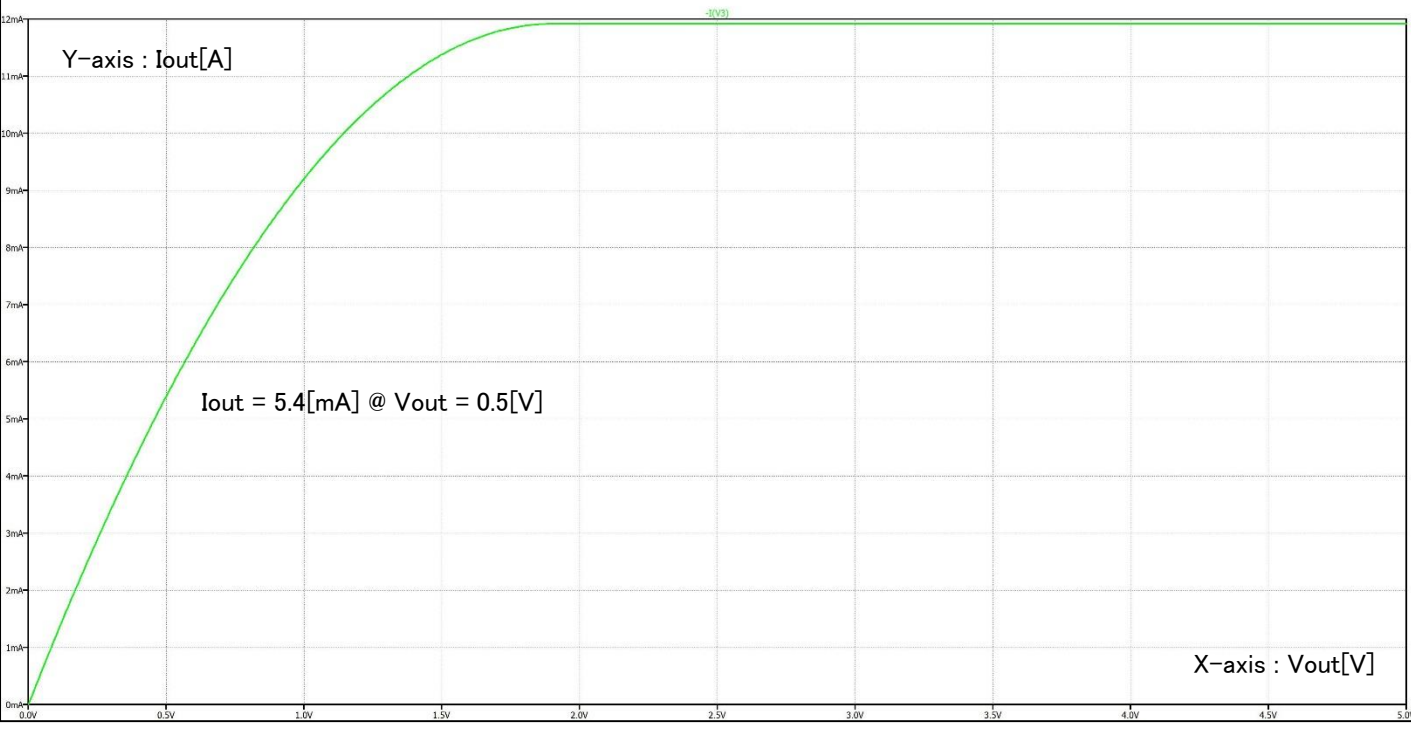
Buck converter Operation (Vdd = 2.4[V]) Testbench

Referred to Data Sheet



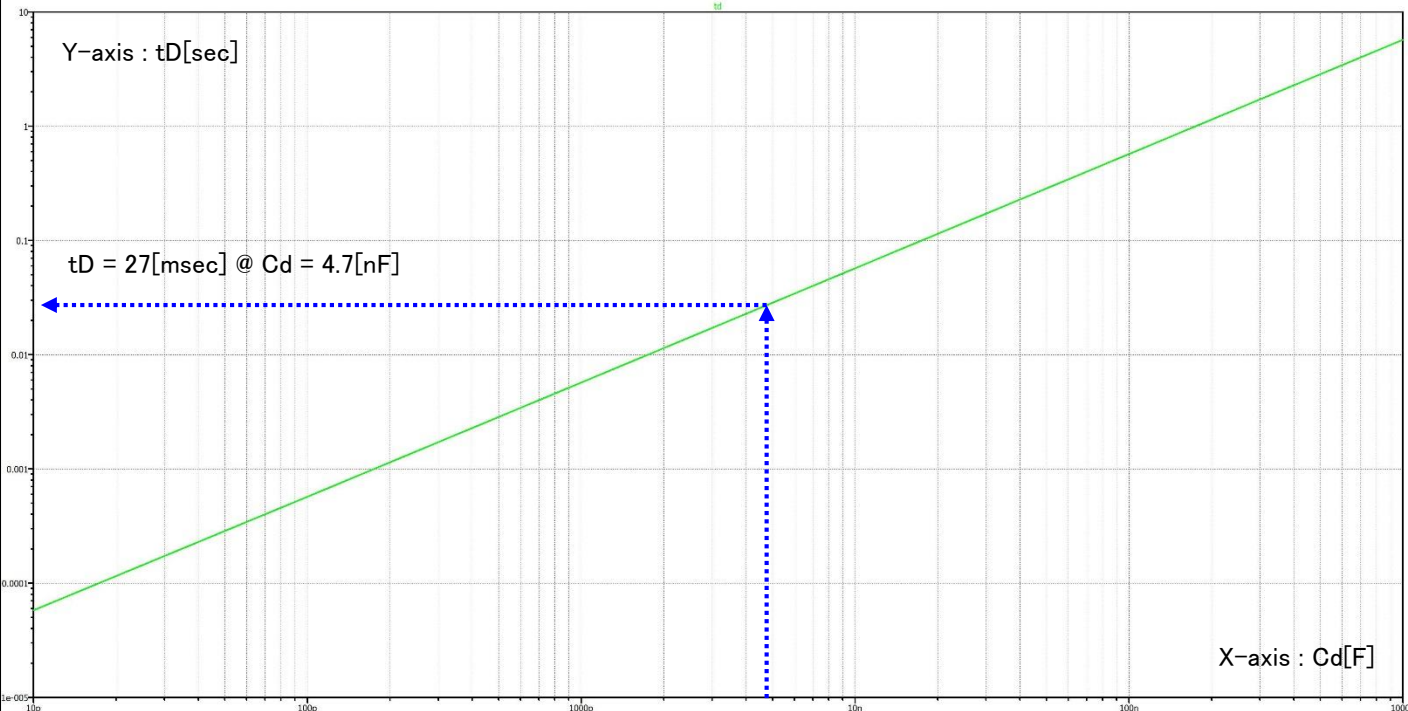
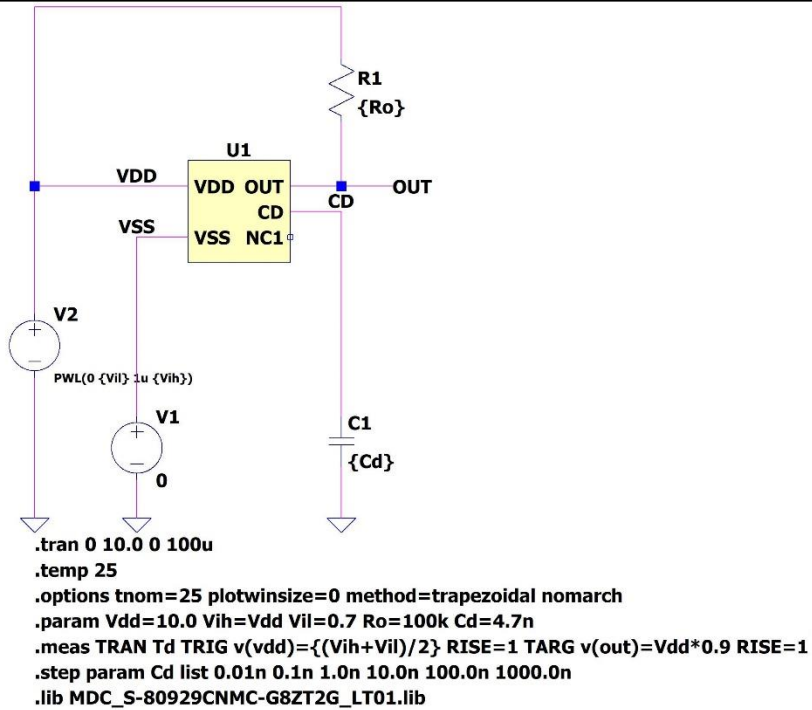
```

.dc v3 0 5 50m
.temp 25
.options tnom=25 plotwinsize=0 method=trapezoidal
.param Vdd=2.4
;.step param Vdd list 1.2 2.4 3.6 4.8 6.0
.lib MDC_S-80929CNMC-G8ZT2G_LT01.lib
    
```



Buck converter Operation (Vdd = 10.0[V], Rout=100[kohm]) Testbench

Referred to Data Sheet



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