

# LTspice Model

## Dual-Channel Synchronous Rectifier Controller

### Texas Instruments Inc.

### UCC24624

#### Model Information

<b>Model</b>	A macro model		
<b>Call Name</b>	MDC_UCC24624_LT		
<b>Pin Assign</b>	1:VG1 2:PGND 3:REG 4:VD1 5:VSS 6:VD2 7:VDD 8:VG2		
<b>File List</b>	Model Library	MDC_UCC24624_LT01.lib	
	Model Report	MDC_UCC24624_LT.pdf(this file)	
<b>Verified Simulator Version</b>	LTspice XVII		
<b>Note</b>			

#### References

The information which was used for modeling is as follow:

[Data Sheet]	
●Date/Version	18-Nov-2020
●Product name	UCC24624
●Company name	Texas Instruments Inc.

[Characteristics listed]	
●Characteristics	RVG_PU, RVG_PD, VREG tdVGON, tdVGOFF

#### Simulation Condition

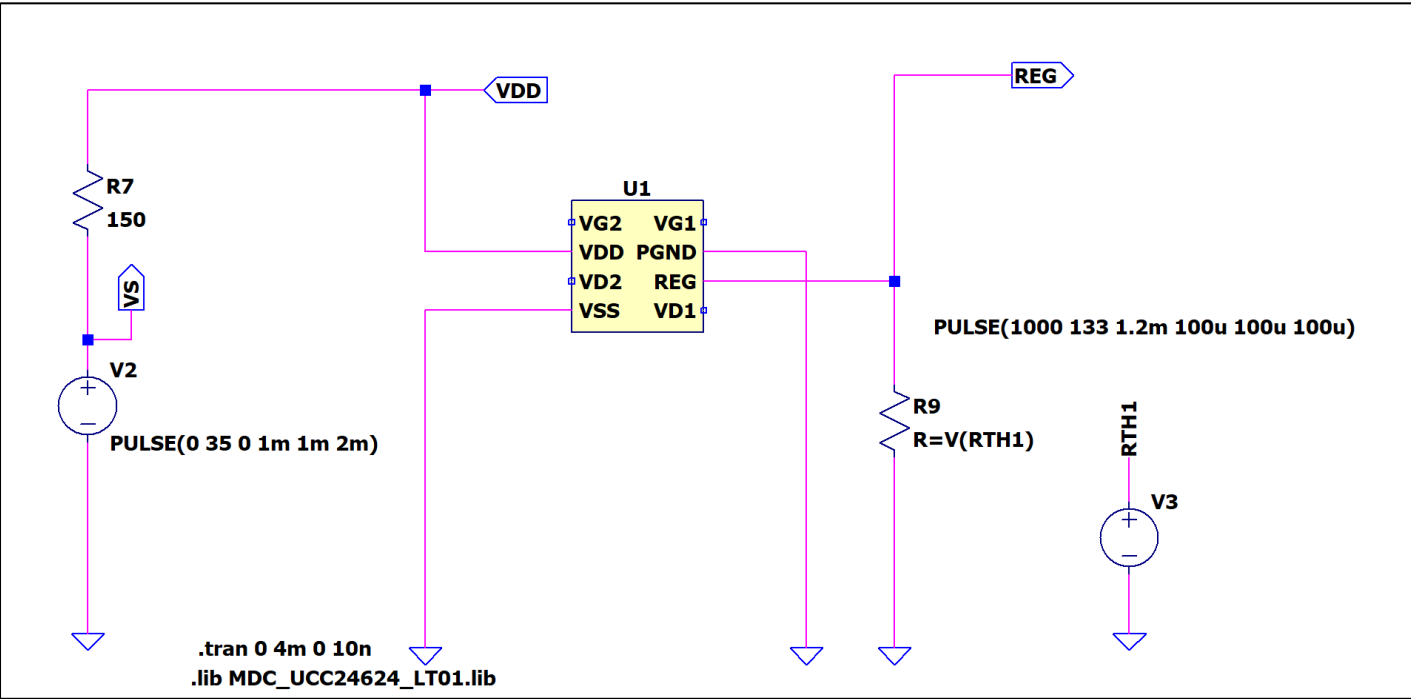
This table shows the range of evaluated simulation range that was not occurs any convergence problems in this area.

Item	Condition			Unit
	Min	Typ	Max	
VDD	4.25		26	V
Temperature		25		deg C

Model Functions Table

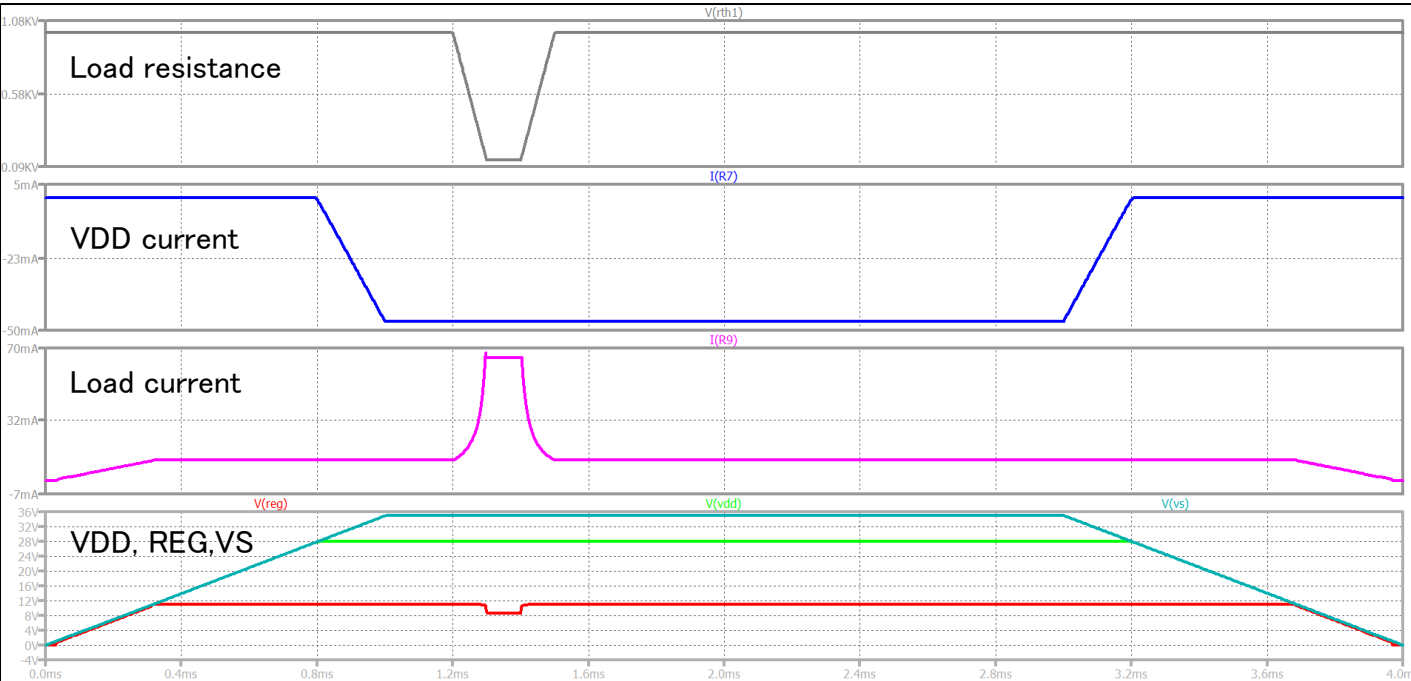
Functions	Implemented
Power Management	<input type="radio"/>
Synchronous Rectifier Control	<input type="radio"/>
Turn-off Threshold Adjustment	<input type="radio"/>
On-Time Blanking	<input type="radio"/>
Off-Time Blanking	<input type="radio"/>
SR Turn-on Re-arm	<input type="radio"/>
Two-Channel Interlock	<input type="radio"/>
Gate Voltage Clamping	<input type="radio"/>
Standby Mode	<input type="radio"/>

Testbench for Gate Voltage Clamping  
Referred to Data Sheet

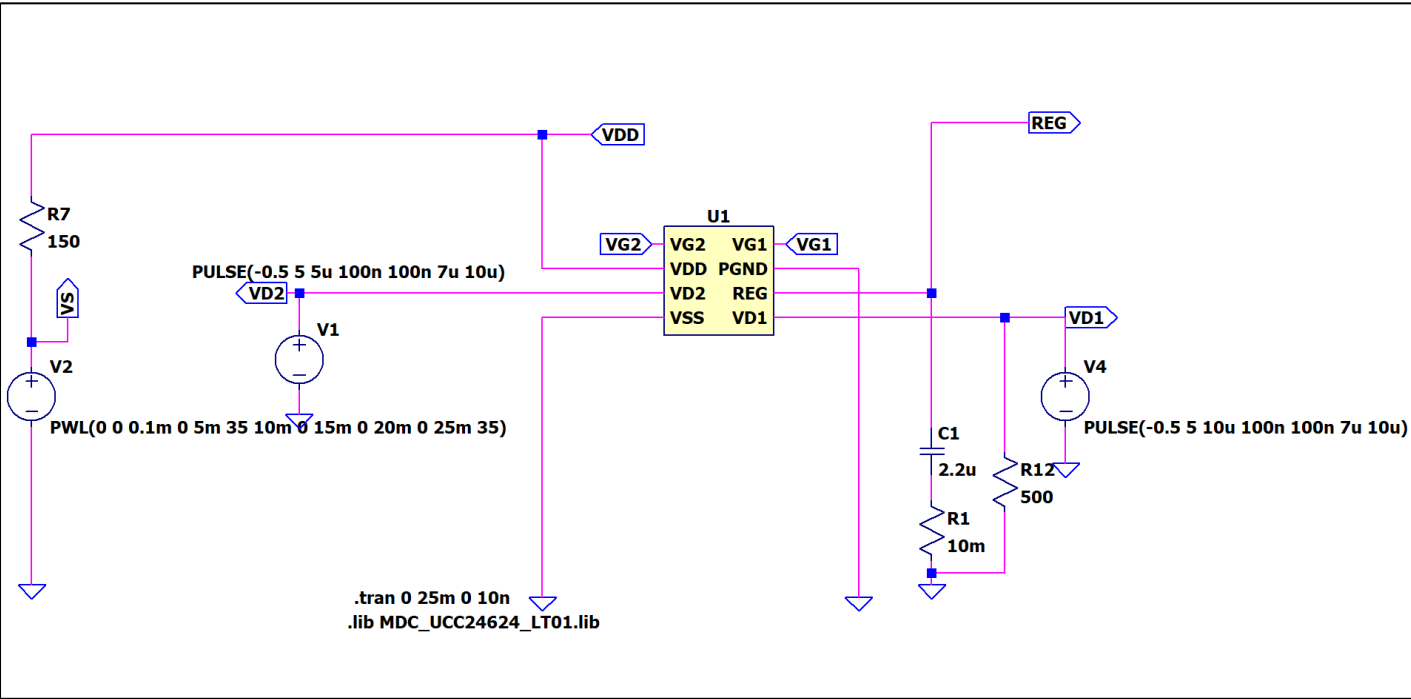


Simulation results are following.  
Explanatory notes    — : simulated

Gate Voltage Clamping



Testbench for UVLO  
Referred to Data Sheet

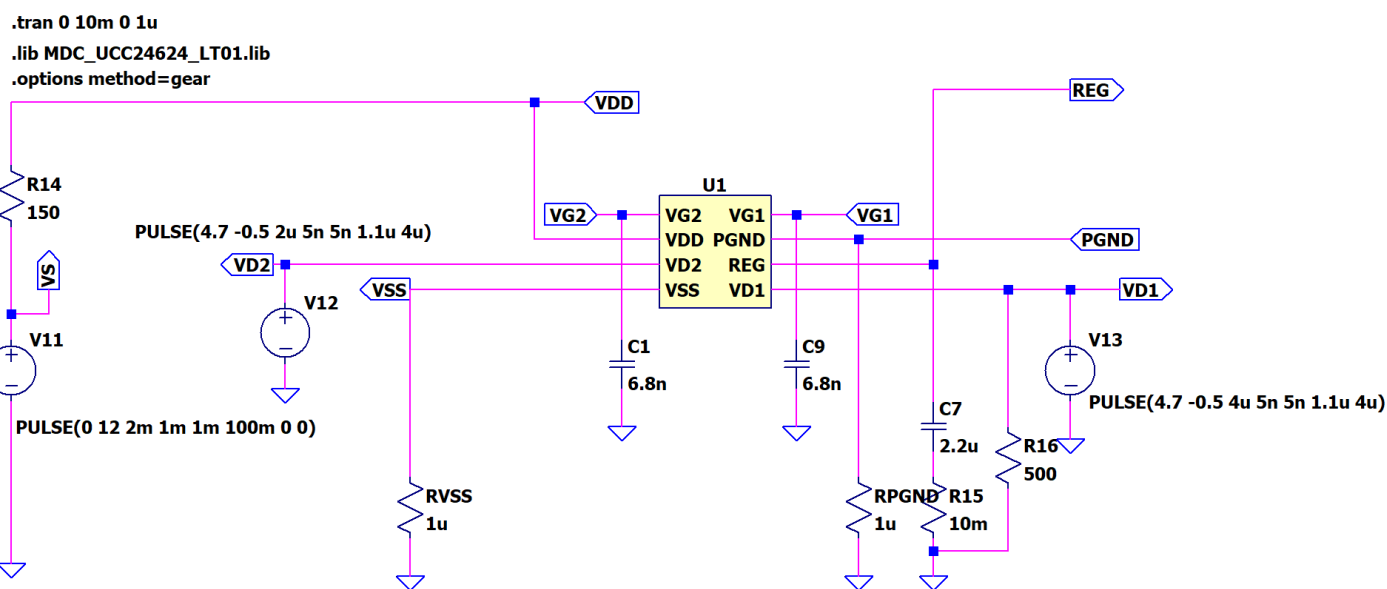


Simulation results are following.  
Explanatory notes    — : simulated

UVLO

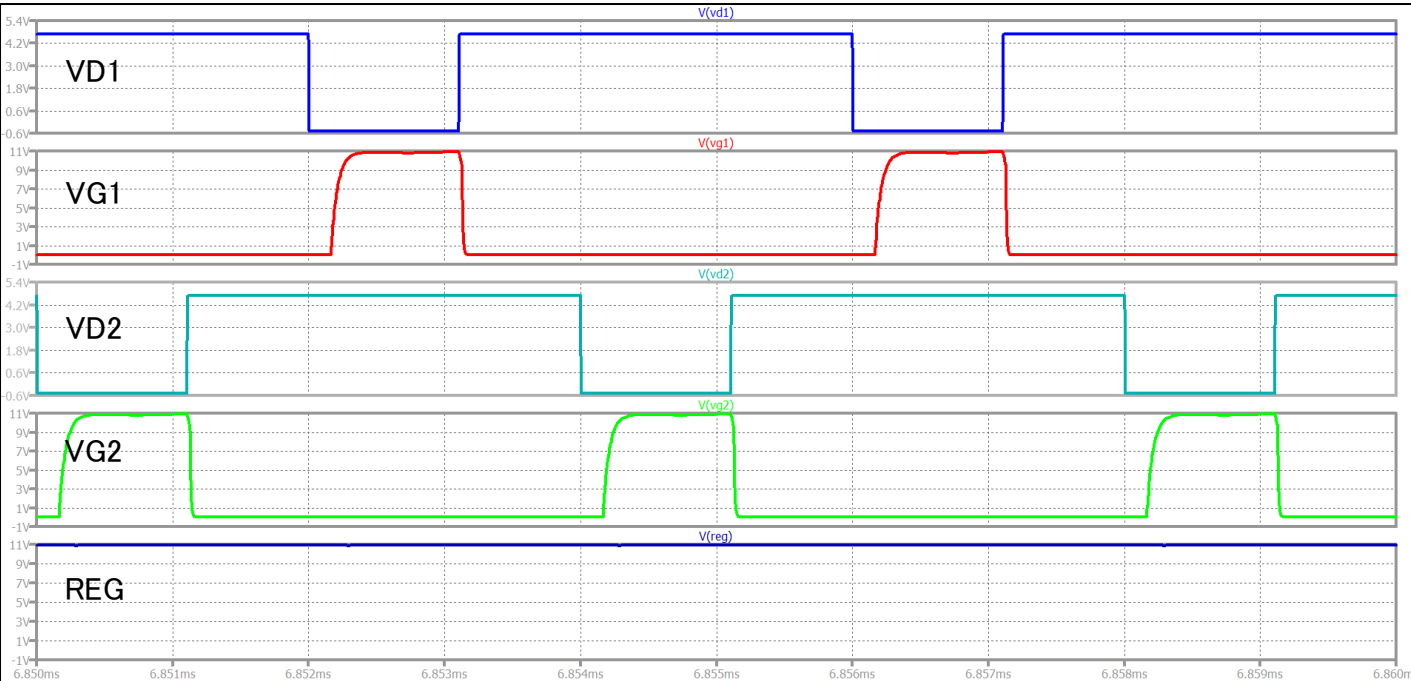


## Testbench for Two-Channel Interlock function Referred to Data Sheet

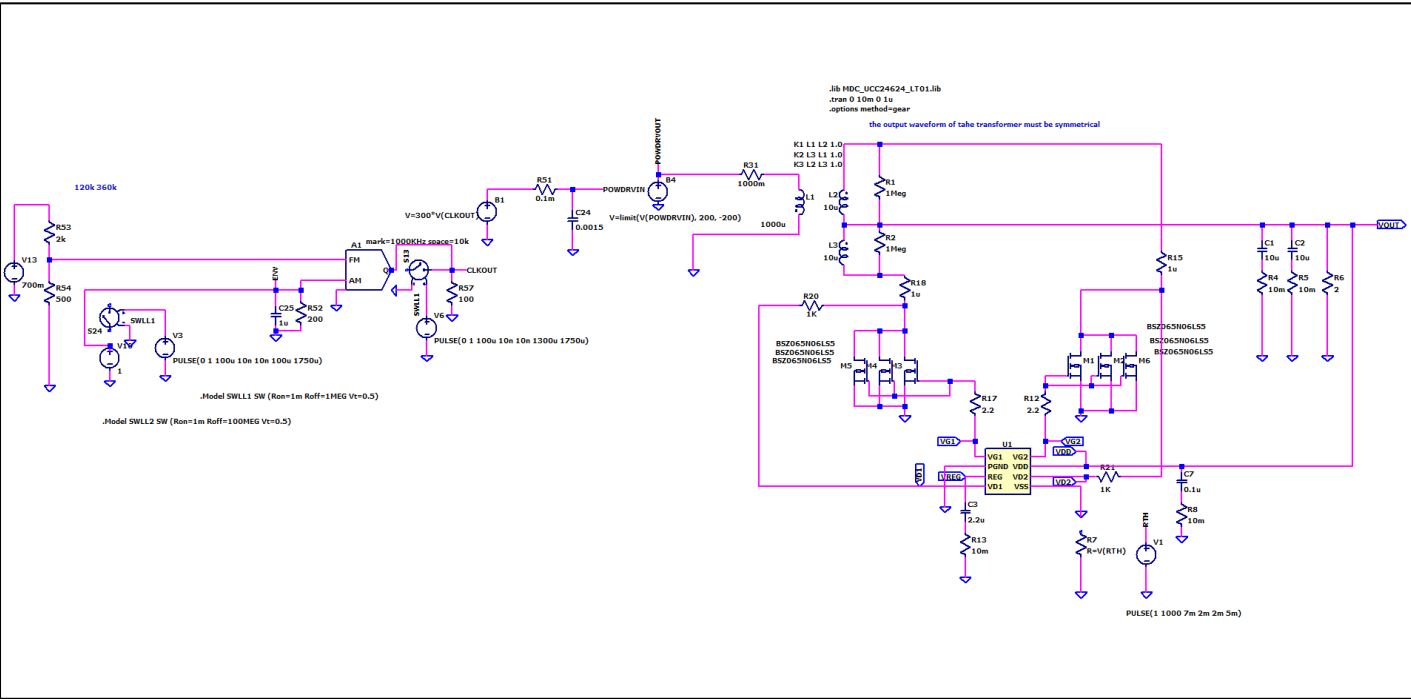


Simulation results are following.  
Explanatory notes    — : simulated

Two-Channel Interlock function



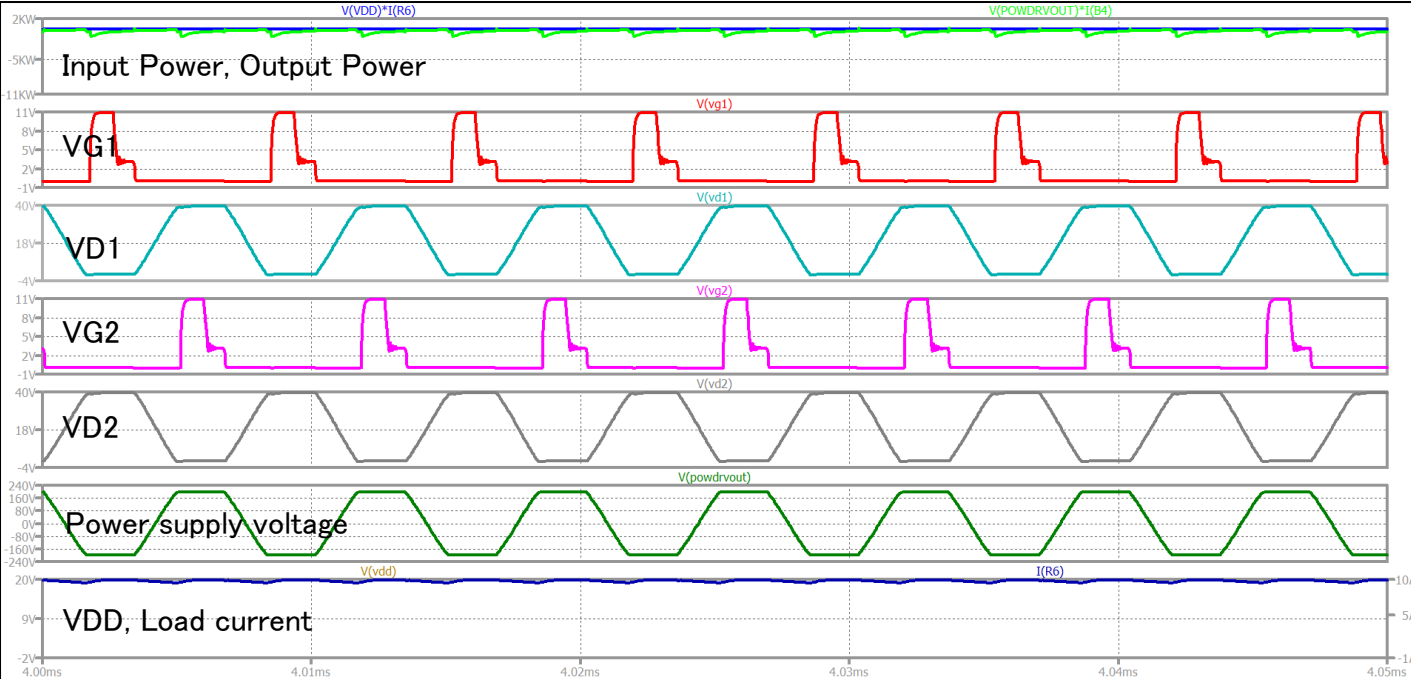
**Referred to Data Sheet**



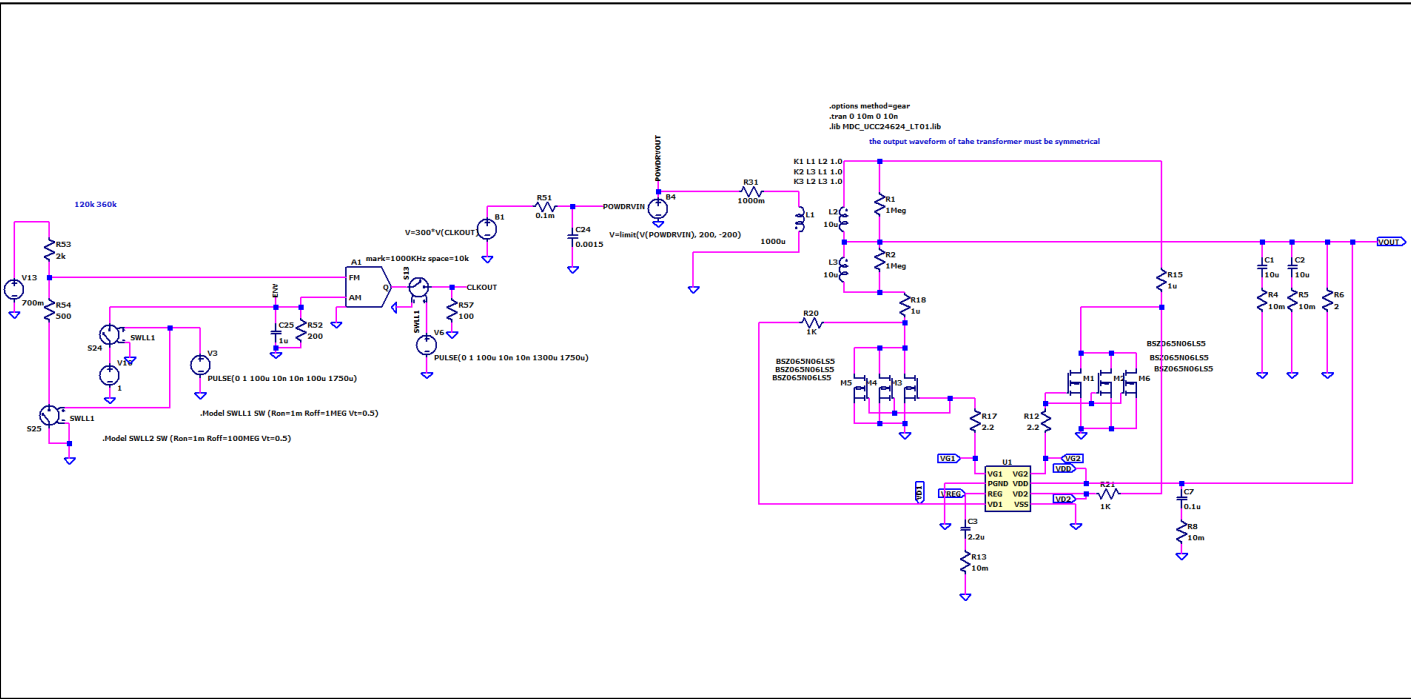
Simulation results are following.  
Explanatory notes    — : simulated

Synchronous Rectifier Control

Efficiency = 97.7% = 191.25[W]/195.73W

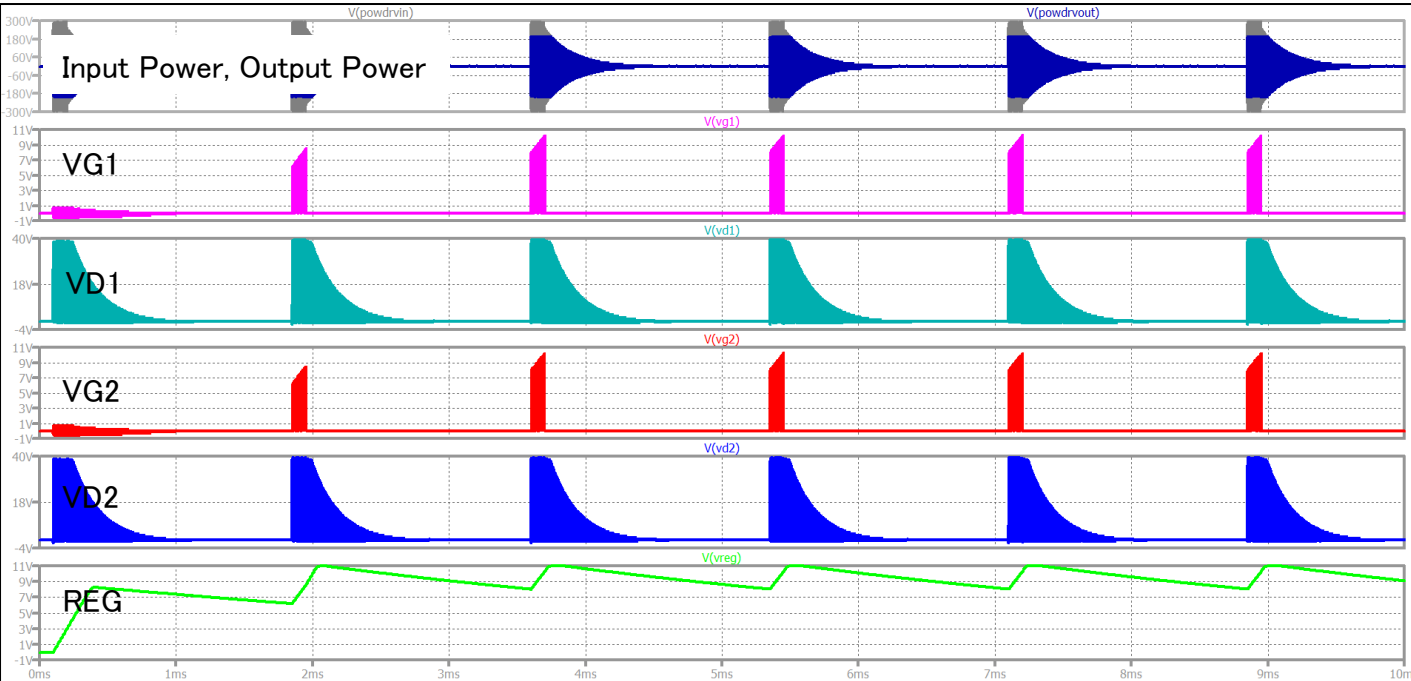


**Testbench for Burst-mode**  
**Referred to Data Sheet**



Simulation results are following.  
Explanatory notes    — : simulated

Synchronous Rectifier Control



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