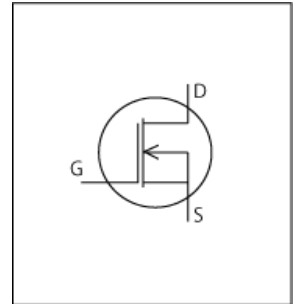


PSpice Model

NMOS

Infineon

IPC100N04S5-1R2



Model Information

Model A macro model based on BSIM3 model
Call Name MDC_IPC100N04S5-1R2_PS
Pin Assign 1:S 2:S 3:S 4:G 5:D 6:D 7:D 8:D
File List Model Library MDC_IPC100N04S5-1R2_PS01.lib
 Model Report MDC_IPC100N04S5-1R2_PS.pdf (this file)

Verified Simulator Version PSpice version 17.2
Note

References

The information which was used for modeling is as follow:

[Data Sheet]

- Date/Version 2017-08-03 Rev. 1.3
- Product name IPC100N04S5-1R2
- Company name Infineon Technologies AG
- Characteristics IdVds[Vgs],Rds(on)Id[Vgs],IdVgs[Temp],Rds(on)Temp[Id],Vt hTemp[Id],CapacitanceVds[Cname],IsVsd[Temp],BvTemp[Ir],VgsQg[Vdd],SwitchingIdd[Tname],SwitchingWaveform,Trrlf[Ir],Qrrlf[Ir],TrrQrrWaveform

Simulation Range

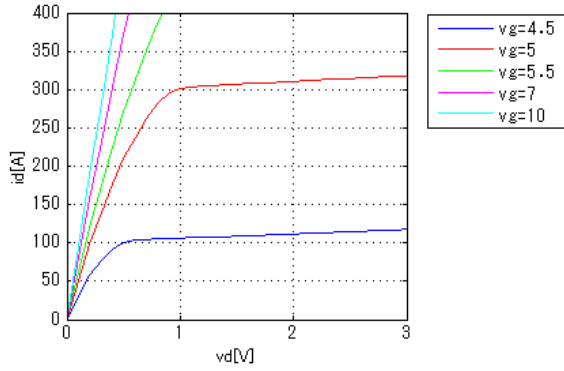
This table shows the range of evaluated simulation range that was not occurs any convergence problems in this area.

Item	Range			Unit
	Min.		Max.	
Drain-source voltage (DC)	0	to	40	V
Gate-source voltage (DC)	-20	to	20	V
Temperature	-55	to	175	deg C

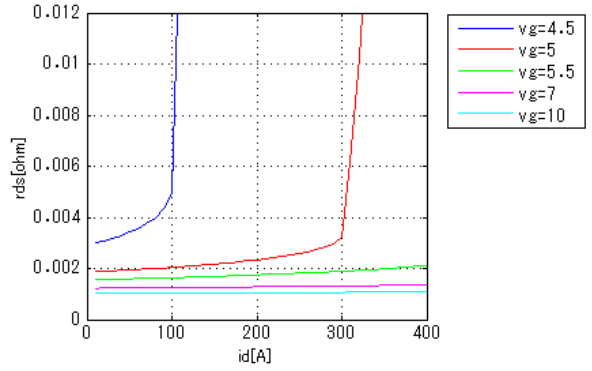
Simulation results are following.
 Explanatory notes — : simulated

IdVds[Vgs]

Temp. = 25degC

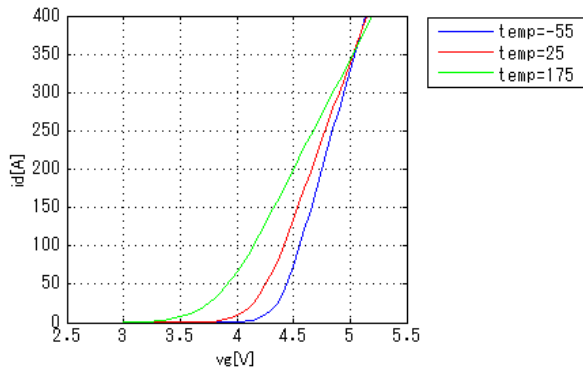


Rds(on)Id[Vgs]



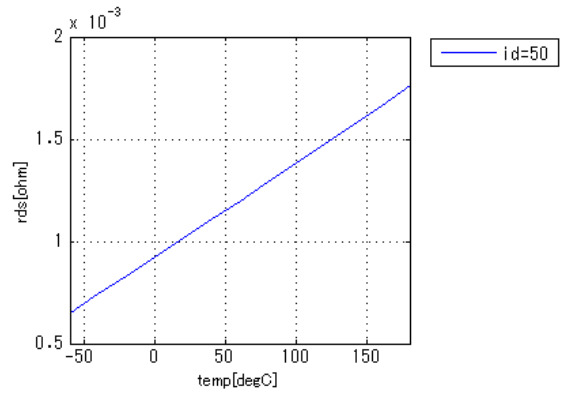
IdVgs[Temp]

Vds = 6V



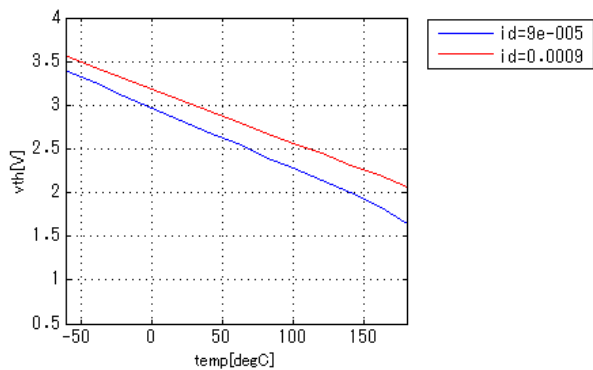
Rds(on)Temp[Id]

Vgs = 10V

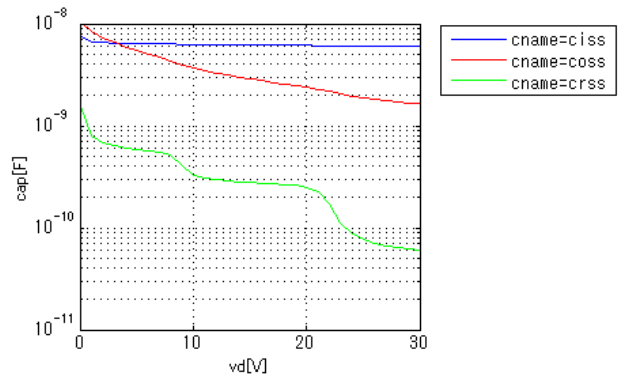


VthTemp[Id]

Vd = Vg

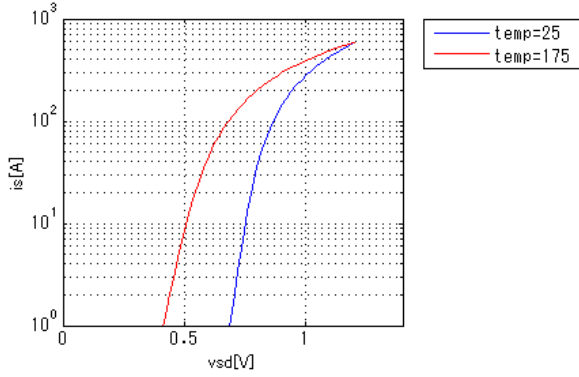


CapacitanceVds[Cname]

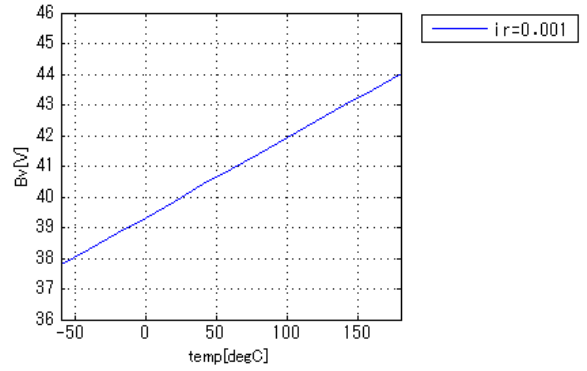


Simulation results are following.
 Explanatory notes — : simulated

IsVsd[Temp]

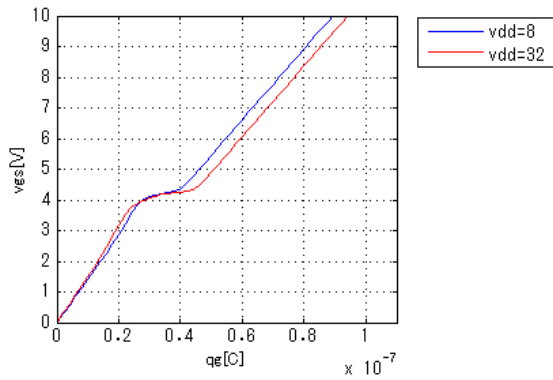


BvTemp[Ir]

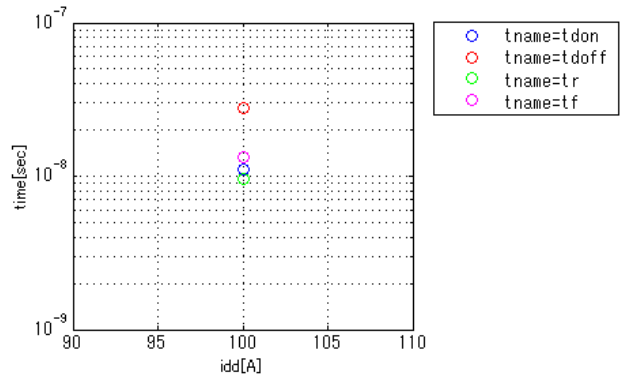


VgsQg[Vdd]

Id = 40A

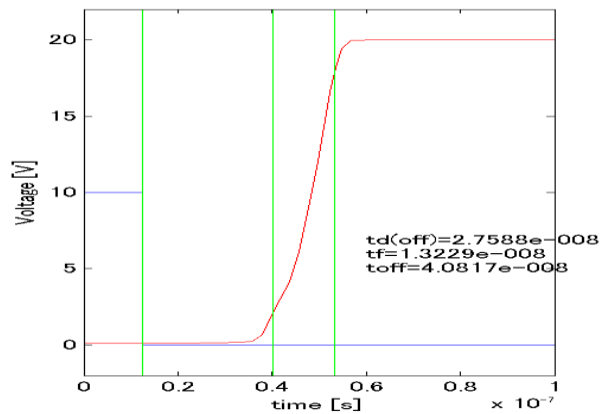
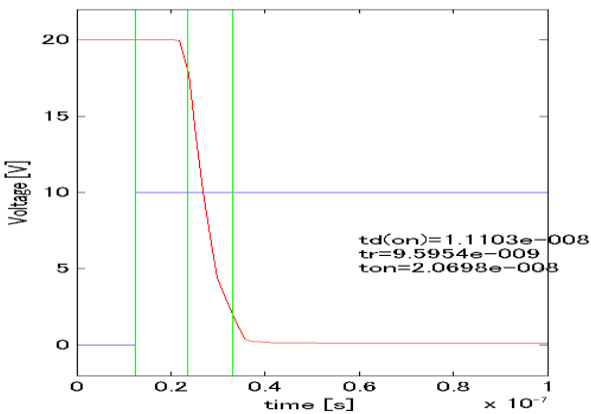


SwitchingIdd[Tname]



SwitchingWaveform

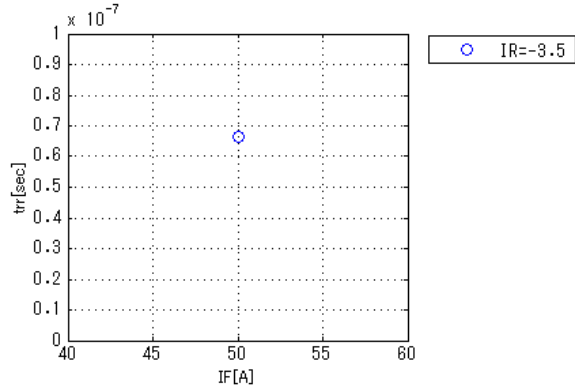
Blue : INPUT Red : OUTPUT



Simulation results are following.
 Explanatory notes — : simulated

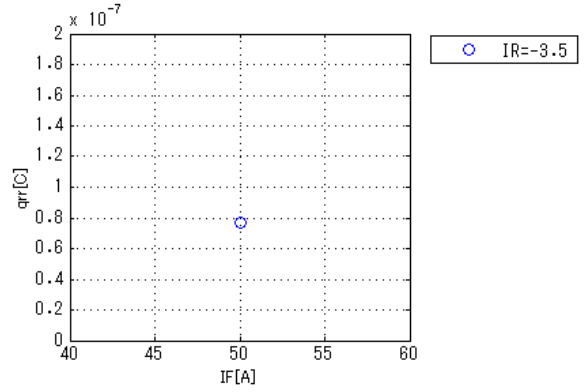
Trrlf[μ s]

didt = 100A/us



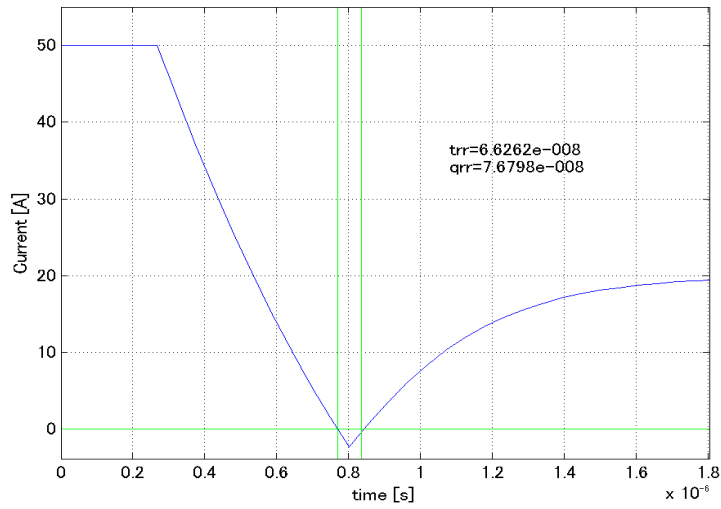
Qrrlf[μ s]

didt = 100A/us



TrrQrrWaveform

didt = 100A/us



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