Pspice Model
LDO Regulators with Watch Dog and Timer Voltage Detector
ROHM
BD4271HFP

Model Information

Model	A macro model
Call Name	MDC_BD4271HFP_PS
Pin Assign	1:VCC 2:CTL 3:RO 4:GND 5:CT 6:CLK 7:VO FIN:GND
File List	Model Library MDC_BD4271HFP_PS.lib
	Model Report MDC_BD4271HFP_PS.pdf(this file)

Verified Simulator Version Pspice

Note

References

The information which was used for modeling is as follow:

[Data Sheet]

- ●Date/Version
- ●Product name BD4271HFP
- ●Company name ROHM

[Characteristics listed]

●Characteristics

Output Voltage vs Input Voltage
Line regulation
Load regulation
When supply voltage VCC is ON ⇔ OFF
When output control voltage VCTL is ON ⇔ OFF
When WDT threshold Voltage VCLK is ON ⇔ OFF
Overcurrent Protection Characteristics

Simulation Condition

This table shows the range of evaluated simulation range that was not occurs any convergence problems in this area.

Item	Condition	Unit
Temperature	25	deg C

○ : Implemented
× : Not Implemented
— : Not applicable

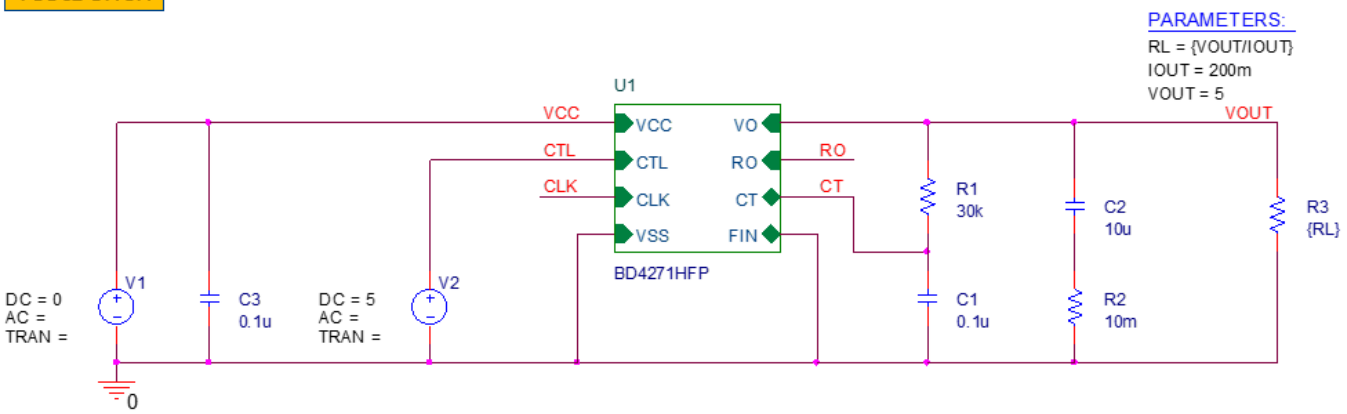
Model Functions Table

	RANK=2	
Functions	**RANK**	**Implemented**
Output Voltage vs Input Voltage	1	○
Line regulation	1	○
Load regulation	1	○
Enable Operation	1	○
Dropout Voltage	1	○
Overcurrent Protection Characteristics	1	○
WDT Reset Operation	2	○

Output Voltage vs Input Voltage (Input=0V~45V Output=5.0V IOUT=200mA)

Simulation results are following.
Explanatory notes — : simulated

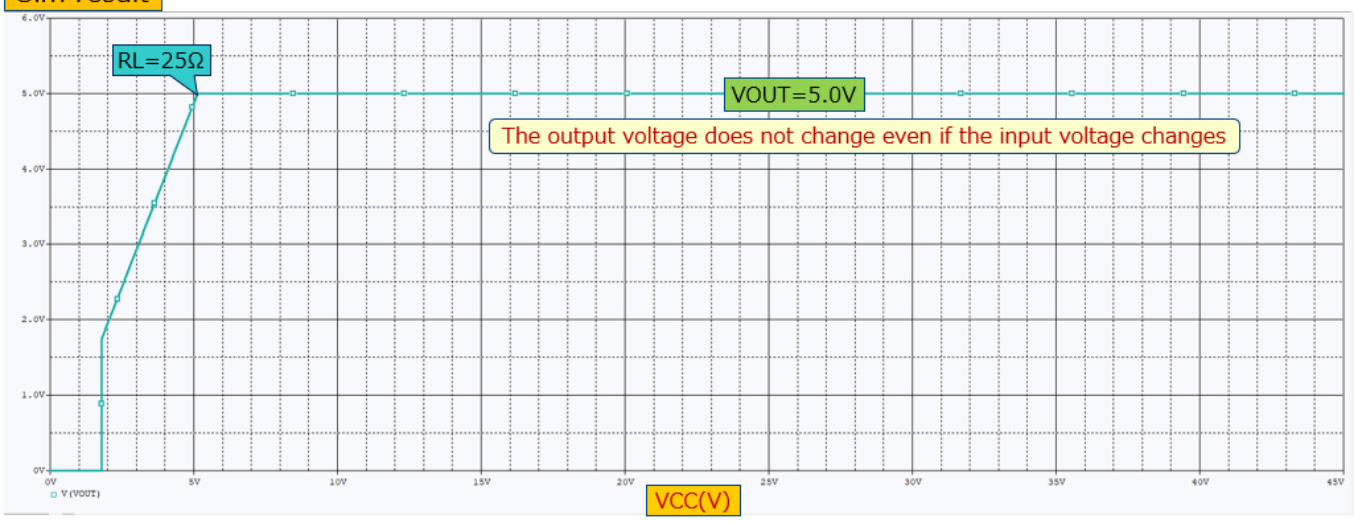
Testbench



Output Voltage vs Input Voltage (Input=0V~45V Output=5.0V IOUT=200mA)

Simulation results are following.
Explanatory notes — : simulated

Sim result

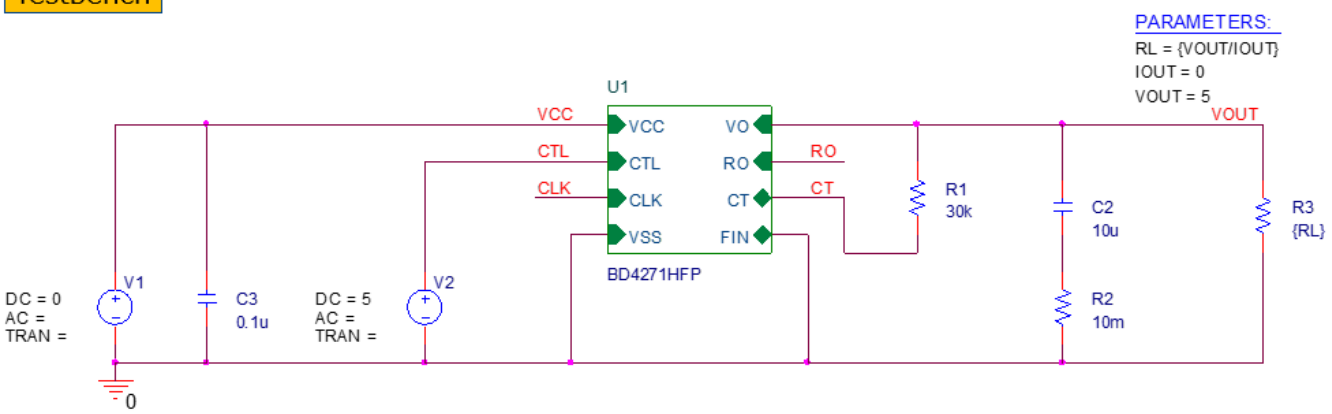


Line regulation (Input=8V~16V Output=5.0V IOUT=0A)

Simulation results are following.
Explanatory notes　— : simulated

ラインレギュレーション	Reg.I	-30	–	30	mV	8 V ≤ Vcc ≤ 16 V

Testbench



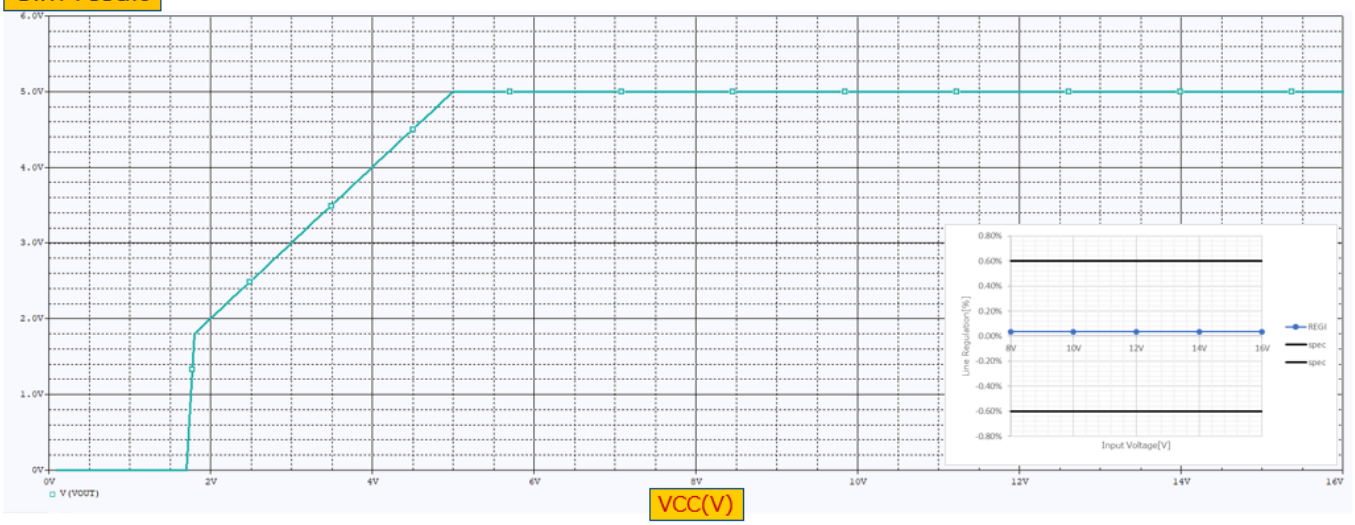
Line regulation (Input=8V~16V Output=5.0V IOUT=0A)

Simulation results are following.
Explanatory notes　— : simulated

Line regulation

VIN	VO	$R_{EG}I$
8V	5.002V	0.03%
10V	5.002V	0.03%
12V	5.002V	0.03%
14V	5.002V	0.03%
16V	5.002V	0.03%

Sim result

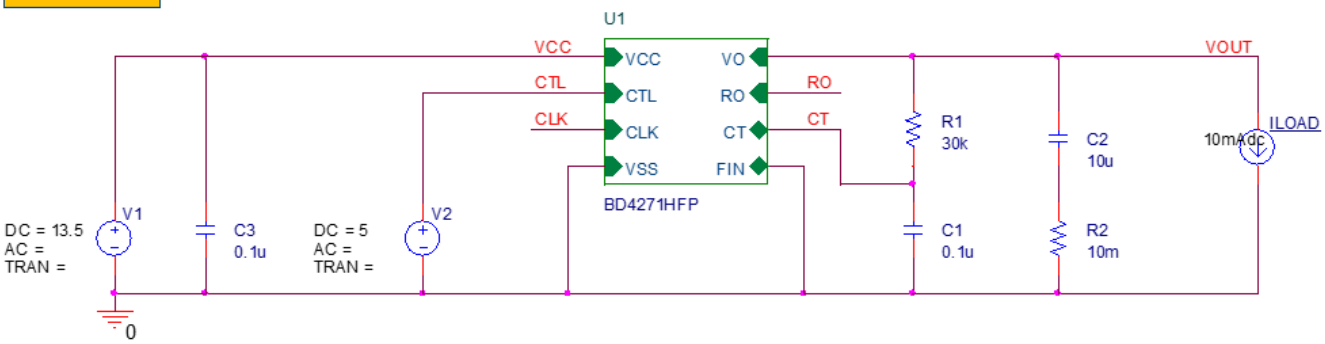


Load regulation (Input=13.5V Output=5.0V IOUT=10mA~300mA)

Simulation results are following.
Explanatory notes　— : simulated

ロードレギュレーション	Reg.L	–	10	40	mV	10 mA ≤ I_O ≤ 300 mA

Testbench



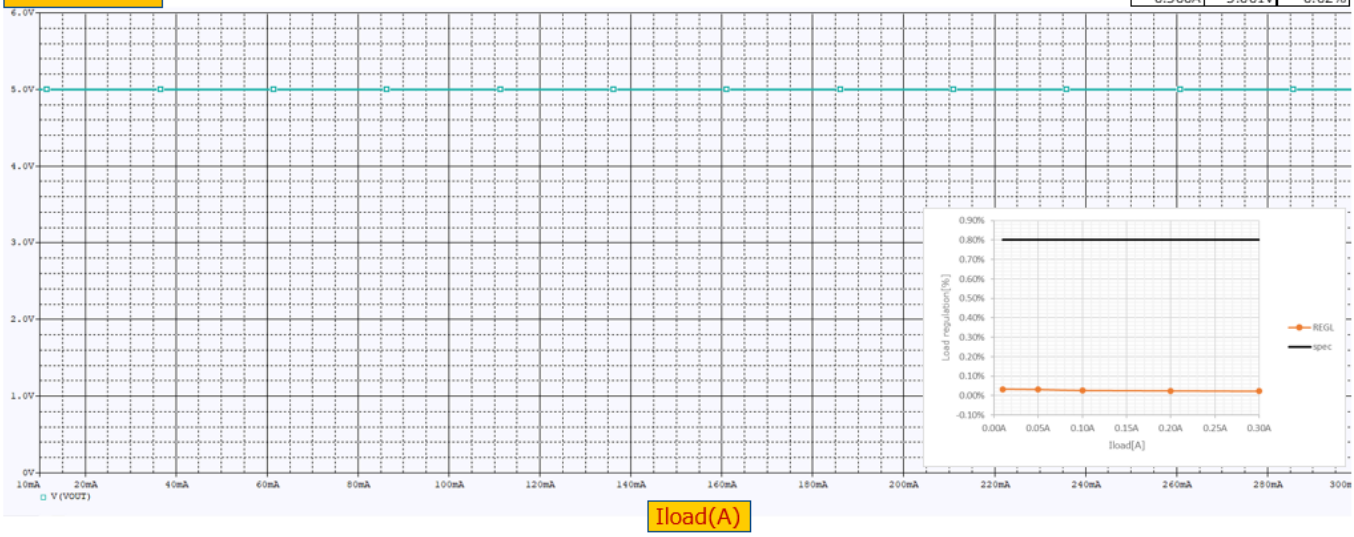
Load regulation (Input=13.5V Output=5.0V IOUT=10mA~300mA)

Simulation results are following.
Explanatory notes　— : simulated

Load regulation

Iload	VO	$R_{EG}L$
0.010A	5.001V	0.03%
0.050A	5.001V	0.03%
0.100A	5.001V	0.03%
0.200A	5.001V	0.02%
0.300A	5.001V	0.02%

Sim result

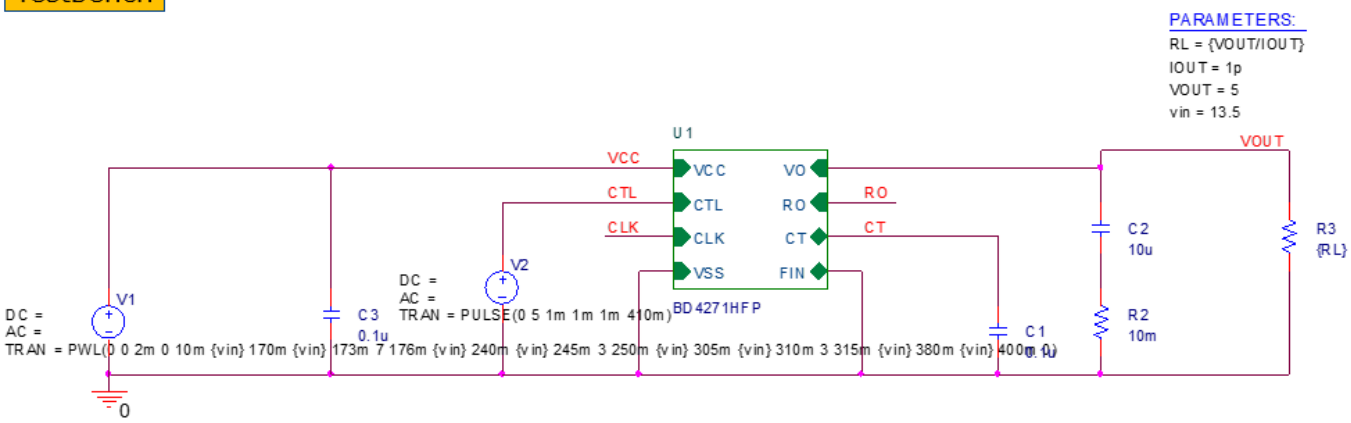


Iload(A)

When supply voltage VCC is ON ⇔ OFF (Input=13.5V Output=5.0V IOUT=1pA)

Simulation results are following.
Explanatory notes — : simulated

Testbench

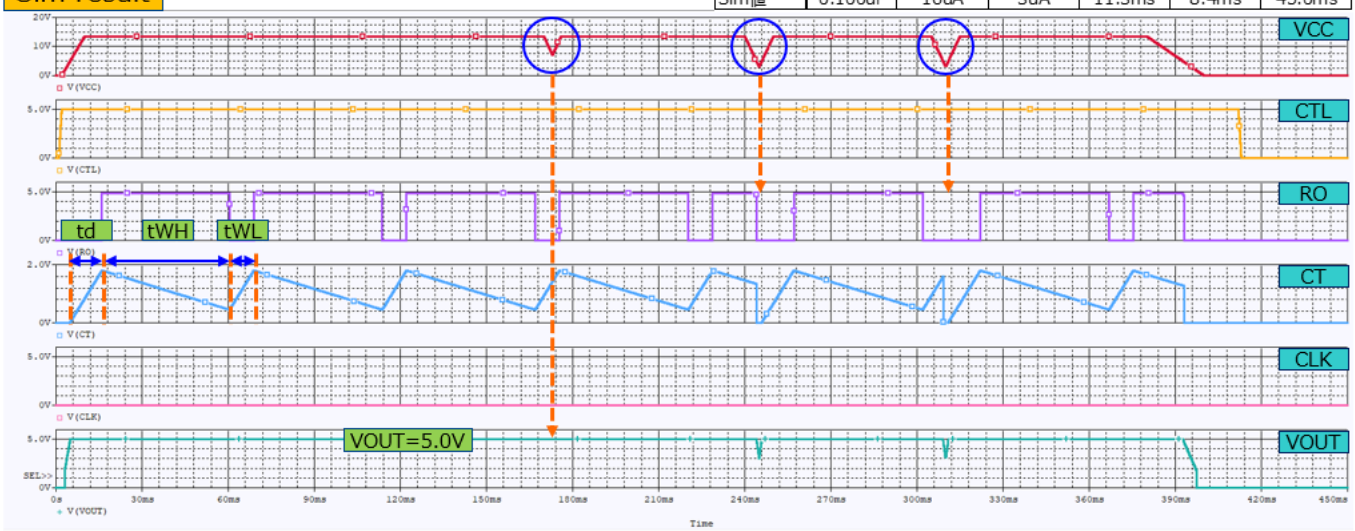


When supply voltage VCC is ON ⇔ OFF (Input=13.5V Output=5.0V IOUT=1pA)

Simulation results are following.
Explanatory notes — : simulated

Sim result

	C_{CT}	ICT_C	ICT_D	t_d	t_{WL}	t_{WH}
DS	0.100uF	16uA	3uA	11.3ms	8.4ms	45.0ms
Sim値	0.100uF	16uA	3uA	11.3ms	8.4ms	45.0ms

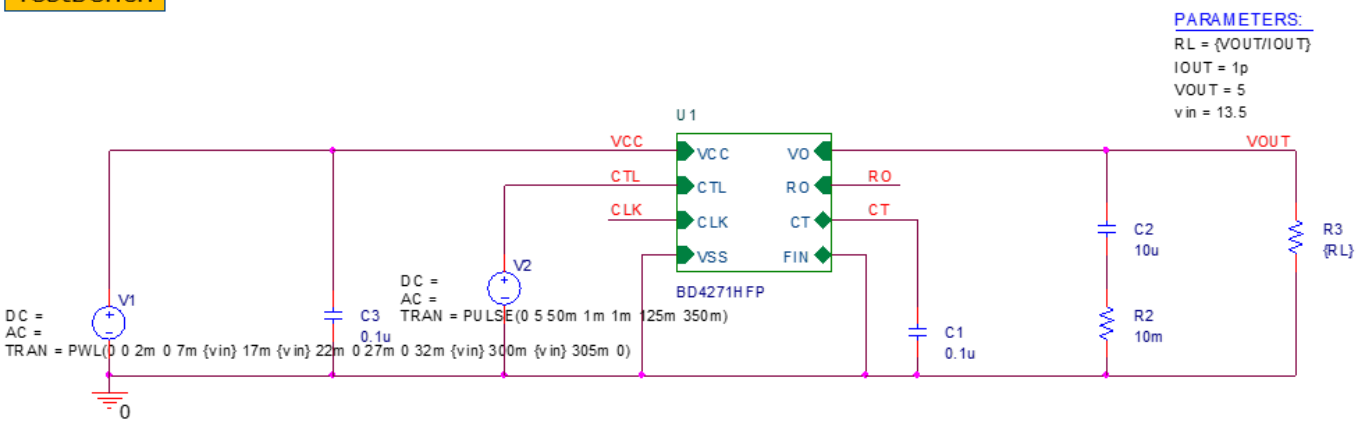


When VOUT drops below 4.65V,
the reset operation discharges the CT and negates the RO

When output control voltage VCTL is ON ⇔ OFF (Input=13.5V Output=5.0V IOUT=1pA)

Simulation results are following.
Explanatory notes — : simulated

Testbench

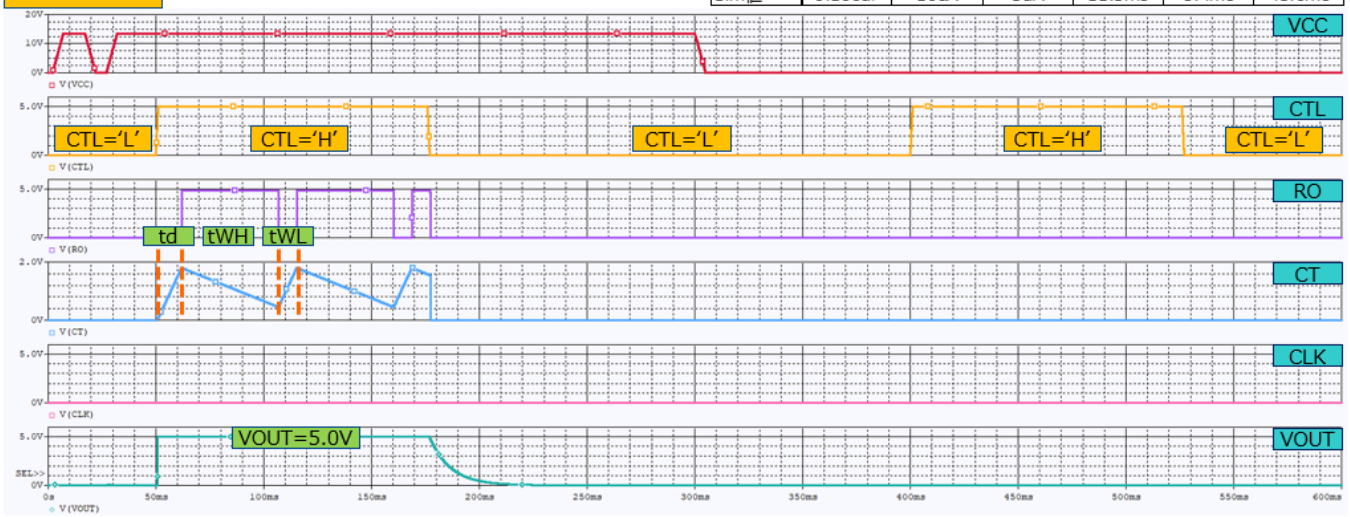


When output control voltage VCTL is ON ⇔ OFF (Input=13.5V Output=5.0V IOUT=1pA)

Simulation results are following.
Explanatory notes — : simulated

Sim result

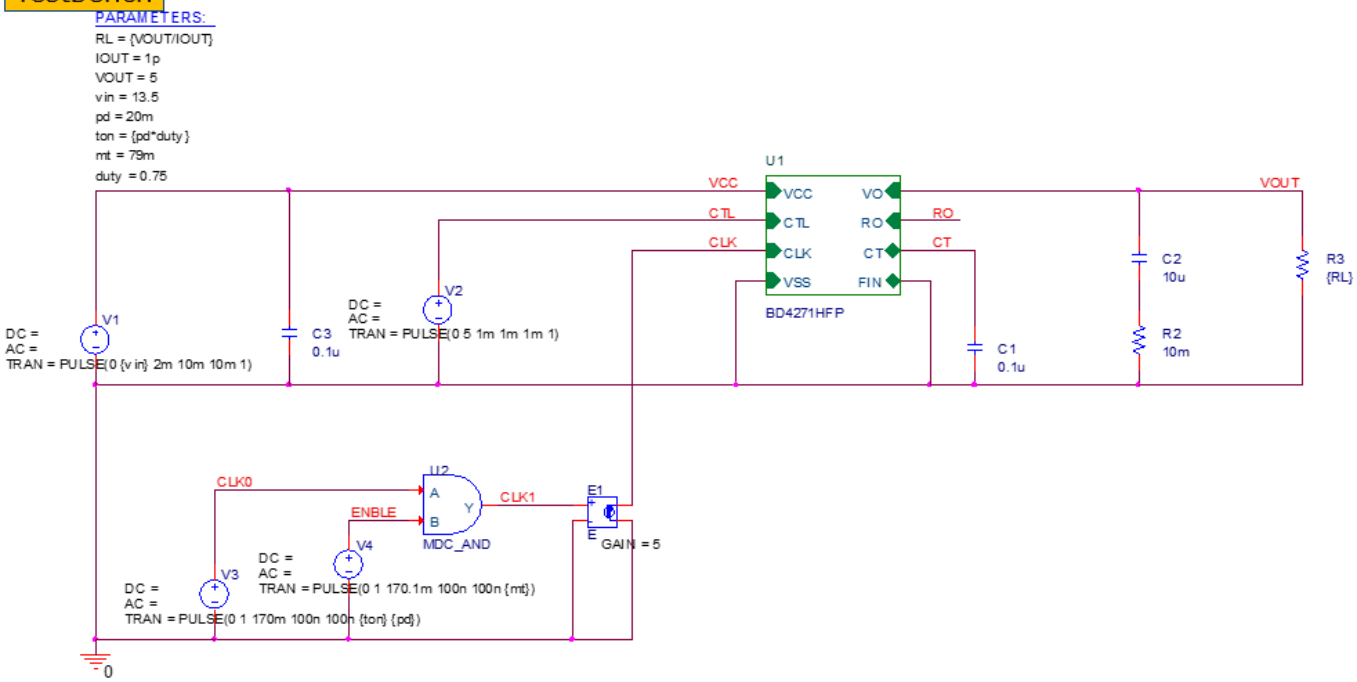
	C_{CT}	ICT_C	ICT_D	t_d	t_{WL}	t_{WH}
DS	0.100uF	16uA	3uA	11.3ms	8.4ms	45.0ms
Sim値	0.100uF	16uA	3uA	11.3ms	8.4ms	45.0ms



When WDT threshold Voltage VCLK is ON ⇔ OFF (Input=13.5V Output=5.0V IOUT=1pA)

Simulation results are following.
Explanatory notes — : simulated

Testbench

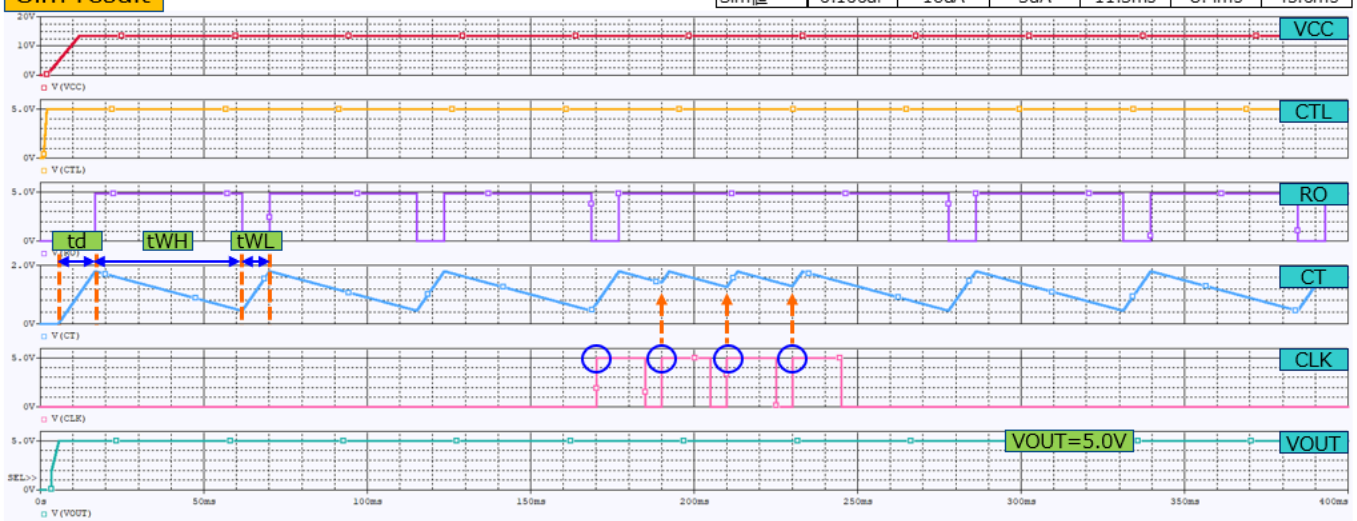


When WDT threshold Voltage VCLK is ON ⇔ OFF (Input=13.5V Output=5.0V IOUT=1pA)

Simulation results are following.
Explanatory notes — : simulated

Sim result

	C_{CT}	ICT_C	ICT_D	t_d	t_{WL}	t_{WH}
DS	0.100uF	16uA	3uA	11.3ms	8.4ms	45.0ms
Sim値	0.100uF	16uA	3uA	11.3ms	8.4ms	45.0ms



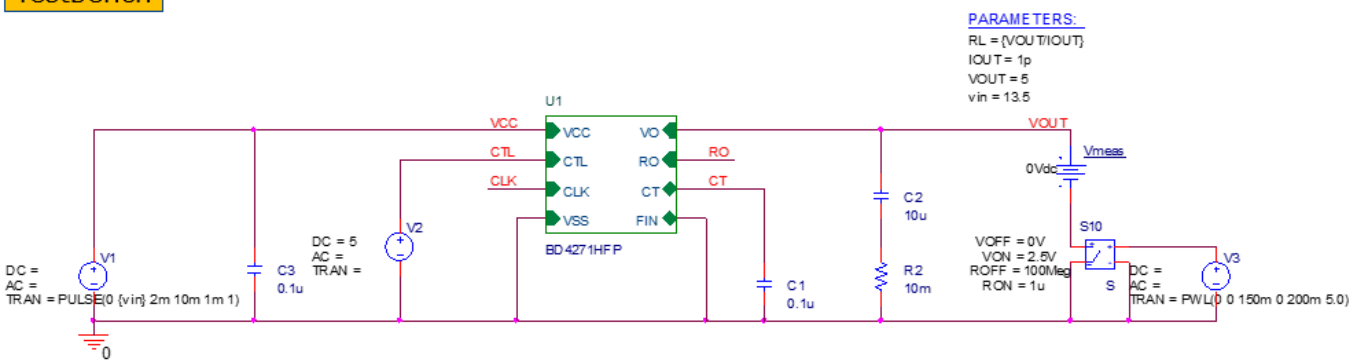
By CLK input, discharging to CT stops and charging starts and when it reaches 1.8V, discharging starts

RO is negated after CLK input is completed and CT = 0.45V is discharged

Overcurrent Protection Characteristics (Input=13.5V Output=5.0V⇒0V)

Simulation results are following.
Explanatory notes — : simulated

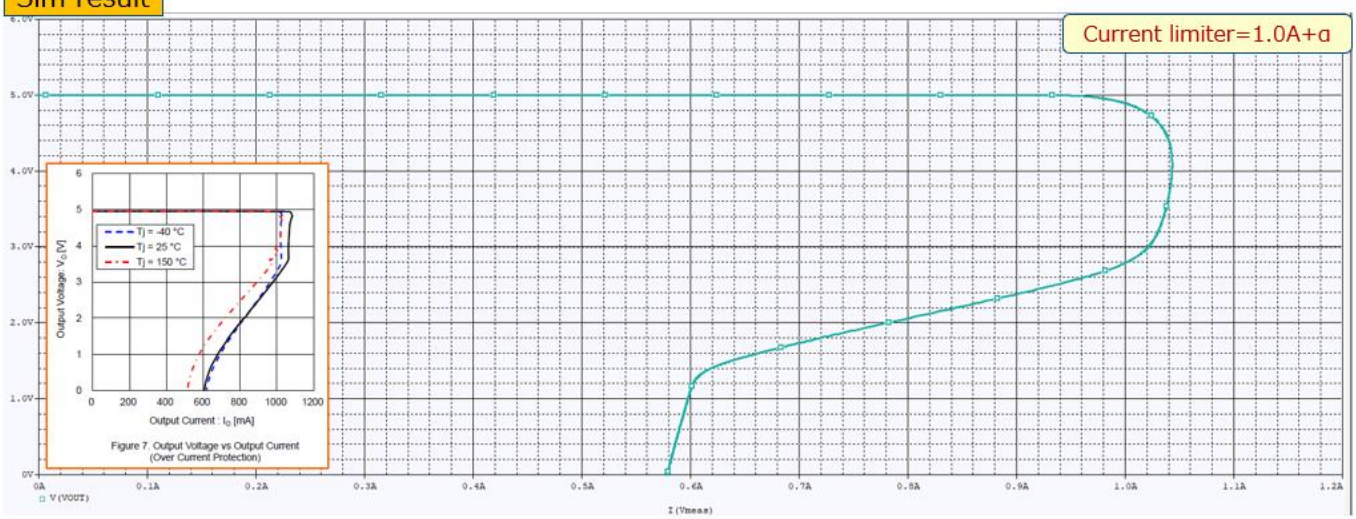
Testbench



Overcurrent Protection Characteristics (Input=13.5V Output=5.0V⇒0V)

Simulation results are following.
Explanatory notes — : simulated

Sim result



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