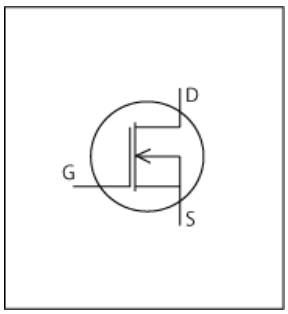
PSpice Model
NMOS
Infineon
IAUC120N04S6N009



Model Information

Model	A macro model based on BSIM3 model	
Call Name	MDC_IAUC120N04S6N009_PS	
Pin Assign	1:S 2:S 3:S 4:G 5:D 6:D 7:D 8:D	
File List	Model Library	MDC_IAUC120N04S6N009_PS01.lib
	Model Report	MDC_IAUC120N04S6N009_PS.pdf (this file)
Verified Simulator Version		PSpice version 16.6
Note		

References

The information which was used for modeling is as follow:

[Data Sheet]

- ●Date/Version 2018-09-27 Rev. 1.0
- ●Product name IAUC120N04S6N009
- ●Company name Infineon Technologies AG
- ●Characteristics IdVds[Vgs],Rds(on)Id[Vgs],IdVgs[Temp],Rds(on)Temp[Id],VthTemp[Id],Ciss,Coss,Crss,IsVsd[Temp],VgsQg[Vdd],tdon,tdoff,tf,tr,trr,qrr

Simulation Range

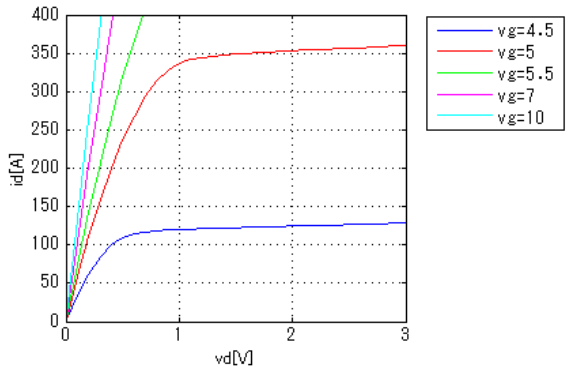
This table shows the range of evaluated simulation range that was not occurs any convergence problems in this area.

Item	Range			Unit
	Min.		Max.	
Drain-source voltage (DC)	0	to	40	V
Gate-source voltage (DC)	0	to	20	V
Temperature	-55	to	175	deg C

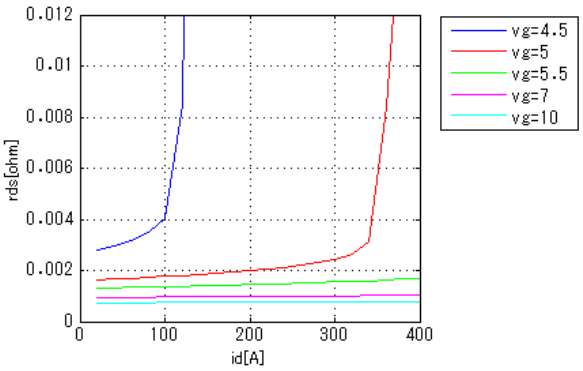
Simulation results are following.
Explanatory notes — : simulated

IdVds[Vgs]

Temp. = 25deg C

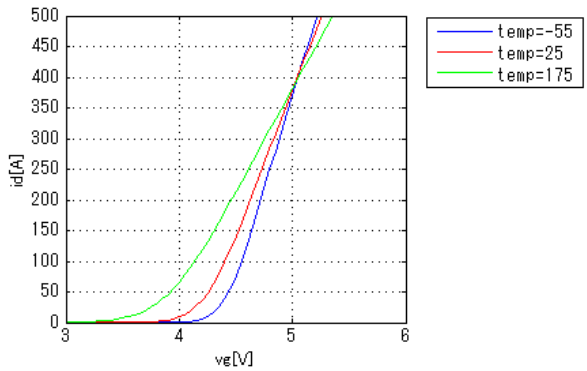


Rds(on)Id[Vgs]



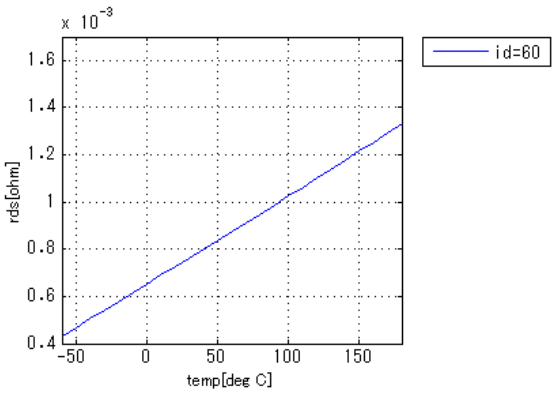
IdVgs[Temp]

Vds = 6V



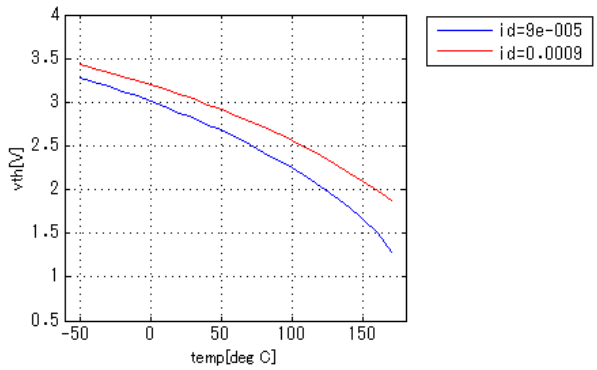
Rds(on)Temp[Id]

Vgs = 10V



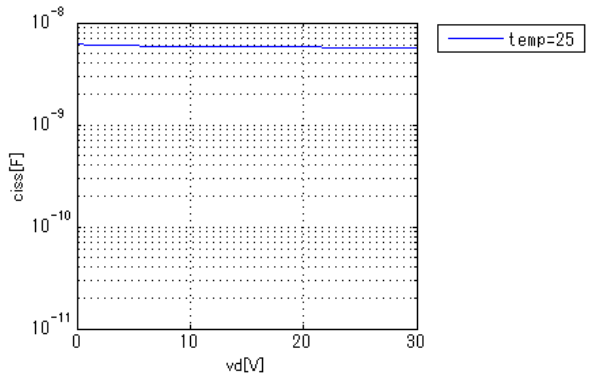
VthTemp[Id]

Vd = Vg



Ciss

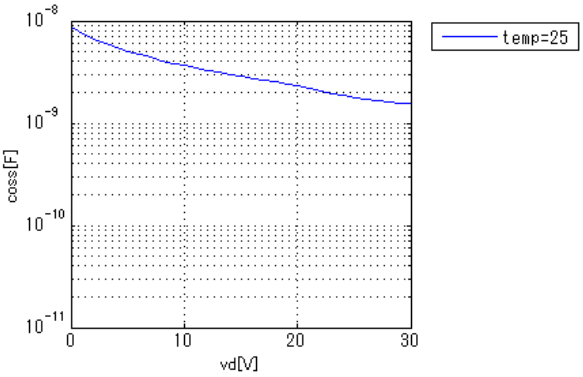
Freq. = 1MHz



Simulation results are following.
Explanatory notes — : simulated

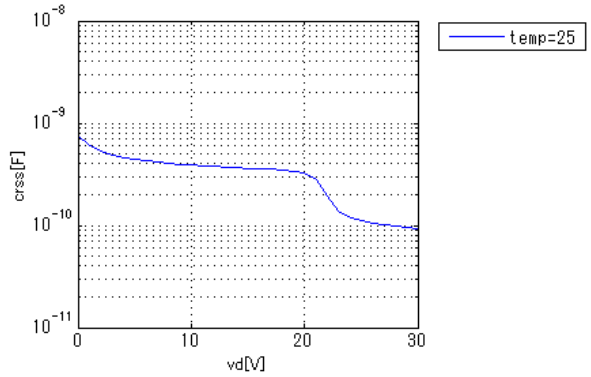
Coss

Freq. = 1MHz

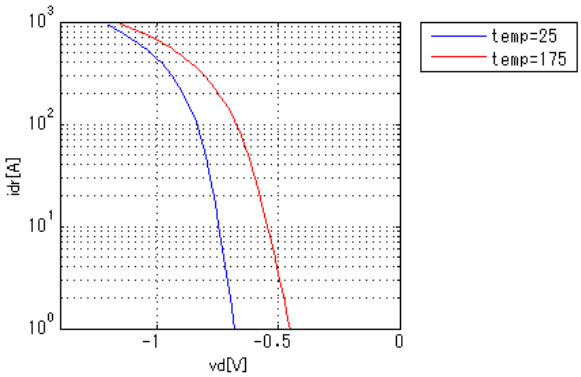


Crss

Freq. = 1MHz

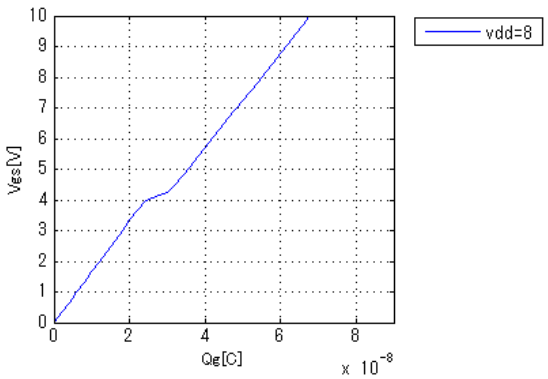


IsVsd[Temp]



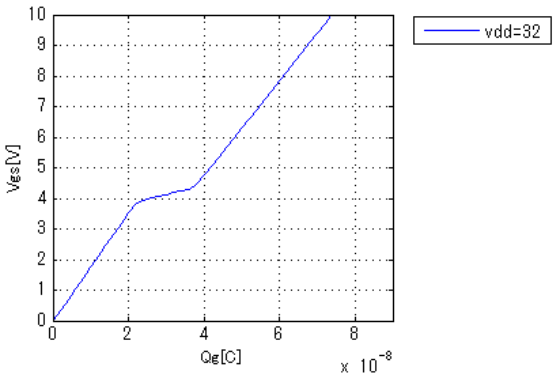
VgsQg[Vdd]

Id = 40A



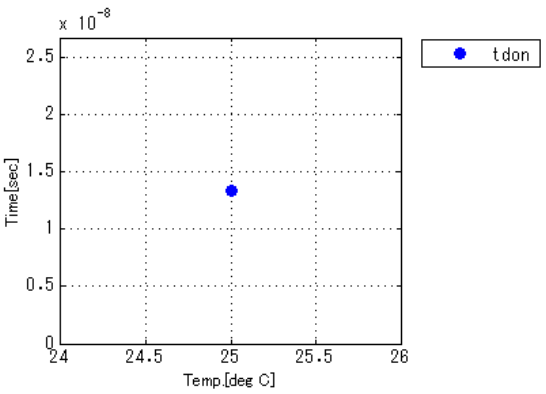
VgsQg[Vdd]

Id = 40A



tdon

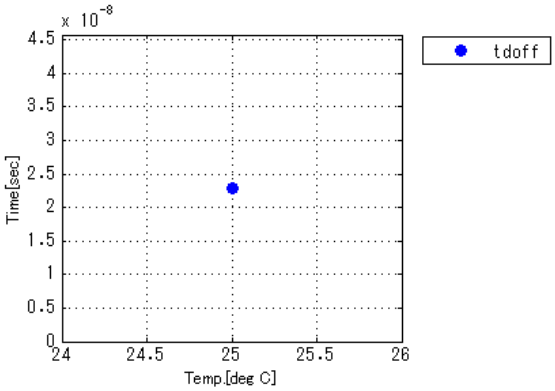
Vdd = 20V, Id = 120A, +Vg = 10V, -Vg = 0V, Rg = 3.5ohm



Simulation results are following.
Explanatory notes — : simulated

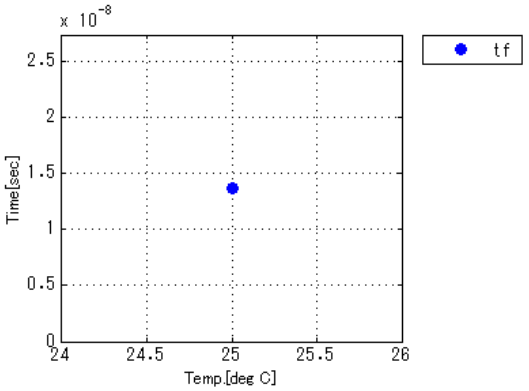
tdoff

Vdd = 20V, Id = 120A, +Vg = 10V, -Vg = 0V, Rg = 3.5ohm



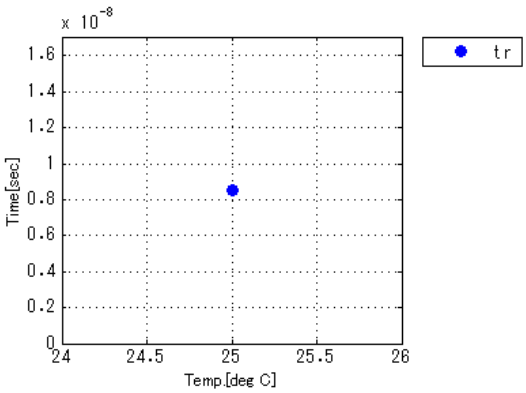
tf

Vdd = 20V, Id = 120A, +Vg = 10V, -Vg = 0V, Rg = 3.5ohm



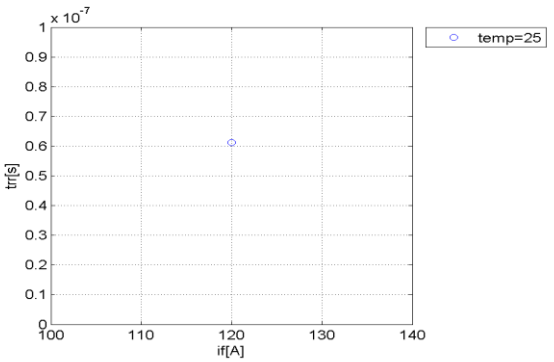
tr

Vdd = 20V, Id = 120A, +Vg = 10V, -Vg = 0V, Rg = 3.5ohm



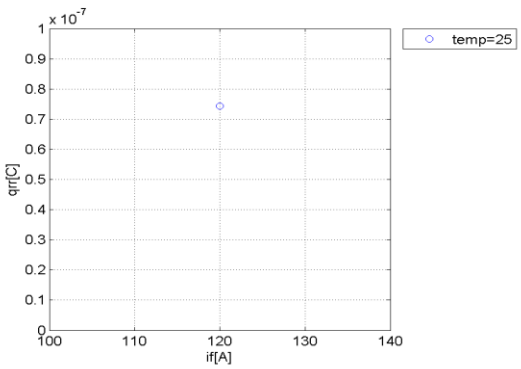
trr

ir=2.43A



qrr

ir=2.43A



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