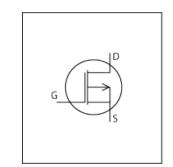


LTspice Model PMOS TOREX XP162A12A6PR-G



Model Information

Model A macro model based on BSIM3 model

Call Name MDC XP162A12A6PR-G LT

Pin Assign 1:G 2:D 3:S

File List Model Library MDC_XP162A12A6PR-G_LT02.lib

Model Report MDC_XP162A12A6PR-G_LT.pdf (this file)

Verified Simulator Version

Note

LTspice version XVII

References

The information which was used for modeling is as follow:

[Data Sheet]

Date/VersionProduct nameJTR1126-003aXP162A12A6PR-G

Company name TOREX SEMICONDUCTOR LTD.

● Characteristics IdVds[Vgs],IdVgs[Temp],Rds(on)Vgs[Id],Rds(on)Id[Vgs],Rds

(on)Temp[Vgs],Rds(on)Temp[Vgs]2,CapacitanceVds[Cname],SwitchingIdd[Tname],VgsQg[Vdd],IsVsd[Vgs],YfsId[Temp],I

dVgs[Temp]2,SwitchingWaveform

Simulation Range

This table shows the range of evaluated simulation range that was not occurs any convergence problems in this area.

Item	Range			Unit
	Min.		Max.	
Drain-source voltage (DC)	0	to	-20	V
Gate-source voltage (DC)	12	to	-12	V
Temperature	-55	to	150	deg C



Model Functions Table

MOSFET

O: Implemented

× : Not Implemented

—: Not applicable

RANK=1

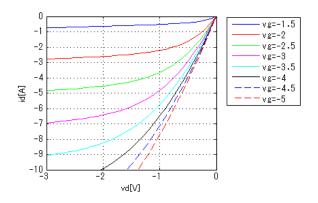
KANK-1	
RANK	Implemented
1	0
1	0
1	0
1	_
1	0
1	_
1	0
1	_
1	0
1	0
1	0
1	_
1	0
1	_
1	0
	RANK 1 1 1 1 1 1 1 1 1 1 1 1 1



Simulation results are following. Explanatory notes — : simulated

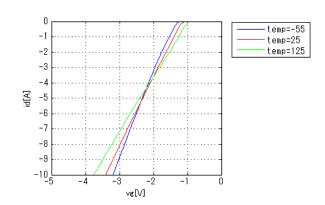
IdVds[Vgs]

Temp. = 25degC

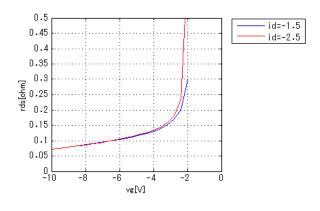


IdVgs[Temp]

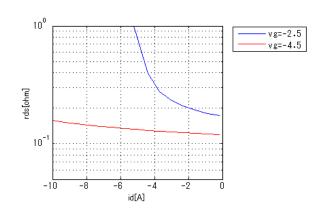
Vds = -10V



Rds(on)Vgs[ld]

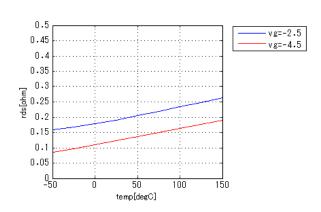


Rds(on)Id[Vgs]



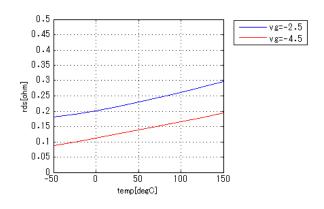
Rds(on)Temp[Vgs]

Id = -1.5A



Rds(on)Temp[Vgs]2

Id = -2.5A

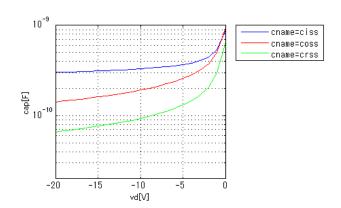




Simulation results are following. Explanatory notes — : simulated

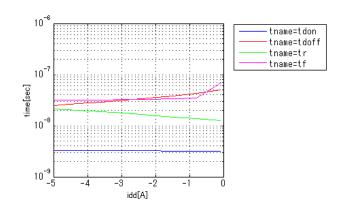
CapacitanceVds[Cname]

freq = 1000000Hz



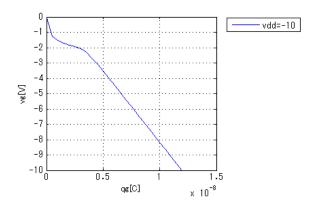
SwitchingIdd[Tname]

vgg = -5V, vdd = -10V, RGG = 50hm

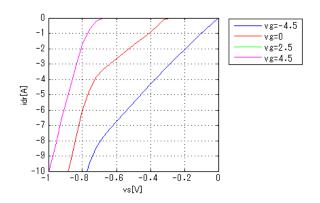


VgsQg[Vdd]

Id. = A

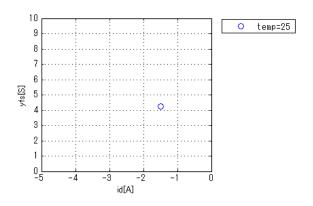


IsVsd[Vgs]



YfsId[Temp]

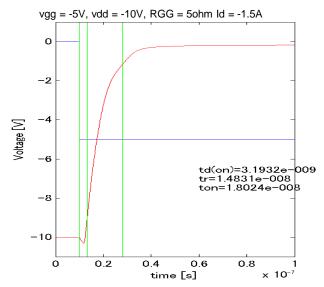
Vds = -10V

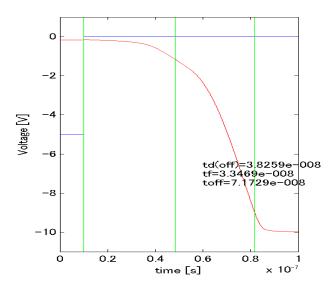




Simulation results are following. Explanatory notes — : simulated

Switching Waveform







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