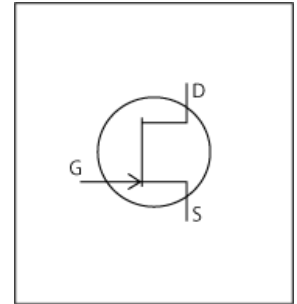
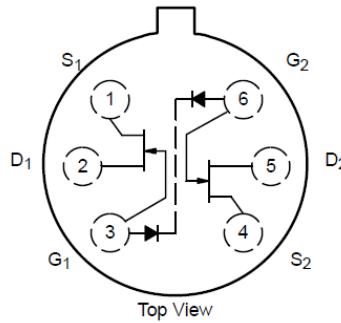


LTspice Model N-Channel JFET VISHAY POLYTECH 2N3958



Model Information

Model A macro model based on general SPICE jfet model
Call Name MDC_2N3958_LT
Pin Assign 1:S1 2:D1 3:G1 4:S2 5:D2 6:G2
File List Model Library MDC_2N3958_LT01.lib
 Model Report MDC_2N3958_LT.pdf (this file)

Verified Simulator Version LTspice version XVII
Note

References

The information which was used for modeling is as follow:

[Data Sheet]

- Date/Version Rev. B, 04-Jun-01
- Product name 2N3958
- Company name Vishay Polytech Co., Ltd.
- Characteristics $I_d V_{ds}[V_{gs}], I_d V_{gs}[Temp], R_{ds(on)} I_d[V_{gs}], C_{iss} V_{gs}[V_{ds}], Y_{fs} I_d[Temp], I_g V_{dg}[I_d], I_g V_{dg}[I_d]^2, E_n Freq[V_{gs}], Y_{os} I_d[Temp]$

Simulation Range

This table shows the range of evaluated simulation range that was not occurs any convergence problems in this area.

Item	Range			Unit
	Min.		Max.	
Gate-drain voltage (DC)	-50	to	0	V
Gate-source voltage (DC)	-50	to	0	V
Temperature	-55	to	150	deg C

JFET

○ : Implemented
 × : Not Implemented
 — : Not applicable

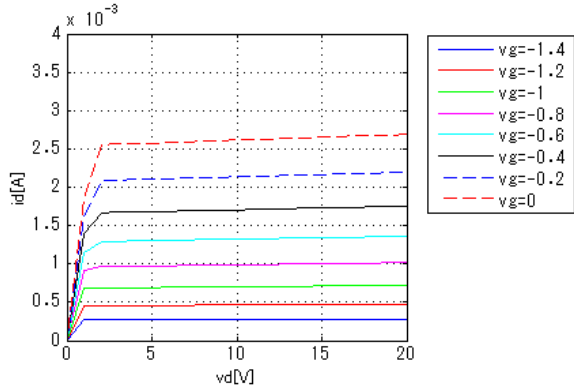
Model Functions Table
RANK=1

Functions	RANK	Implemented
ID-VDS-VGS	1	○
ID-VGS-TEMP	1	○
yfs-ID	1	○
Yos-ID	1	○
RDS(on)-ID	1	○
Capacitance	1	○
IG-VDG	1	○

Simulation results are following.
 Explanatory notes — : simulated

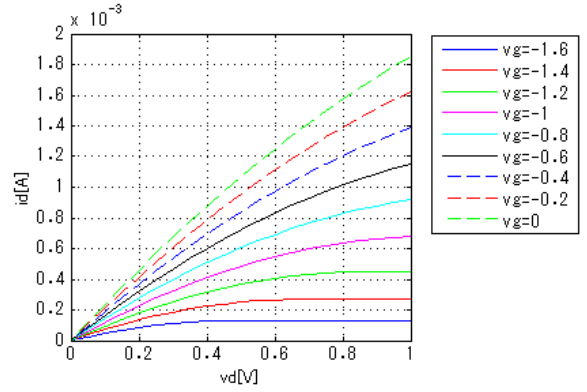
IdVds[Vgs]

Temp. = 25deg C



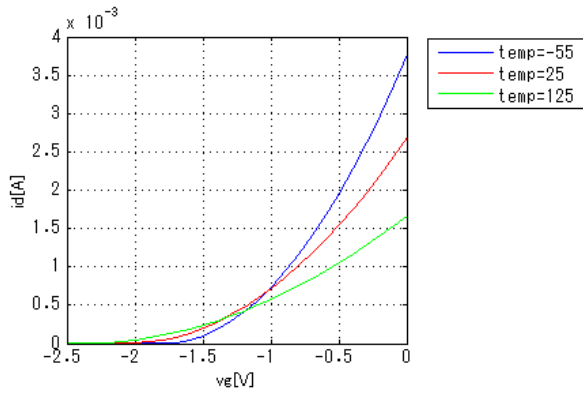
IdVds[Vgs]

Temp. = 25deg C

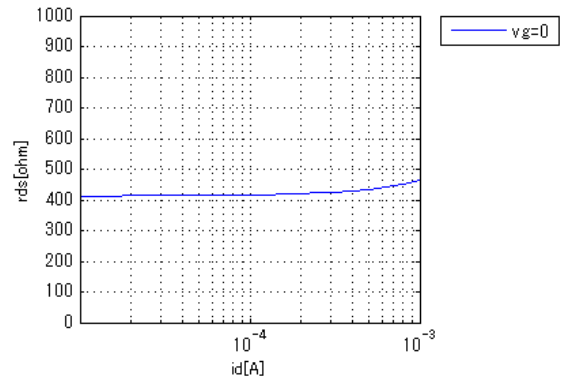


IdVgs[Temp]

Vds = 20V

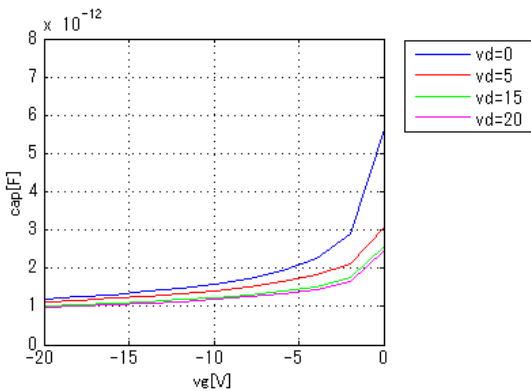


Rds(on)Id[Vgs]



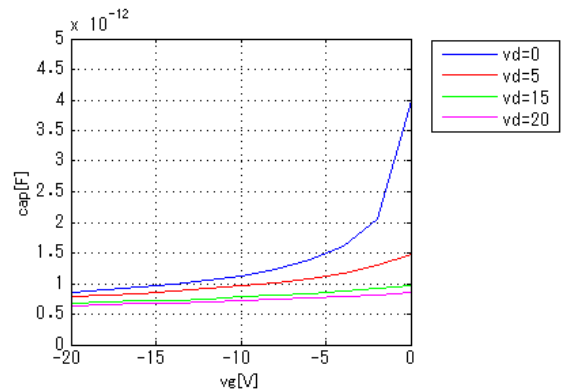
CissVgs[Vds]

freq = 1000000Hz



CissVgs[Vds]

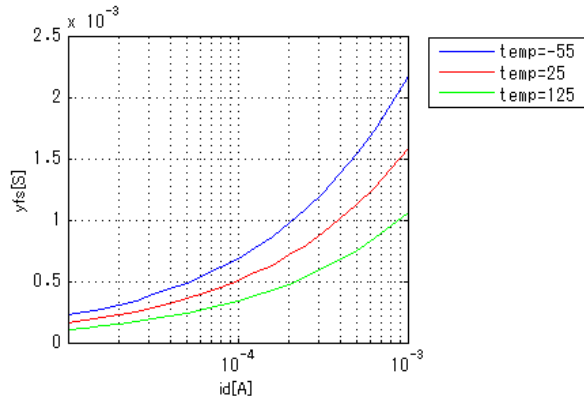
freq = 1000000Hz



Simulation results are following.
 Explanatory notes — : simulated

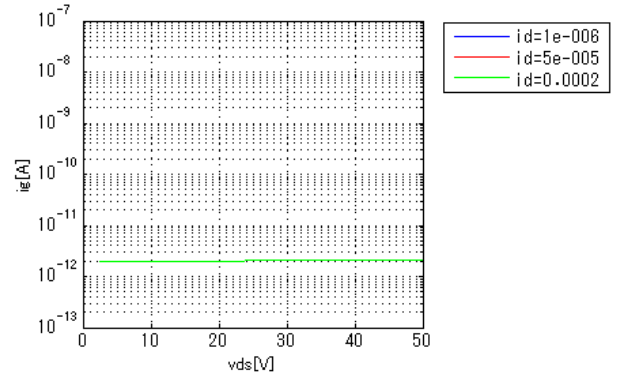
YfsId[Temp]

vd = 20V



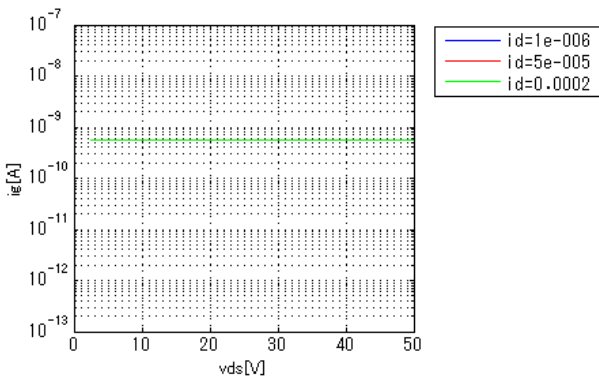
IgVdg[Id]

temp = 25degC



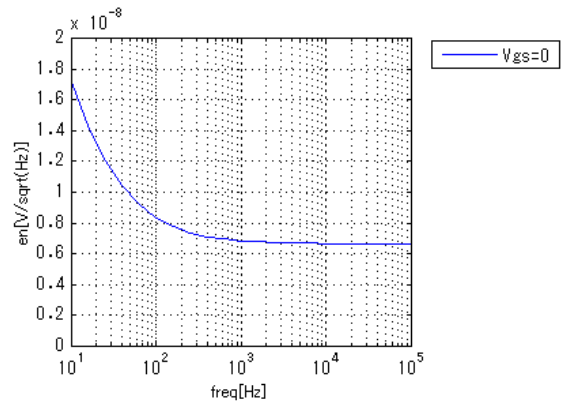
IgVdg[Id]2

temp = 125degC



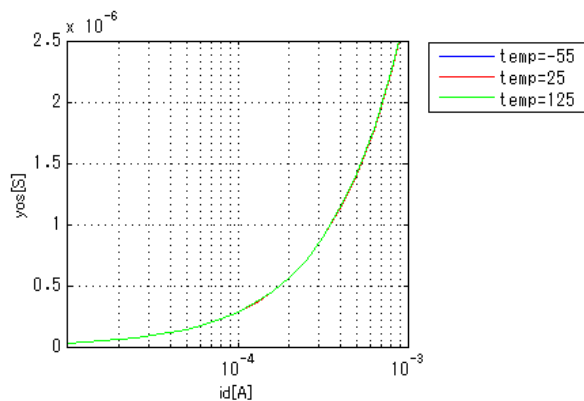
EnFreq[Vgs]

vds = 20V



YosId[Temp]

vd = 20V



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